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Research Article

Low-Power Fully Integrated CMOS DTV Tuner Front-End for ATSC Terrestrial Broadcasting

Jianhong Xiao, Guang Zhang, Tianwei Li, and Jose Silva-Martinez

Analog and Mixed Signal Center, Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843-3128, USA

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A low-cost low-power DTV tuner for current digital television application is described. In order to increase integration level and reduce power consumption for off-air DTV tuner application, an SAW-filterless tuner front-end architecture is adopted. As a part of the concept, key building blocks for this architecture are implemented on a main stream 0.35 μm CMOS technology. Experimental measurements for the prototype chip validate the system architecture; the prototype consumes 300 mw and achieves 45 dB of image rejection ratio within the entire 750 MHz frequency band.

1. INTRODUCTION

Digital television (DTV) broadcasting will replace conventional analog television broadcasting, according to FCC requirements [1]. Currently, both cable and off-air DTV receivers are widely demanded in actual consumer electronic market. These receivers are used in many electronic systems like HDTV (high-definition TV), set-top box, VCR/DVD, computer TV, and even portable devices like PDA and cell phones. A major power expender and costly device in the receiver is the front-end, especially the DTV tuner. The DTV tuner selects the desired television channel from many channels available and down-converts it to the standard intermediate frequency (i.e., 44 MHz) with enough quality. Due to high dynamic range and large image rejection ratio requirements, conventional DTV tuner has high manufacturing cost and huge power consumption [2]. However, low-power low-cost DTV tuners are preferred to meet the increased personal multimedia entertainment demands. For emerging applications such as portable TV, low-power consumption is critical to extend battery life; a high-integration and low-power off-air DTV tuner is mandatory in such applications.

In this paper, system specifications and design challenges for ATSC 8-VSB off-air DTV tuner system are discussed in Section 2; most relevant parameters such as dynamic range needed, noise figure, and image rejection are further studied. In Section 3, based on conventional dual conversion architecture review, a complex architecture using a single down-conversion is proposed for low-cost and low-power DTV tuner designs. In order to verify the concepts, the tuner front-end is implemented in a mainstream CMOS technology; the main design issues are discussed in Section 4. Fabrication and measurement results are given in Section 5. The conclusions are drawn in the final section.

2. ATSC TERRESTRIAL DTV TUNER SYSTEM

8-VSB is the modulation scheme used for USA digital television broadcasting. According to ATSC digital television standard [1], digital television information including video and audio are compressed into MPEG-2 format first; the digital data is modulated with 8-VSB and up-converted to the desired RF channel for the transmission. Digital television uses the same frequency plan as conventional analog TV broadcasting, which is from 54 MHz up to 806 MHz. For the receiver design, the major difference between analog TV and digital TV is the threshold signal-to-noise ratio (SNR) requirement for the demodulator. Due to noise-like flat spectrum (digital television) instead of discrete carriers (analog television), the SNR for DTV only needs to be 15 dB, which potentially makes it suitable for wide coverage broadcasting. The system specifications for RF tuner are derived based on [1] and listed in Table 1.

For the RF tuner used in North America, the desired channel must be properly selected and translated to 44 MHz.

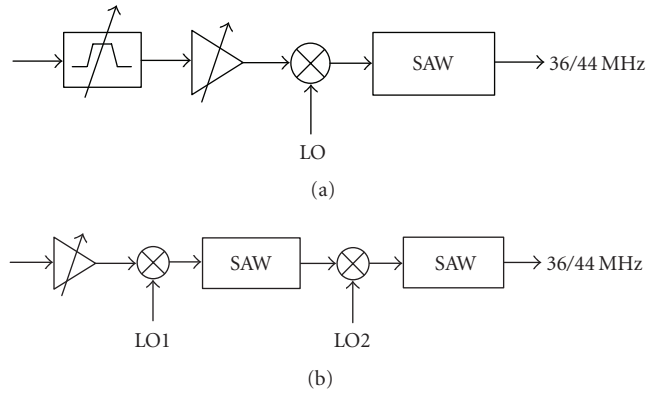


Figure 1: Typical TV-tuner architectures: (a) single-conversion; (b) dual-conversion.

Table 1: System specifications for off-air 8-VSB tuner.

Parameter	Value
Channel bandwidth	6 MHz
DTV frequency range	54 MHz to 806 MHz
Input power	−83 dBm to −10 dBm
Output range	1 V_p @ 500 Ω = 0 dBm
Intermediate frequency	44 MHz
System gain range	83 dB to 10 dB
NF	8 dB
IIP3	13 dBm
Minimum SNR	15 dB
Channel selection ratio	50 dB
Image rejection ratio	65 dB

The minimum power of the desired channel can be as small as −83 dBm, which determines the system sensitivity. Correspondingly, around 8 dB tuner noise figure (NF) is defined so that the tuner output SNR is not less than 15 dB for minimum signal input. Although the maximum input power for the DTV tuner is not specified in the standard, −10 dBm is a practical value for real implementations. Without considering any interference, 73 dB variable-gain range is required to ensure an output peak signal of around 1 volt. In practice, the desired channel is usually received with multiple interferences. Currently, analog TV broadcasting and digital TV broadcasting are coexisting; hence, these interferences are mainly undesired digital TV and/or analog TV channels. The interferences generate distortion components in the desired channel due to the unavoidable nonlinear characteristics of the devices used in the TV-tuner implementation. As a result, the power level of those interference channels can be 40 dB higher than the desired channel, which requires over 10 dBm IIP3 for the tuner design. In addition to the linearity requirement, a sharp selection ratio is necessary to attenuate the interference channels enough at the output of the tuner so that the analog-to-digital converter in the demodulator is not saturated. In the worst case, the tuner has to provide over 50 dB attenuation for the adjacent channel, which defines the baseband filter requirements.

Another important specification listed in Table 1 is the image rejection ratio. Image rejection is a fundamental requirement for all heterodyne receivers. In this specific application, because the final intermediate frequency is 44 MHz, the image channel is 88 MHz away from the desired channel; the required image rejection ratio is usually over 60 dB. This image rejection requirement is a critical factor for the tuner architecture design [2], which will be discussed in the next section.

3. DOUBLE-QUADRATURE DOWN-CONVERSION ARCHITECTURE

Nowadays, the most popular tuner architectures are the single-conversion topology with bulky off-chip tracking filter and the dual-conversion tuner; both tuner architectures are shown in Figure 1. As shown in Figure 1(a), the center frequency of the tracking filter is set according to the desired channel frequency and the desired channel is preselected. After this tracking filter, the image channels are further attenuated and single down-conversion architectures without huge image rejection ratio requirement can then be used. Usually after the down-conversion, an off-chip SAW filter is used to achieve the desired selectivity. As a result of the use of the tracking filter, the tuner architecture is further simplified. However, the tracking filter has to be widely programmable, from 50 MHz up to 800 MHz, and cannot be implemented on-chip in current CMOS technologies; therefore, this architecture is not suitable for cheap integrated tuner solutions.

In dual conversion architectures, as depicted in Figure 1(b), the desired channel is first up-converted to a high intermediate frequency like 1.1 GHz; the channel is preselected by an off-chip high-Q bandpass SAW filter and then down-converted to the standard 44 MHz frequency. Due to the first

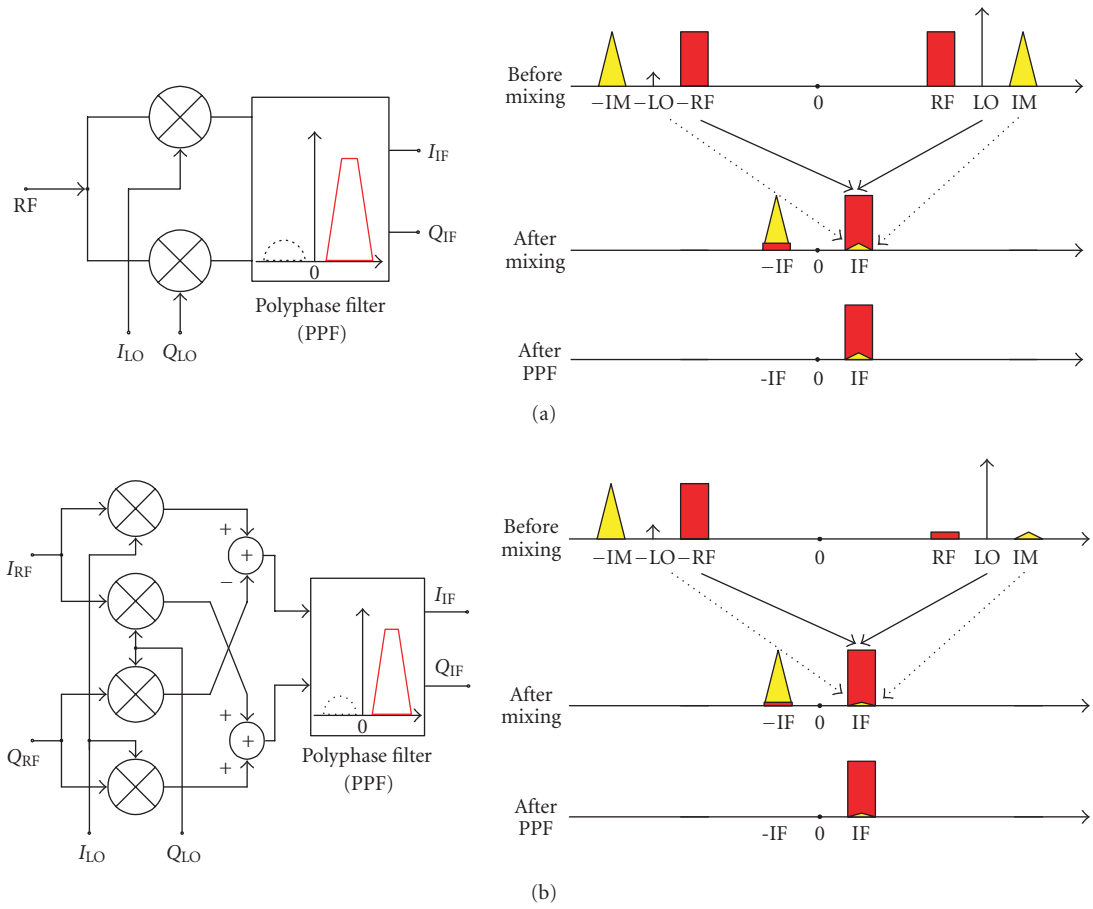


Figure 2: (a) Single-quadrature down-converter; (b) double-quadrature down-converter.

up-conversion, the frequency of the image channel is out of band and thus not relevant. In the down-conversion process, however, the image channel is fixed and 88 MHz away from the desired channel but the high-Q off-chip SAW filter attenuates this image channel by more than 30 dB. The second mixer (usually image rejection quadrature mixer) also provides more than 30 dB image rejection. Therefore, over 60 dB image rejection ratio can be achieved without major challenges, and the tuner (except for the two SAW filters) has more integration level than Figure 1(a). This dual-conversion architecture is the most popular solution for market available integrated DTV tuners [2–4]. The main drawbacks of this architecture are high-power consumption and the need of off-chip SAW filters. Due to the up-conversion, the RF front-end circuits have to work at higher frequency (over 1 GHz) and the resulting power consumption of the overall tuner is usually over 1 W. Unfortunately, it is hard to design robust and precise narrowband ($Q > 300$) on-chip filters to replace the SAW filter; hence, the tuner cannot be fully integrated. These drawbacks limit this architecture for future low-power low-cost tuner systems.

In both architectures shown in Figure 1, the image rejection specification is the key consideration; the specifications are achieved due to the filtering involved using either variable-frequency tracking filters or fixed-frequency SAW filters. In principle, the image channels can also be rejected if image cancellation architectures like Hartley and Weaver mixers are used; therefore, undersampling demodulation methods that eliminate the use of off-chip components could be used. However, those architectures suffer from I/Q mismatch and it is not possible to achieve 60 dB image rejection ratio without the use of sophisticated calibration schemes [5]. The main principles and limitations of the conventional image cancelation architecture are discussed below.

The typical quadrature down-converter is shown in Figure 2(a), where the RF input is mixed with two quadrature LO signals and the quadrature outputs of the mixer are processed by the image rejection polyphase filter. For the analysis, the RF input can be expressed as $A_{RF}\cos(\omega_{RF}t) + A_{IM}\cos(\omega_{IM}t)$; the ideal quadrature LO signals can be described as $A_{LO}\cos(\omega_{LO}t)$ and $A_{LO}\sin(\omega_{LO}t)$. A_{RF}, A_{IM}, and A_{LO} are the amplitudes of desired RF signal, image signal, and LO signal, respectively; it is assumed that there is no mismatch between quadrature LO signals in this stage. For simplicity, the quadrature LOs can be combined and viewed as a complex LO signal $A_{LO}e^{j\omega_{LO}t}$. Thus the

quadrature output of the mixer can also be expressed as $[A_{RF}\cos(\omega_{RF}t) + A_{IM}\cos(\omega_{IM}t)]A_{LO}e^{j\omega_{LO}t}$.

If $\omega_{IF} = \omega_{LO} - \omega_{RF}$, and ignoring the high frequency components ($\omega_{RF} + \omega_{LO}$ and $\omega_{IM} + \omega_{LO}$), the output can be further simplified as $(1/2)A_{RF}A_{LO}e^{j\omega_{IF}t} + (1/2)A_{IM}A_{LO}e^{-j\omega_{IF}t}$. Therefore, after the down-conversion, the desired RF signal and undesired image signal are separated as positive IF and negative IF. The polyphase filter after the mixer ideally eliminates the negative frequency components and passes the positive frequencies only. Usually the image rejection ratio is defined as P_{image}/P_{signal}, where P_{image} is the power of the image signal present at the output of the mixer's output and P_{signal} is the desired signal power at the same output. Therefore, the overall image rejection ratio only depends on the image attenuation provided by the polyphase filter, which can be as high as 60 dB with proper polyphase filter design. However, practical device mismatches and process parameter tolerances limit the overall image rejection performance. For example, the quadrature mismatch between LO signals can drastically degrade image rejection ratio, as graphically shown in Figure 2(a). In ideal case, the spectrum of the complex LO should consist of a single tone (positive LO in this case); the mismatch of the LOs generates a small negative LO component. This undesired negative LO mixes with undesired positive image signal and the product falls within the desired positive IF frequency, which cannot be filtered away by the polyphase filter. Hence, even if the polyphase filter has infinite image attenuation, the achievable image rejection ratio IIR is finite and can be obtained as

$$\mathrm{IRR} \approx \frac{1}{4}\left[\left(\frac{\Delta A}{A}\right)^2 + \left(\tan(\Delta\Phi)\right)^2\right], \tag{1}$$

where ΔA is the overall gain mismatch between the I/Q paths and A is the nominal gain, $\Delta\Phi$ is the overall phase imbalance in radians. Both ΔA and $\Delta\Phi$ are determined by the LO and mixer's mismatches as shown below:

$$\begin{aligned} \frac{\Delta A}{A} &\approx \frac{\Delta A_{LO}}{A_{LO}} + \frac{\Delta G_{mixer}}{G_{mixer}}, \\ \tan(\Delta\Phi) &\approx \tan\left(\Delta\Phi_{LO}\right) + \tan\left(\Delta\Phi_{mixer}\right), \end{aligned} \tag{2}$$

where the LO signals are modeled as $A_{LO}\cos(\omega_{LO}t)$ and $(A_{LO}+\Delta A_{LO})\cos(\omega_{LO}t+\Delta\Phi_{LO})$, and the mixer gains are modeled with $G_{mixer}e^{j\Phi_{mixer}}$ and $(G_{mixer} + \Delta G_{mixer})e^{j(\Phi_{mixer}+\Delta\Phi_{mixer})}$. Usually the LO amplitude mismatch is negligible compared with mixer gain mismatch, also the mixer's phase imbalance is negligible compared with LO's phase imbalance. To achieve 60 dB image rejection ratio, both LO phase mismatch and mixer normalized gain mismatch should be less than 0.1 degree and 0.1%, respectively. The mixer's gain mismatch can be minimized by using a proper architecture like passive mixer and good layout techniques, but the LO phase imbalance is usually over 1 degree even with sophisticated calibration, which implies that no more than 40 dB image rejection can be achieved. Therefore, to achieve over 60 dB image rejection ratio, double-quadrature architecture, which can relax the matching requirement of the LO, is preferred [6, 7].

As shown in Figure 2(b), the double-quadrature architecture handles the down-conversion with complex LO and complex RF signals. Four mixers are needed to achieve the complex down-conversion, as shown in the equation below:

$$\begin{aligned} I_{IF} + jQ_{IF} &= (I_{RF} + jQ_{RF}) \times (I_{LO} + jQ_{LO}) \\ &= (I_{RF}I_{LO} - Q_{RF}Q_{LO}) + j(I_{LO}Q_{RF} + Q_{LO}I_{RF}). \end{aligned} \tag{3}$$

Because the RF input is complex, only the negative frequency components (desired RF and undesired image signals) are present at the input of the mixer. Considering the mismatch between quadrature RF signals, part of the positive frequency components will be prefiltered before the mixing operation. Therefore, the undesired product due to negative LO and positive image, which cannot be filtered away by the complex filter as pointed earlier, will be much smaller than the counterpart in the conventional single quadrature architecture shown in Figure 2(b). IIR is still given by (1), but the overall gain mismatch and phase imbalance for double-quadrature architecture is obtained as

$$\begin{aligned} \frac{\Delta A}{A} &= \frac{\Delta A_{RF}}{A_{RF}}\frac{\Delta A_{LO}}{A_{LO}} + \frac{\Delta G_{mixer}}{G_{mixer}}, \\ \tan(\Delta\Phi) &= \tan\left(\Delta\Phi_{RF}\right) * \tan\left(\Delta\Phi_{LO}\right) + \tan\left(\Delta\Phi_{mixer}\right). \end{aligned} \tag{4}$$

Therefore, to achieve 60 dB image rejection ratio, assuming 0.1% mixer gain mismatch, only 2.4 degree phase imbalance and 3% gain mismatch are required for the quadrature RF and LO, which can be achieved even without any need of calibration scheme.

Based on the double-quadrature architecture, single-conversion DTV-tuner architecture can be built; the block diagram is shown in Figure 3. Off-air DTV signal is first received by the antenna and prefiltered by an external filter (not shown in Figure 3), which removes the out-of the DTV band interferences. A wideband on-chip low-noise variable-gain amplifier is used as a front-end and it must provide two functionalities. First, the gain of the low-noise amplifier (LNA) should be adjusted according to the dynamic range requirements, which ensures the output signal of the LNA not to saturate the following stages; for that purpose, the broadband LNA operates as a variable-gain amplifier as well. Second, this amplifier needs to convert the single-ended input signal into differential signal with good differential matching properties. Differential signals are required not only because of better common mode rejection but also the requirement of the RF quadrature generation. In this implementation, the RF quadrature signal generator is designed with a passive polyphase filter [8], which requires differential inputs

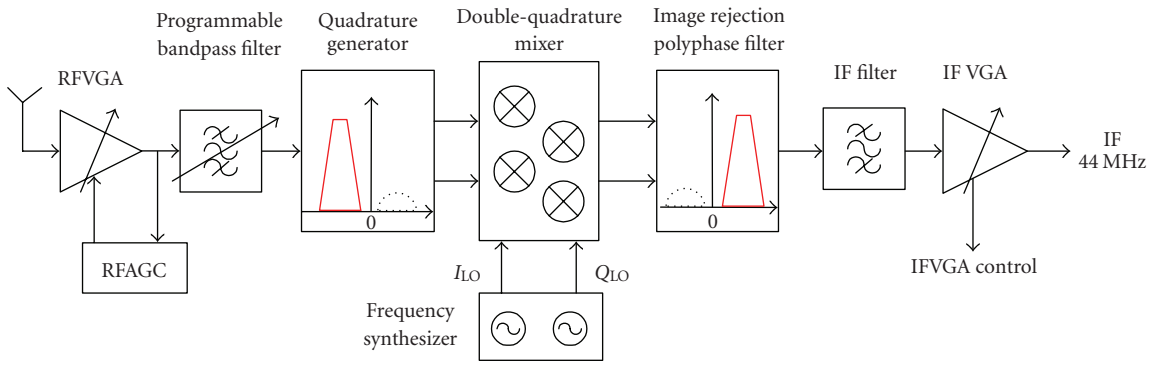


Figure 3: Double-quadrature DTV tuner architecture.

to generate quadrature outputs. The quality of the differential signal affects the matching performance of the quadrature RF and eventually degrades the overall system's IIR.

The programmable bandpass filter in Figure 3 serves to suppress the harmonic components. In this broadband system, the harmonics of the LO ($n \times$ LO) will mix with in-band interference channels ($n \times$ LO + IF) and generate additional undesired images, which cannot be filtered by the baseband filter and degrades the output-signal quality. The design of this programmable filter is still an issue. The double-quadrature down-converter provides inherited 3rd harmonic distortion suppression [6], and the programmable bandpass filter removes those 5 LO + IF interferences and achieves 5th harmonic component suppression as well. In addition, the programmable filter can also serve as rough band selection and relax linearity challenges of the following stages.

After image rejection due to IF complex filter, some baseband blocks including the baseband filter and a low-frequency variable-gain amplifier are used to further reject the out-of-band signals and amplify the desired signal before the conversion of the selected channel to digital format. With double-quadrature down-conversion architecture, 60 dB image rejection ratio is achievable without requiring any bulky tracking filters or high frequency off-chip SAW filter. This will greatly reduce manufacturing cost and minimize power consumption.

4. DESIGN OF THE BASIC BUILDING BLOCKS

Currently, most of the integrated terrestrial and cable DTV tuners are built with bipolar or BiCMOS technologies [2, 4, 9], which are more expensive than mainstream CMOS technology. Furthermore, with the increasing demand for system integration (tuner, ADC, and decoder), CMOS implementation will greatly reduce the overall silicon area, power consumption, and cost. Therefore, 0.35 μm CMOS technology is chosen for the design of this prototype. In this chip, the main goal is to verify the image rejection concept and only the most critical blocks are designed. These blocks include wideband (fixed gain in this prototype) LNA, double-quadrature down-converter, and frequency synthesizer.

Table 2: LNA designs pecifications.

Parameter	Value
Bandwidth	50 MHz $\sim$ 850 MHz
Gain	16 dB
Noise figure (NF)	3 dB
S11	< -10 dB
Differential phase error	$\pm 2^\circ$
Differential magnitude error	$\pm 1\%$

4.1. Wideband LNA design

The front-end low-noise amplifier needs to provide variable-gain function and accurate single-ended to differential conversion. The variable-gain amplifier for DTV tuner has been reported in [2, 3, 10, 11]; here we are mainly focusing on the implementation of single-ended to differential conversion then a fixed-gain LNA was designed. As shown in Figure 4, the first stage of the LNA is a typical shunt-feedback LNA structure. The gain of the amplifier is mainly decided by the transistor M0, feedback resistor R_F, and load resistor R_{L0}. The feedback resistor R_F provides broadband input impedance matching. The design specifications of the LNA including gain, noise figure, and input return loss are given in Table 2. The detailed design procedure for the shunt-feedback LNA can be found elsewhere; see for instance [12].

The second and third stages of the LNA are designed to generate differential signal with proper matching performance, as listed in Table 2. There are several topologies reported in the literature [13] but a single differential pair is an efficient yet robust approach. The single differential pair with one terminal grounded is shown in Figure 5(a), which is the basic analog cell for the differential generation. In the ideal case, differential output current $(1/2)g_m v_{\text{in}}$ can be obtained, where g_m is the small signal transconductance of M1 (ideally equal to M2). However, due to the parasitic capacitances, the signals at the drain of M1 and M2 are not perfectly matched. Furthermore, this mismatch is frequency-dependent, mainly due to the capacitances present at the common-source node

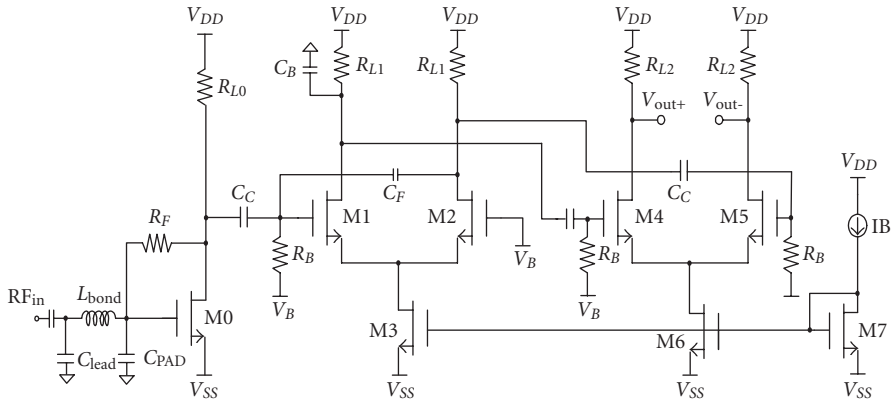


Figure 4: Wideband LNA schematic.

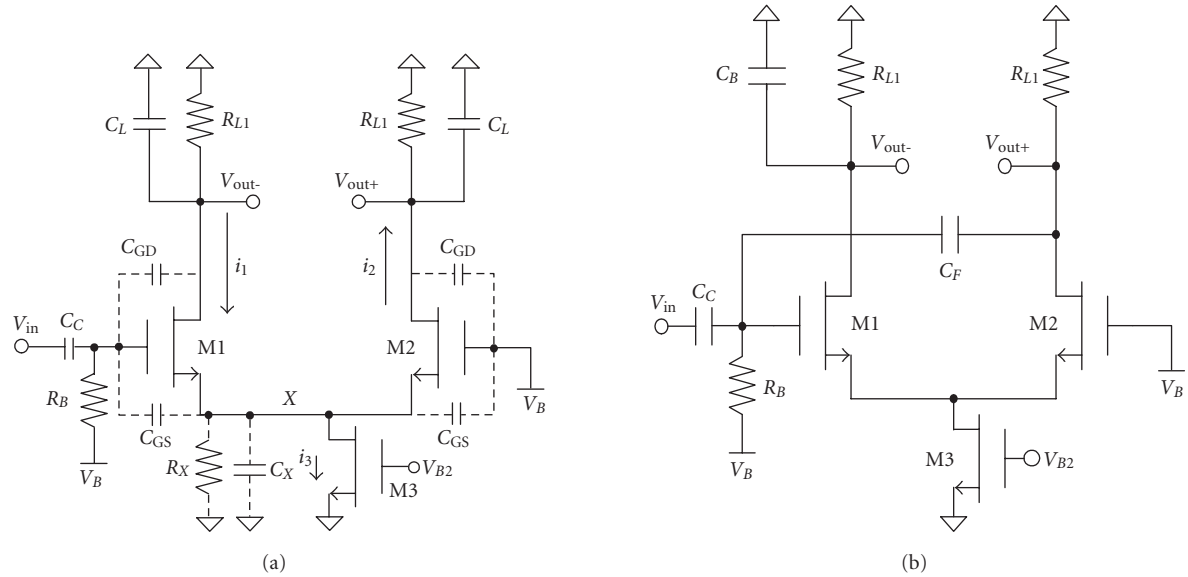


Figure 5: Single-to-differential converter: (a) single differential pair; (b) compensated differential pair.

of M1 and M2. To analyze the broadband matching performance of the circuit, the parasitic capacitors are included and the differential outputs can be obtained as

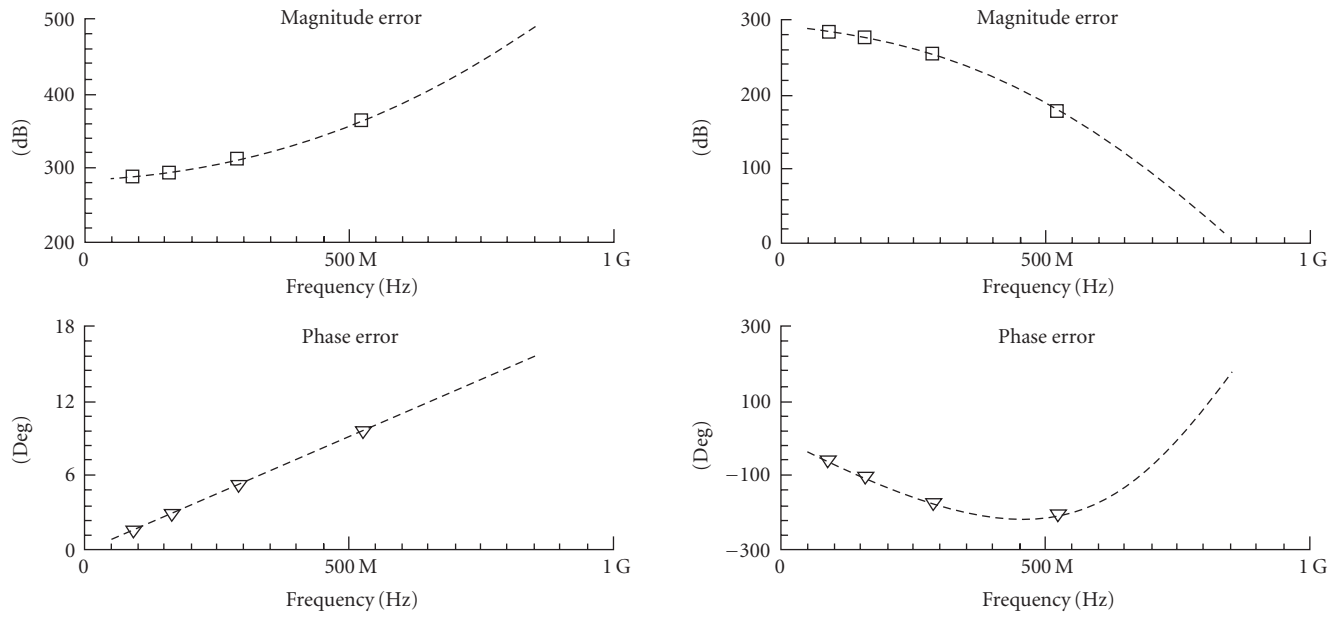
$$v_{out+} = \frac{(g_m R_{L1}/2)(1+s(C_{GS}/g_m))}{(1+g_X/2g_m)(1+s((C_X+2C_{GS})/(g_X+2g_m)))(1+sR_{L1}C_L)} \cdot v_{in}, \quad (5a)$$

$$v_{out-} = -\frac{(g_m R_{L1}/2)(1+g_X/g_m)(1+s((C_{GS}+C_X)/(g_m+g_X)))}{(1+g_X/2g_m)(1+s((C_X+2C_{GS})/(g_X+2g_m)))(1+sR_{L1}C_L)} \cdot v_{in}, \quad (5b)$$

where C_{GS} and C_{GD} are input pair's gate to source and gate to drain parasitic capacitances; $R_X = 1/g_X$ and C_X are the resistance and capacitance lumped to node X, respectively; C_L is the overall load capacitance. In the analysis above, both transistors are assumed perfectly matched; C_{GD} is ignored because it can be shown that the error introduced by the common source node is dominant compared with the error generated by C_{GD}. The mismatch between the two output signals is better appreciated if the ratio of both output signals is considered as follows:

$$\frac{v_{out+}}{v_{out-}} = -\left(\frac{1}{1+g_X/g_m}\right)\left(\frac{1+s(C_{GS}/g_m)}{1+s((C_{GS}+C_X)/(g_X+g_m))}\right). \quad (6)$$

At low frequencies, the pole and zero can be ignored and the mismatch is mainly defined by g_X/g_m, which can be minimized with proper design of the current source. At higher frequencies, the parasitic capacitances play the most relevant role and the mismatch (especially the phase mismatch) gets worse. According to Cadence results, the magnitude error and phase error for the conventional converter (Figure 5(a))



(a) Without compensation

(b) With compensation

Figure 6: Magnitude and phase mismatch plots (a) single differential pair; (b) compensated differential pair.

can be as high as 0.5 dB and 16° in the entire 50–800 MHz frequency band, as shown in Figure 6(a). Clearly this error cannot be afforded in the proposed TV tuner architecture. Notice that phase error is by far the most critical one.

In order to minimize the aforementioned mismatch, two compensation capacitors are added to balance the overall gain transfer function. First, a capacitor C_F is added between amplifier's input and noninverting output, as shown in Figure 5(b); the inverting output will not be affected by C_F but the noninverting output voltage will be modified as

$$v_{\text{out+}} \approx \frac{(g_m/2)\,(1+s((C_{\text{GS}}+2C_F)/g_m))}{(1+s((C_X+2C_{\text{GS}})/2g_m))\,(1/R_{L1}+sC_L+sC_F)}\,v_{\text{in}}. \tag{7a}$$

During the derivation, g_X term is neglected if considering $g_X/g_m \ll 1$, which is valid when the current source is designed to have large output impedance.

Comparing (7a) with (5b), if bypass capacitance C_F is $C_X/2$, the bypass capacitance shifts the zero of noninverting output to the frequency exactly as the inverting one. However, the bypass capacitance also shifts the pole of the noninverting output to lower frequency, which introduces additional errors. By adding an extra capacitor (C_B) to the inverting output node, the $v_{\text{out}-}$ pole can be shifted to lower frequency to fully balance the architecture; the inverting output can be rewritten as

$$v_{\text{out}-} \approx -\frac{(g_m R_{L1}/2)\,(1+s((C_{\text{GS}}+C_X)/g_m))}{(1+s((C_X+2C_{\text{GS}})/2g_m))\,(1+sR_{L1}(C_L+sC_B))}\,v_{\text{in}}. \tag{7b}$$

Therefore, by selecting the compensating capacitors $C_F = C_B = C_X/2$, the differential outputs are perfectly matched in ideal case. In this design, C_X is around 200 fF, C_F and C_B are designed as 100 fF. According to cadence simulations, the magnitude and phase error over the entire DTV band were reduced down to 0.5 dB and 0.3°, respectively, as shown in Figure 6(b). This novel method features simplicity and excellent improvement without additional power consumption.

The third stage of the LNA shown in Figure 4 is a standard differential pair, which further suppresses the differential mismatch due to its inherent common mode rejection property. Also this circuit serves as a buffer, which provides output impedance matching for the LNA stand-alone measurement. The entire LNA is depicted in Figure 4.

4.2. Double-quadrature down-converter design

The broadband quadrature signal generator is the critical block of the double-quadrature down-converter. In order to generate such broadband quadrature signal with less than 3% I/Q mismatch, we need a filter's attenuation of at least 40 dB for the entire image frequency band from positive 50 MHz up

Table 3: Component values of quadrature generator.

R1	C1	R2	C2	R3	C3	R4	C4	R5	C5
125 Ω	1.29 pF	250 Ω	1.25 pF	500 Ω	1.52 pF	1000 Ω	1.85 pF	2000 ΩF	1.79 pF

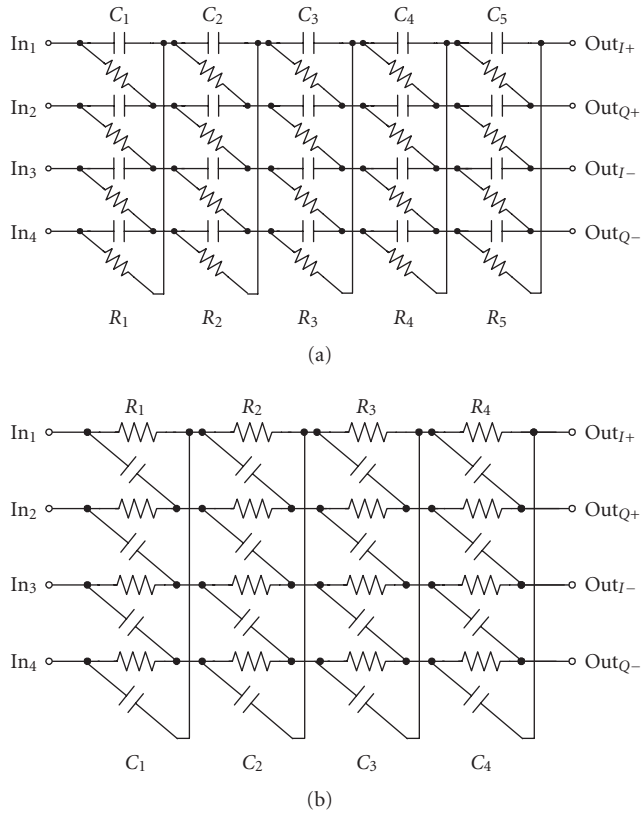


Figure 7: Schematic of (a) quadrature generator and (b) image rejection filter.

to 806 MHz; these specifications can be achieved if a multistage passive polyphase filter is used [6–8, 14]. The schematic of a broadband generator is shown in Figure 7(a); the differential RF signals are applied at nodes in1 (and in2) and in3 (and in4), respectively.

Due to the presence of the unavoidable PVT variations, on-chip resistors and capacitors deviate from the nominal values. Therefore, the filter must be over-designed to cover the 30% RC time constant variations. The poles are evenly distributed in log scale from 40 MHz up to 1.1 GHz. In addition to the aforementioned variations, the mismatch between the RC components also introduces additional I/Q mismatch and affects the image rejection performance [15]. It has been verified using Monte Carlo simulations that mismatches of 1% in both resistors and capacitors are enough to achieve 1% I/Q matching.

The design challenge of the polyphase circuit comes from the gain and noise figure requirements. This circuit is passive and presents losses that have to be minimized not to degrade the down-converter overall noise figure; that implies that the impedance of each filters stage has to be tapped up from the first stage to final stage. Also, due to the lossy property of this circuit, the final stage is the dominant noise source of this filter; hence small-value resistor at the final stage is preferred to minimize the noise figure. But this constraint adds a design challenge because the previous stage of this quadrature generator needs to drive low impedances from 50 MHz up to 1 GHz. A proper design strategy to deal with the tradeoff between noise and gain is required; the component values are set as listed in Table 3. Notice that high frequency poles are distributed at the earlier stages to allocate smaller resistor in the early stages. The simulated frequency response plots for the quadrature generator are given in Figure 8(a). The positive frequency attenuation is over 40 dB from 40 MHz to 1.1 GHz, and less than −4 dB attenuation is observed for the negative (desired) frequency input. In this paper, positive frequency means the phases of the inputs are counterclockwise and negative frequency means the phases of the inputs are clockwise.

Similar to the quadrature signal generator, the IF image rejection filter uses a passive polyphase filter structure as shown in Figure 7(b). The image rejection filter provides more than 60 dB attenuation over the image band (negative 41 MHz to 47 MHz). Instead of five stages, four stages are enough to cover the frequency range from 32 MHz to 63 MHz, which is over-designed, even considering 25% process variation. For the operation of the image rejection filter, the quadrature outputs of the mixer are directly connected to the four inputs of the filter (counterclockwise phase). The frequency response plot for this filter is shown in Figure 8(b).

A main concern of the IF filter is the high component's matching requirement. In the case of components mismatch, undesired image signal will be coupled to the desired passband signal, which degrades the image rejection ratio; 0.1% mismatch is required to ensure less than −60 dBc coupling. The resistors and capacitors values have been properly selected to achieve the matching requirement. Also, careful layout techniques such as common centroid, placement of dummy elements, and minimization of parasitic capacitances have been used to improve the matching of components.

As mentioned in Section 3, four mixers are required to implement the fully complex mixer. The double-quadrautre architecture relaxes the matching requirement for the RF and LO inputs; however, the matching requirement for the mixer remains in the range of 0.1%, which is still quite challenging. Passive CMOS switching mixer is chosen because it has better tradeoff between matching and power consumption [6, 8]; large-size transistors are used to improve the matching of

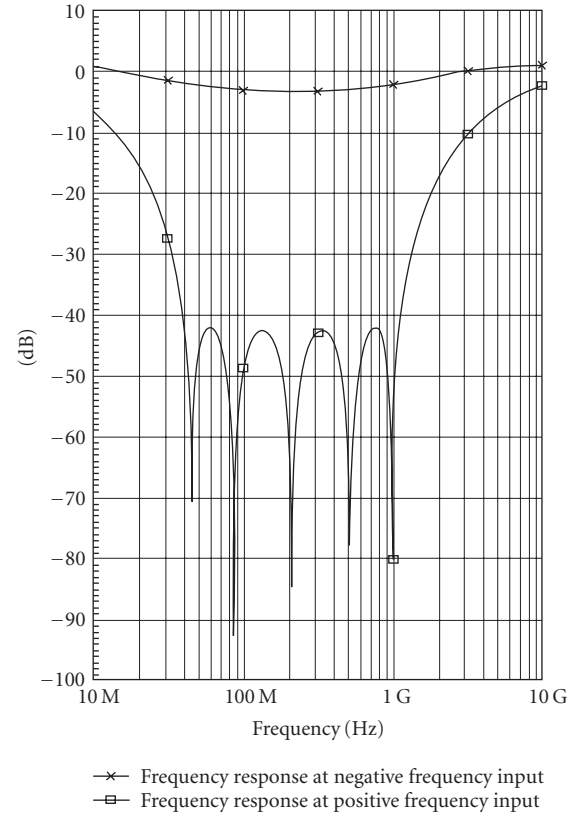


Figure 8: Frequency response plot of (a) quadrature generator and (b) image rejection filter.

the mixer section while power consumption is not affected. High swing LO is used to have high over-drive voltage, which also decreases the noise contribution of the switches. On the other hand, the passive mixer does not provide voltage gain and it adversely affect the noise level unless it is terminated using active devices as shown in Figure 9 [14, 16]. To drive the small input impedance of the passive mixer, a source-follower-based buffer is inserted between the quadrature generator and the mixer. If ideal square wave LO and infinite-gain amplifier are assumed, the mixer's gain can be obtained as

$$\frac{v_{\text{out}}}{v_{\text{RF}}} = \frac{2}{\pi}\left(\mu_n C_{\text{ox}}\frac{W}{L}\right)\left(\frac{R}{1+sRC}\right)V_{\text{LO}}, \tag{8}$$

where μ_n is the channel mobility factor and C_{ox} is the gate oxide capacitance; W/L is the aspect ratio of the switch transistor; R and C are the feedback resistor and capacitor; V_{LO} is the amplitude of the LO signal. The gain is proportional to the LO swing and feedback resistor. With proper design, the gain of the mixer can be around 8 dB, which is beneficial because it minimizes the noise contribution from the IF stages.

Although the added active transimpedance amplifier provides gain boosting for this passive mixer, it may degrade the matching performance of the mixer. If the amplifier has large gain at the desired IF band, the matching of the transimpedance amplifier will be mainly defined by the matching of feedback resistors and capacitors, which can be as good as 0.1%. A related issue is the required OPAMP gain at 44 MHz to achieve the required accuracy. In this prototype, the amplifier is essentially a simple one-stage operational transconductance amplifier (OTA), which is composed of NMOS differential pair and PMOS current source load can be found elsewhere, for instance, [17]. The gain of the amplifier is only around 30 dB at 44 MHz. With more advanced technologies such as 0.18 μm CMOS and better amplifier topologies, it is expected to achieve better performance.

The mixer's overall input-referred noise power spectral density can be obtained as

$$v_{n\_\text{in}}{}^2 = 4KT\frac{1}{g_0} + KT\frac{\pi^2(1+sRC)^2}{g_0{}^2R} + \frac{\pi^2 v_{n\_\text{OTAin}}{}^2 G_{m\text{OTA}}{}^2}{4g_0{}^2}, \tag{9}$$

where $g_0 = \mu_n C_{\text{ox}}(W/L)V_{\text{LO}}$, K is the Boltzmann constant, and T is the absolute temperature in Kelvin degrees; the OTA input-referred spectral noise density and overall transconductance are denoted as v_{n_OTAin} and $G_{m\text{OTA}}$, respectively. The dominant noise sources of this mixer are due to the switches and OTA, which can be minimized by reducing switch-on resistance and increasing the transconductance of the OTA's input stage. For the complete down-converter design, the overall gain is around −4 dB and noise figure is less than 20 dB; IIP3 is expected to be around 10 dBm.

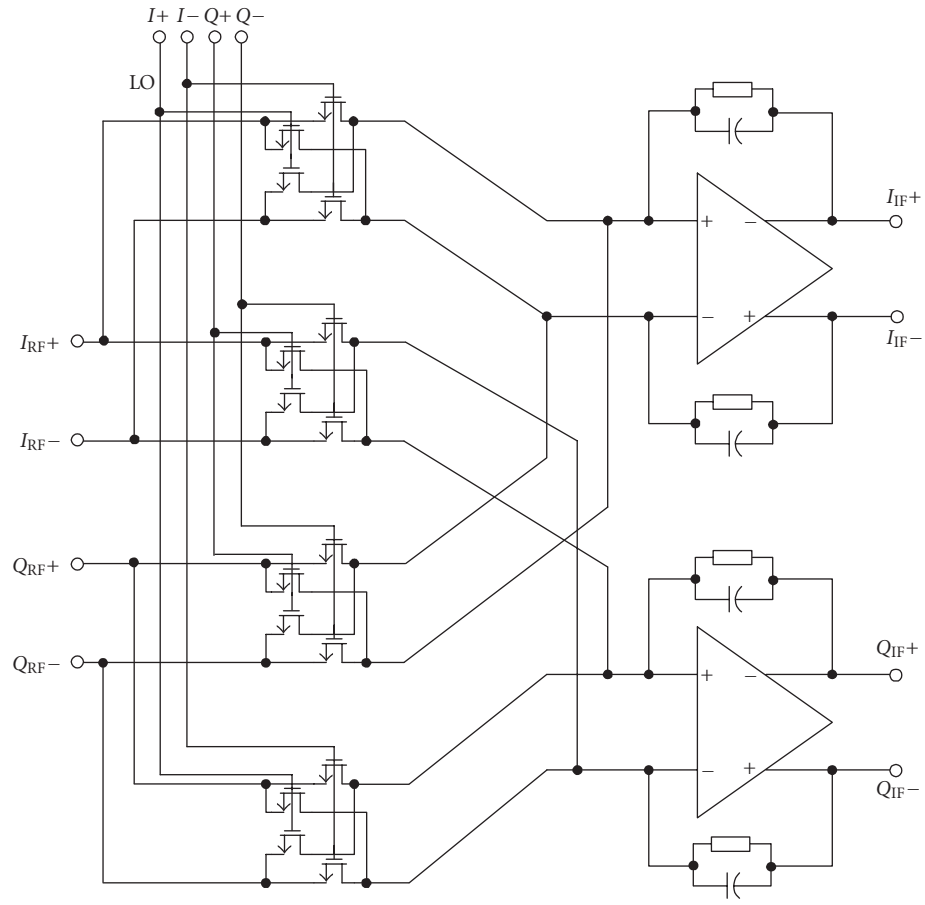


Figure 9: Double-quadrature passive mixer schematic.

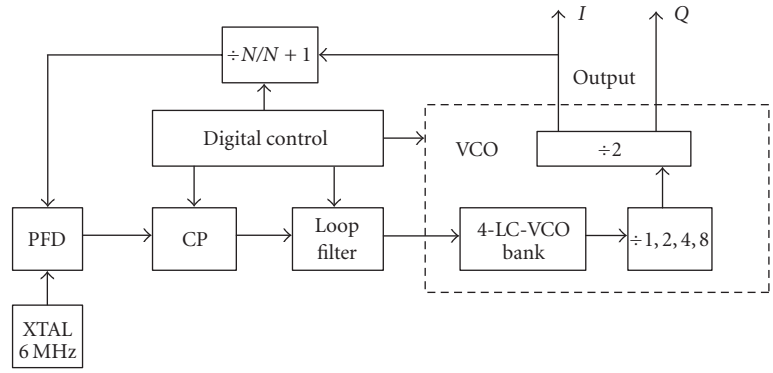


Figure 10: Frequency-synthesizer-concept block diagram.

4.3. Frequency synthesizer design

The major requirements for the frequency synthesizer are low phase noise (less than −76 dBc in 10 kHz offset) and wide frequency tuning range (98 MHz–850 MHz); the block diagram of the frequency synthesizer is shown in Figure 10. Phase noise of frequency synthesizer is strongly affected by the voltage control oscillator phase-noise performance, which is usually decided by inductor's quality factor Q achieved on-chip. For the 0.35 μm technology used, inductor Q is limited to be around 3 according to our simulations, and previously reported results [18]; more advanced technologies such as 0.18 μm and 0.13 μm have higher-Q inductors (>10). The other major design challenge is its wide

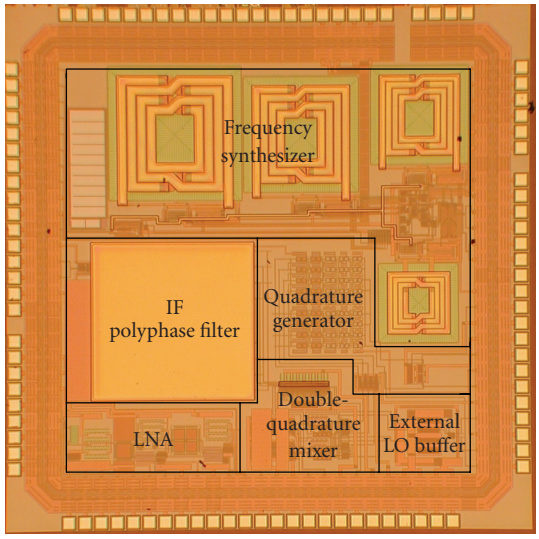


Figure 11: CMOS DTV tuner front-end layout.

tuning range (around 800 MHz). The typical tuning range of a stand-alone varactor might be in the range of ±30%, but when inserted in a system, the tuning range decreases to no more than ±12%. Better results can be obtained if BiCMOS technologies are used, but in general, it is extremely difficult to have such wide tuning range with good enough phase noise for the entire DTV bandwidth. In this work, four LC VCOs are used to cover such wide frequency band. Digital control selects the proper VCO and division ratio inside the 4-LC-VCO bank. A divide-by-2 circuit is used to generate accurate quadrature LO signals. The main building blocks of the PLL such as VCO are similar to those reported in [6, 10], and hence they are not further discussed.

In order to enable functionality test even without the on-chip PLL, an external LO also can be applied for tuner front-end. Multistage current-mode buffer has been used to adjust the LO signal to properly drive the passive mixer. To minimize signal feedthrough from digital to RF part, the digital circuits are isolated with guard rings; in addition, analog and digital supply lines are not shared.

5. EXPERIMENTAL RESULTS

In order to validate the aforementioned concepts, a test chip has been fabricated in the TSMC 0.35 μm technology through the MOSIS educational program; the die photograph is shown on Figure 11. The total active area for this die is roughly 3.5 mm $*$ 3.5 mm and packaged with TQFP100A. To test the chip, the test PCB board has been carefully designed, especially for the high frequency paths such as the RF input and external LO.

The measured LNA gain and noise figures are shown in Figure 12, where right-side scale is 2.3 dB/division and the left side is 1.8 dB/division, respectively. The low-frequency differential gain is around 24.2 dB; it drops down to 10 dB at 800 MHz. This unexpected frequency response is mainly due to the package frequency response limitation. The package size is around 10 mm $\times$ 10 mm and the bondwire inductor can be as large as 4nH; the lead capacitor is also around 2 $\sim$ 3 pF. To reduce this testing issue, QFN package with co mpact size should be used. The LNA overall noise figure is around 4.6 dB from 50 MHz to 850 MHz. The spike observed in certain frequencies like 210 MHz is mainly due to the coupling from instrument or hostile environment.

Table 4: Prototype measurement summary.

Parameter	Value
S11	>−7 dB
LNA gain	22 dB
LNA NF	4.5 dB
LNA differential phase error	±1.5°
LNA differential magnitude error	±0.65 dB
Down-converter gain	−6 dB
Down-converter NF	20 dB
Down-converter IIP3	7 dBm
Image rejection ratio	>45 dB
Total power consumption	300 mW

Figure 13 shows the measured differential mismatch including magnitude and phase. In the entire frequency range from 50 MHz to 800 MHz, the measured magnitude and phase mismatches are less than ±0.65 dB and ±1.5°, respectively. The measured matching performance is not as good as the simulation results, mainly due to the combination of transistor mismatches, bonding wire effects, and PCB stray capacitances. Nevertheless, the experimental results are still able to verify that the proposed calibration method together with the additional fully differential stage improve the circuit's matching performance.

The image rejection ratio at 200 MHz for the down-converter was measured; the results are shown in Figure 14. First, a 200 MHz signal with −20 dBm power level was applied to the RF input, and the output spectrum is shown in Figure 14(a). The LO is set as 244 MHz and the power of output signal (44 MHz) is −36.85 dBm. Second, the image signal (288 MHz) is applied with the same input power level, the output power at 44 MHz is −87.24 dBm. The output power difference is the image rejection ratio, which is 50 dB in this case. Similar procedure has been carried out for the entire DTV band and the measured broadband image rejection ratio is given in Figure 15. For most of the frequencies, image rejection ratio is over 40 dB. Although it is still less than the expected image rejection requirement, this prototype gave us better performance than the conventional down-converter.

The remaining parameters for the down-converter including gain, NF, and IIP3 are given in Table 4. This prototype failed to get measurement result for the frequency synthesizer because the output buffer did not operate properly. Excluding the frequency synthesizer, the LNA and down-converter consume around 300 mW power consumption with 3.3 V power supply in a standard 0.35 μm CMOS technology.

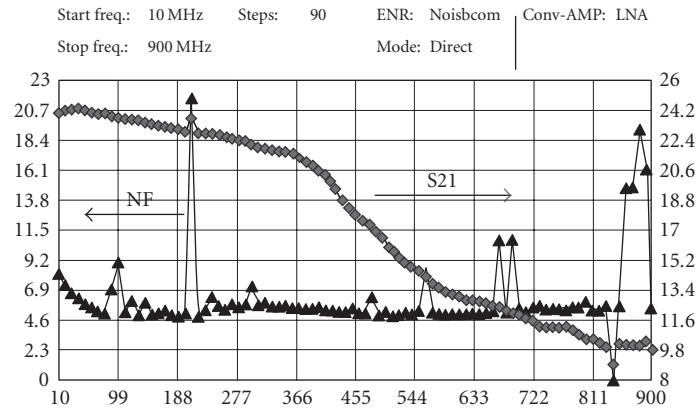


Figure 12: LNA gain and LNA NF measurements plot.

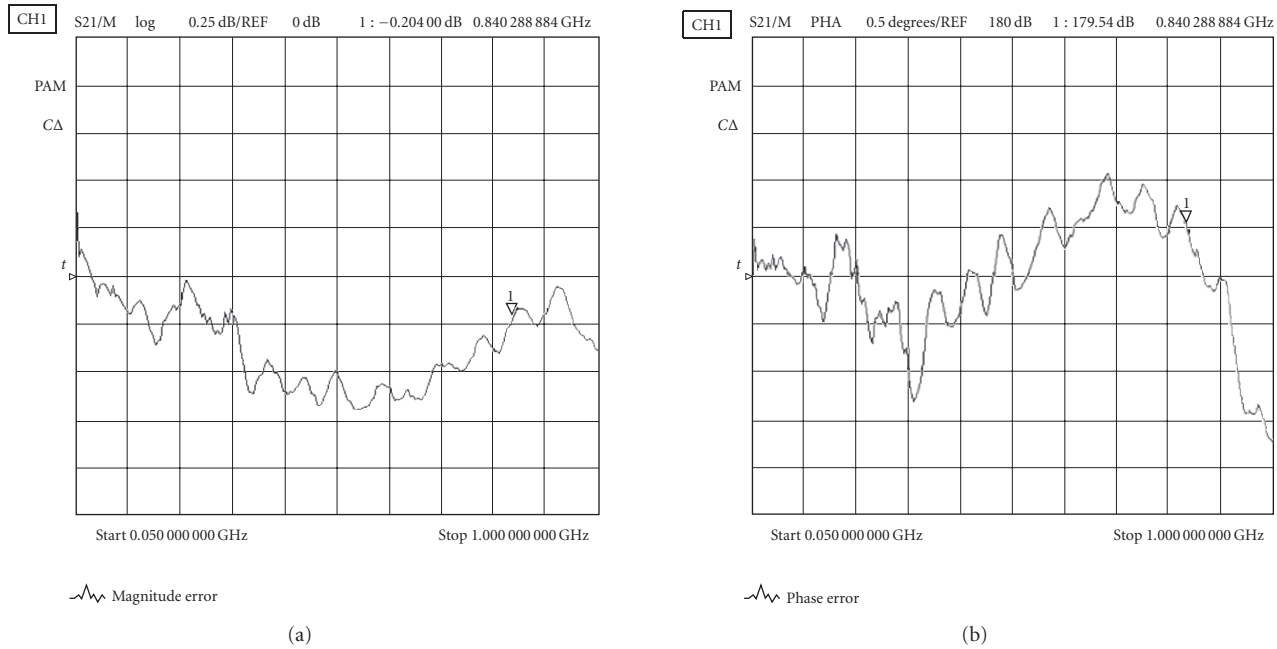


Figure 13: Experimental results: (a) LNA differential magnitude error plot; (b) phase error plot.

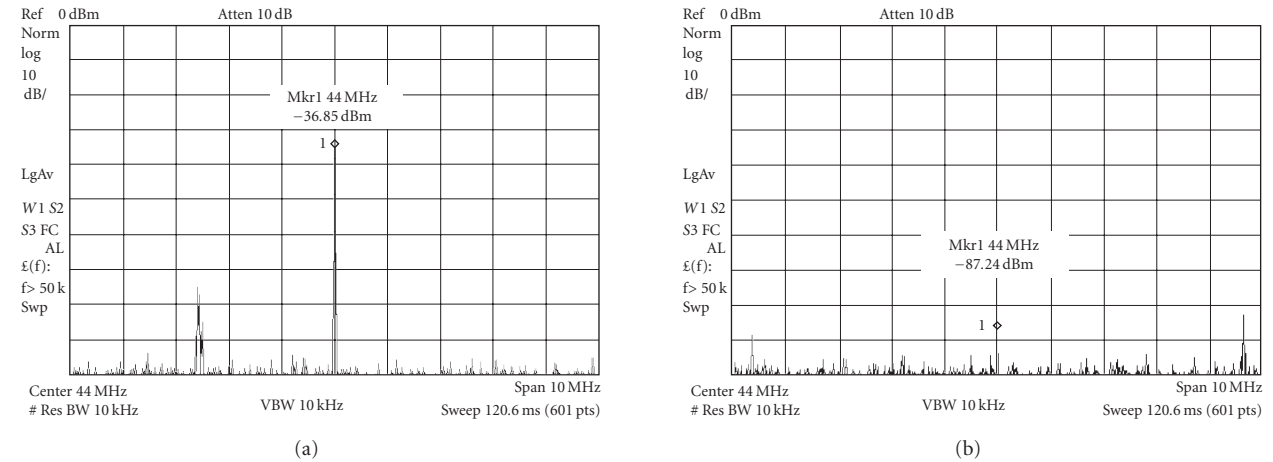


Figure 14: Output spectral plots at LO 244 MHz: (a) −20 dBm RF input at 200 MHz; (b) −20 dBm RF input at 288 MHz.

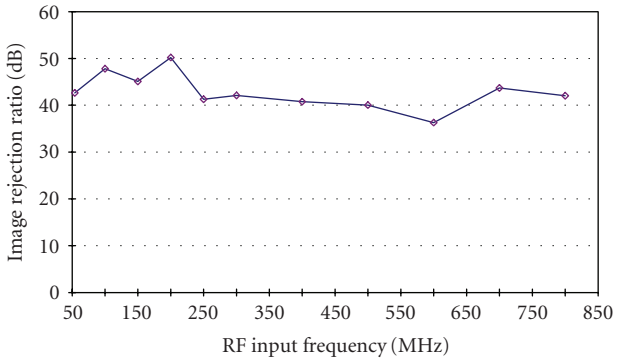


Figure 15: Measured image rejection ratio versus RF input frequency.

6. CONCLUSION

In this paper, a low-power low-cost architecture has been adopted for ATSC off-air DTV tuner application. The design issues as well as main design challenges were discussed. Relevant DTV tuner specifications were obtained. Among other building blocks, a novel mismatch compensation technique for single-ended to fully differential signal conversion without extra power consumption was proposed. The prototype chip for the key blocks was fabricated with low-cost digital 0.35 μm CMOS technology. Measurement results of the blocks mostly validate the proposed design approach. Based on this prototype, fully integrated terrestrial DTV tuner can be designed with less power consumption and lower manufacture cost.

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REFERENCES

[1] United States Advanced Television Systems Committee, "ATSC Digital Television Standard," September 1995.

[2] I. Mehr, S. Rose, S. Nesterenko, et al., "A dual-conversion tuner for multi-standard terrestrial and cable reception," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 340–343, Kyoto, Japan, June 2005.

[3] L. Connell, N. Hollenbeck, M. Bushman, et al., "A CMOS broadband tuner IC," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers (ISSCC '02)*, pp. 400–401, San Francisco, Calif, USA, February 2002.

[4] N. Scheinberg, R. Michels, V. Fedoroff, et al., "A GaAs up converter integrated circuit for a double conversion cable TV "set-top" tuner," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 6, pp. 688–692, 1994.

[5] L. Der and B. Razavi, "A 2-GHz CMOS image-reject receiver with LMS calibration," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 167–175, 2003.

[6] J. van Sinderen, F. Seneschal, E. Stikvoort, et al., "A 48-860MHz digital cable tuner IC with integrated RF and IF selectivity," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers (ISSCC '03)*, pp. 444–506, San Francisco, Calif, USA, February 2003.

[7] J. Crols and M. S. J. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1483–1492, 1995.

[8] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, 2001.

[9] M. Dawkins, A. P. Burdett, and N. Cowley, "A single-chip tuner for DVB-T," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1307–1317, 2003.

[10] D. Saias, F. Montaudon, E. Andre, et al., "A 0.12um CMOS DVB-T tuner," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers (ISSCC '05)*, pp. 430–431, San Francisco, Calif, USA, February 2005.

[11] S. Azuma, H. Kawamura, S. Kawama, et al., "A digital terrestrial television (ISDB-T) tuner for mobile applications," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers (ISSCC '04)*, vol. 1, pp. 278–279, San Francisco, Calif, USA, February 2004.

[12] B. Razavi, *RF Microelectronics*, Prentice-Hall PTR, Englewood Cliffs, NJ, USA, 1997.

[13] H. Ma, S. J. Fang, F. Lin, and H. Nakamura, "Novel active differential phase splitters in RFIC for wireless applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, part 2, pp. 2597–2603, 1998.

[14] M. S. J. Steyaert, J. Janssens, B. De Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular transceiver front-end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1895–1907, 2000.

[15] C.-Y. Chou and C.-Y. Wu, "The design of wideband and low-power CMOS active polyphase filter and its application in RF double-quadrature receivers," *IEEE Transactions on Circuits and Systems I*, vol. 52, no. 5, pp. 825–833, 2005.

[16] J. Crols and M. S. J. Steyaert, "A 1.5 GHz highly linear CMOS downconversion mixer," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 7, pp. 736–742, 1995.

[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Higher Education, New York, NY, USA, International edition, 2001.

[18] A. N. Mohieldin, E. Sánchez-Sinencio, and J. Silva-Martinez, "A 2.7-V 1.8-GHz fourth-order tunable LC bandpass filter based on emulation of magnetically coupled resonators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1172–1181, 2003.