

Research Article

Figure-of-Merit-Based Area-Constrained Design of Differential Amplifiers

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A new methodology based on the concept of figure of merit under area constraints is described for designing optimum performance differential amplifiers. First a figure of merit is introduced that includes the three performance parameters, namely, input-referred noise, differential dc gain, and unity-gain bandwidth. Expressions for these parameters have been derived analytically and finally arrived at an expression for the figure of merit. Next it is shown how these performance parameters vary with the relative allocation of the total available area between the input and load transistors. The figure of merit peaks at a certain value of relative area allocation in the range of 60% to 80% of the available area to the input transistors. The peak value of figure of merit is a function of area. However, it is independent of biasing current (and, therefore, power consumption) subject to the minimum current (and, therefore, a minimum power) required to keep all the transistors biased in the saturation region. The peak figure of merit and minimum power required to achieve the peak figure of merit are also plotted as a function of area. These analyses help in synthesizing optimal differential amplifier circuit designs under area constraints.

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1. INTRODUCTION

The first stage of an operational amplifier and several types of comparators is typically a differential amplifier that needs to provide sufficient gain and bandwidth while introducing as little noise as possible. Moreover, if this is desired with a constraint on area, the problem becomes more difficult. The classical noise optimization techniques for low noise amplifier (LNA) design presume a device given with fixed characteristics, and thus offer no explicit guidance on how to best exercise the IC designer's freedom in tailoring device geometries under the constraints of area [1].

2. CONCEPT OF FIGURE OF MERIT

To compare different solutions for an analog circuit design, first a figure of merit must be agreed upon. One of the key issues is the design of a circuit with maximal figure of merit under constraints of area. Here, a figure of merit has been proposed that takes into account the three key perfor-

mance parameters, that is, the differential dc gain, unity-gain bandwidth, and input-referred noise. The proposed figure of merit in this paper is given by

$$\text{FoM} = \frac{\text{UGB} * \text{Ad}}{\text{IRN}}, \quad (1)$$

where UGB is the unity-gain bandwidth, Ad is the differential dc gain, and IRN is the peak input-referred noise spectral density; the differential amplifier is illustrated in Figure 1.

3. PERFORMANCE PARAMETERS

3.1. Noise model for MOST

Each semiconductor device in the circuit introduces noise. Various types of noises that could be possible in a device are shot, thermal, flicker ($1/f$), avalanche, burst, and so forth.

At low frequencies, flicker ($1/f$) noise dominates all other noises. Therefore, here only flicker noise has been considered to introduce the concept developed.

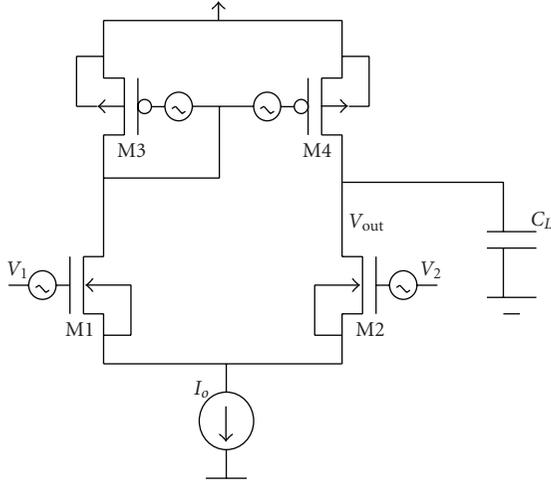


FIGURE 1: Differential amplifier.

There exist numerous models for flicker noise in the MOS transistor [2–10]. In accordance with the most popular model [10], the flicker noise due to a MOS transistor can be lumped as a voltage source at the gate and is given by

$$\overline{V_{eq}^2} = \frac{K_F}{C_{OX} \cdot W_{eff} \cdot L_{eff}} \cdot \frac{\Delta f}{f}, \quad (2)$$

in the noise bandwidth of Δf at frequency f . W_{eff} and L_{eff} are the effective width and length of the gate of the MOS transistor, K_F is the flicker noise coefficient for the MOS transistor, and C_{OX} is the gate capacitance per unit area.

However, the overall circuit noise depends on the circuit configuration.

3.2. Input-referred noise

For the differential amplifier shown in Figure 1, there are four voltage noise sources connected at the gate of each transistor. If all these sources are lumped together at the gate of transistor M1, the mean-square value of the equivalent noise voltage source at input (gate of M1) for the total circuit noise is given by

$$\overline{V_{eqT}^2} = \overline{V_{eq1}^2} + \overline{V_{eq2}^2} + \left(\frac{g_{ml}}{g_{mi}}\right)^2 \cdot (\overline{V_{eq3}^2} + \overline{V_{eq4}^2}), \quad (3)$$

where $\overline{V_{eq1}^2}$, $\overline{V_{eq2}^2}$, $\overline{V_{eq3}^2}$, $\overline{V_{eq4}^2}$ are the noise sources at the gates of transistors M1, M2, M3, and M4. g_{mi} and g_{ml} are the transconductance of the input (M1 and M2) and load (M3 and M4) transistors, respectively, and are given by

$$g_{mi} = \sqrt{2 \cdot k_n \cdot \left(\frac{W_i}{L_i}\right) \cdot \left(\frac{I_o}{2}\right)}, \quad (4)$$

$$g_{ml} = \sqrt{2 \cdot k_p \cdot \left(\frac{W_l}{L_l}\right) \cdot \left(\frac{I_o}{2}\right)},$$

where W_i , W_l , L_i , and L_l are the widths and lengths of input and load transistors, respectively, k_n and k_p are the process

transconductance parameters for n -channel and p -channel MOS transistors, and I_o is the tail current of the differential amplifier.

Using (2), (3), and (4), the power spectral density of noise at the gate of M1 is written as

$$S_{VG}^2 = \frac{\overline{V_{eqT}^2}}{\Delta f} = \frac{2 \cdot K_{Fn}}{C_{OX} \cdot W_i \cdot L_i \cdot f} \cdot \left[1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right]. \quad (5)$$

Therefore, root-mean-square value of spectral power density better known as input-referred noise at frequency f is written as

$$IRN = \sqrt{\frac{2 \cdot K_{Fn}}{C_{OX} \cdot W_i \cdot L_i \cdot f} \cdot \left[1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right]}. \quad (6)$$

3.3. Unity-gain bandwidth

Unity-gain bandwidth of the circuit, UGB, is given by

$$UGB = \frac{g_{mi}}{2 \cdot \pi \cdot C_L} = \frac{1}{2 \cdot \pi \cdot C_L} \sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}}, \quad (7)$$

as C_L is the total load capacitance at the output node.

3.4. Differential dc gain

The differential dc gain, A_d , of the differential amplifier is given by

$$A_d = \frac{g_{mi}}{g_{di} + g_{dl}} = 20 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i} + \frac{1}{2 \cdot L_l}\right)^{-1}, \quad (8)$$

where g_{di} and g_{dl} are the drain to source conductance of input and load transistors, respectively. The drain to source conductance g_d is approximated as

$$g_d = \frac{I_o}{2 \cdot L} \cdot \left(\frac{dx_d}{dV_{DS}}\right), \quad (9)$$

where (dx_d/dV_{DS}) (known as channel-length modulation parameter) is a process parameter [11], and its value has been taken as $0.1 \mu\text{m}/\text{V}$ for NMOS and $0.05 \mu\text{m}/\text{V}$ for PMOS transistors.

3.5. Figure of merit

Substituting the values of UGB, A_d , and IRN from (6), (7), and (8) in (1), we get the following:

$$FoM = \frac{5\sqrt{2} \cdot \mu_n \cdot C_{OX}^{3/2} \cdot W_i^{3/2} \cdot L_i^{3/2}}{\pi \cdot C_L \cdot \sqrt{K_{Fn}} \cdot (1/f)} \cdot \frac{1}{L_i} \cdot \left(1 + \frac{L_i}{2 \cdot L_l}\right)^{-1} \cdot \left(1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right)^{-1/2}. \quad (10)$$

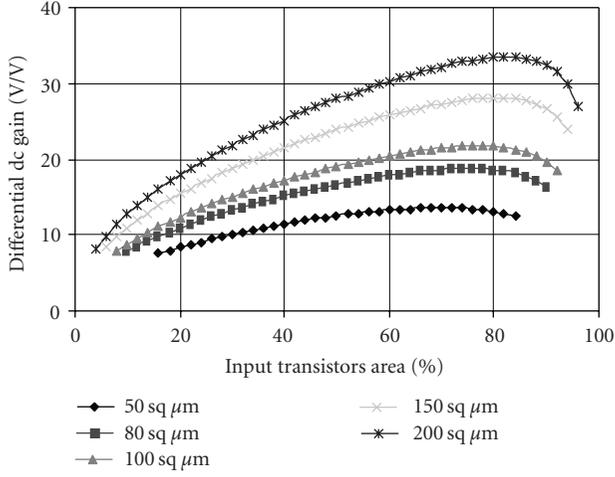


FIGURE 2: The differential dc gain as a function of input transistor area.

4. MAXIMIZATION OF FIGURE OF MERIT UNDER AREA CONSTRAINTS

If A is the total area available for the devices in the differential amplifier, then let us assign $x\%$ of A , that is, $x \cdot A$ to the input transistors and $(1-x) \cdot A$ to load transistors. Then, writing the expressions for UGB, A_d , and peak IRN (at $f = 1$) in terms of x , area (A), bias current (I_o), and technology parameters, we get

$$\begin{aligned}
 A_d &= 20 \cdot \sqrt{\frac{k_n \cdot (x \cdot A)}{I_o}} \cdot \left(1 + \frac{L_i}{2 \cdot L_l}\right)^{-1}, \\
 \text{UGB} &= \frac{\sqrt{k_n \cdot I_o \cdot (x \cdot A)}}{2 \cdot \sqrt{2} \cdot \pi \cdot C_L} \cdot \frac{1}{L_i}, \\
 \text{IRN} &= \sqrt{\frac{4 \cdot K_{Fn}}{C_{OX} \cdot (x \cdot A)}} \cdot \left[1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right].
 \end{aligned} \tag{11}$$

Hence, from (1) and (11) figure of merit (FoM) in terms of x , area (A), bias current (I_o), and technology parameters is written as

$$\begin{aligned}
 \text{FoM} &= \frac{5 \cdot \sqrt{2} \cdot k_n \cdot C_{OX}^{1/2} \cdot (x \cdot A)^{3/2}}{\pi \cdot C_L \cdot K_{Fn}^{1/2}} \cdot \frac{1}{L_i} \\
 &\cdot \left(1 + \frac{L_i}{2 \cdot L_l}\right)^{-1} \cdot \left(1 + \frac{k_p \cdot K_{Fp} \cdot L_i^2}{k_n \cdot K_{Fn} \cdot L_l^2}\right)^{-1/2}.
 \end{aligned} \tag{12}$$

From (12), the following conclusions can be drawn.

- (i) Figure of merit, FoM, is dependent on technology parameters, k_n , k_p , C_{OX} , K_{Fn} , K_{Fp} .
- (ii) It is inversely proportional to the output load C_L .
- (iii) To maximize FoM, length of input transistor L_i should be kept minimum for a given area A , as it maximizes all the three product terms wherever it appears.
- (iv) Figure of merit is independent of the width of load transistor, W_i , hence it should be kept as minimum.

- (v) Length of load transistor L_l should be as large as possible under the constraints of area since it maximizes the last two product terms and hence maximizes figure of merit FoM.

5. ANALYTICAL RESULTS

Figure 2 shows the variation of differential dc gain as a function of relative area allocated to input transistors at different values of total area. It is clear that as the total area increases, the differential dc gain increases. But it does not keep on increasing with the increase in input transistors area. The peak value of dc gain is obtained for x in the range of 0.6 to 0.8. Figure 3 shows that the unity-gain bandwidth is a monotonically increasing function of x .

The variation of peak value of input-referred noise as a function of x is shown in Figure 4. For larger values of x , the noise is reducing because with increasing x , the gate area of input transistors is increasing and their noise contribution is decreasing. But it is interesting to note that it starts increasing beyond a point for all the values of A . It implies that beyond this point, the contribution of noise from load transistors over and above the contribution of input transistors increases. Next the figure of merit is plotted as a function of percent area allocated to input transistors. Figure of merit is a peaking function of x in the range 60% to 80% as shown in Figure 5. It is clear that figure of merit increases with total area A . It also indicates that for a fixed value of total area, about how much percent of total area should be assigned to input transistors to obtain a maximum value of figure of merit. Peak value of figure of merit as a function of total area is plotted in Figure 6. The value of figure of merit is independent of bias current I_o . However, a minimum value of power is essential to keep all the transistors in saturation. Figure 7 shows the minimum bias current required for keeping all the transistors in the circuit in saturation region (and in strong inversion) as a function of total area. It implies that for a given area, a minimum power has to be provided. To increase the figure of merit, area increase alone is not enough; more power is also required to keep the transistors in saturation.

6. SIMULATION RESULTS

Simulations using Tanner Tools Pro also validated the analytical results. To perform this task, a value of total area was chosen. The total area was divided between input and load transistors in a predefined ratio. Then, for this distribution of areas, all combinations of aspect ratio of input and load transistors were simulated to obtain the differential dc gain, unity-gain bandwidth, and peak value of input-referred noise. The figure of merit was computed from these parameters. The peak figure of merit as a function of input transistor area in percent (ratio of area allocated to input transistors to the total available area A) for various values of total area is plotted as shown in Figure 8. This plot matches well with the analytical results shown in the previous section.

TABLE 1: Comparison between analytical and simulated performances at peak figure of merit.

Area (μm^2)	Peak figure of merit (in $\times 10^{12} \text{ Hz}^{3/2}/\text{V}$)		Ad%		UGB%		IRN%	
	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
50	325.44	369.47	98.05	94.55	96.36	95.06	100.16	100
80	787.86	594.21	98.23	95.25	95.45	92.68	100	100
100	1179.8	723.55	98.11	99.56	95.55	94.84	100	100
150	2405.63	1091.78	98.71	98.92	95.65	91.2	100.13	100
200	3938.29	1397.69	98.66	94.24	95.74	81.85	100.16	100

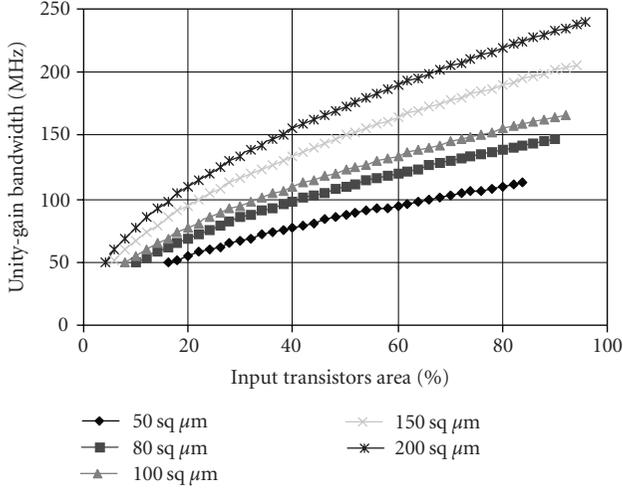


FIGURE 3: Unity-gain bandwidth (in MHz) as a function of input transistor area.

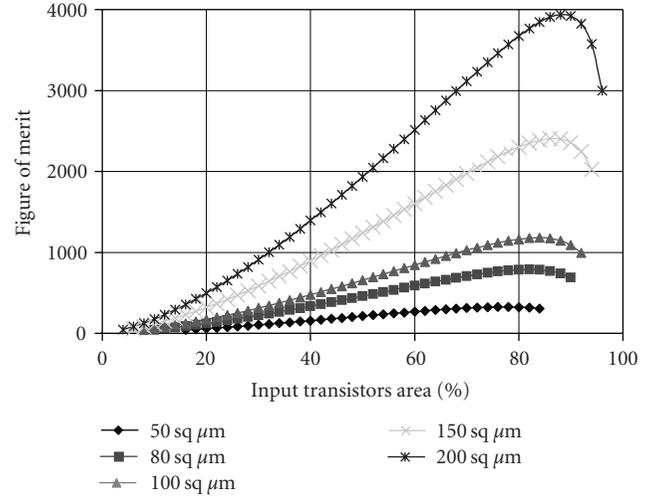
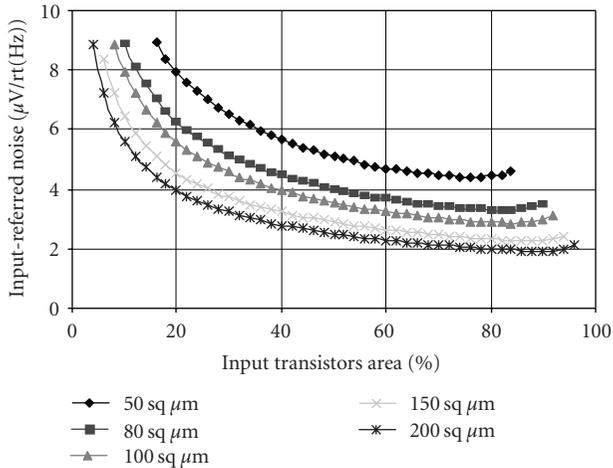
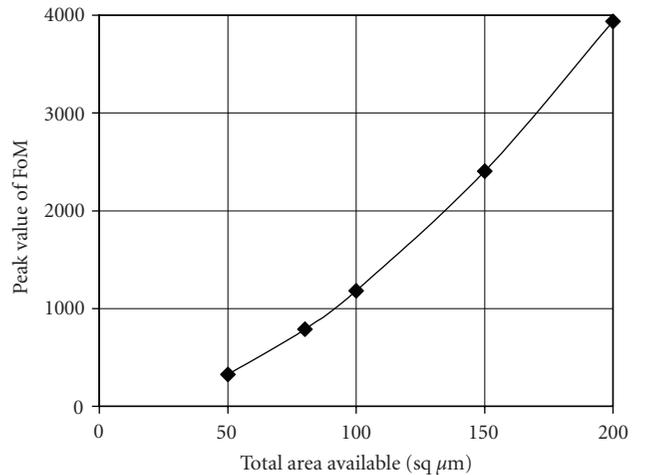
FIGURE 5: The figure of merit, FoM, (in $\times 10^{12} \text{ Hz}^{3/2}/\text{V}$) as a function of input transistor area.FIGURE 4: Input-referred noise (in $\mu\text{V}/\text{rt}(\text{Hz})$) as a function of input transistor area.

FIGURE 6: Peak value of figure of merit, FoM, as a function of area.

In order to demonstrate the utility of figure of merit as a tool to optimize the design, we define three new parameters as follows:

Ad% is the differential dc gain at peak figure of merit as a percentage of maximum differential dc gain achievable for a given area;

UGB% is unity-gain bandwidth at peak figure of merit as a percentage of maximum unity-gain bandwidth achievable for a given area;

IRN% is input-referred noise at peak figure of merit as a percentage of minimum input-referred noise achievable for a given area.

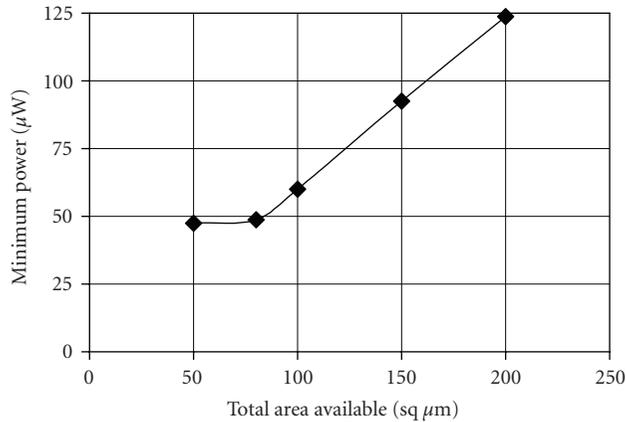


FIGURE 7: Minimum power desired as a function of total area.

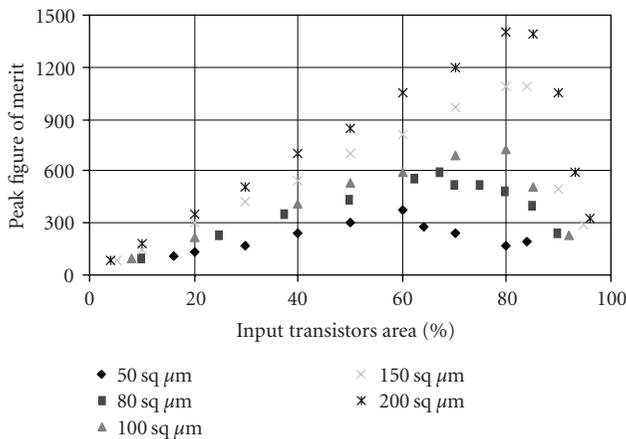


FIGURE 8: Simulated plot of figure of merit, FoM, (in $\times 10^{12} \text{ Hz}^{3/2}/V$) as a function of input transistor area.

Table 1 compares the analytical and simulated values of peak figure of merit, Ad%, UGB%, and IRN% for constant area. In most cases, value of Ad% is more than 95%, and the value of UGB% is more than 91%. IRN% is less than 101% in all cases.

7. CONCLUSION

The concept of figure of merit is a suitable tool for synthesizing optimal design of differential amplifiers under area constraints and leads to the realization of differential dc gain, unity-gain bandwidth, and input-referred noise values that are also very close to their individually achievable maximum values under the same area constraints. The above analyses validate that the idea of FoM may be deployed in a CAD tool for automatically synthesizing the differential amplifiers and can be extended for many other building blocks for low frequency applications. The paper also highlights the dependence of peak figure of merit and the minimum power required to achieve it on the area available for the circuit.

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