

## Review Article

# Recent Advances on the Design of High-Gain Wideband Operational Transconductance Amplifiers

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Feed-forward techniques are explored for the design of high-frequency Operational Transconductance Amplifiers (OTAs). For single-stage amplifiers, a recycling folded-cascode OTA presents twice the GBW (197.2 MHz versus 106.3 MHz) and more than twice the slew rate (231.1 V/ $\mu$ s versus 99.3 V/ $\mu$ s) as a conventional folded cascode OTA for the same load, power consumption, and transistor dimensions. It is demonstrated that the efficiency of the recycling folded-cascode is equivalent to that of a telescopic OTA. As for multistage amplifiers, a No-Capacitor Feed-Forward (NCFF) compensation scheme which uses a high-frequency pole-zero doublet to obtain greater than 90 dB DC gain, GBW of 325 MHz and better than 70° phase margin is discussed. The settling-time- of the NCFF topology can be faster than that of OTAs with Miller compensation. Experimental results for the recycling folded-cascode OTA fabricated in TSMC 0.18  $\mu$ m CMOS, and results of the NCFF demonstrate the efficiency and feasibility of the feed-forward schemes.

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## 1. Introduction

The growing demand for high-speed and high-precision analog ICs dictates stringent design specifications for the amplifiers which are the basic building blocks for numerous applications; IF switched-capacitor (SC) filters and high-resolution data converters with sampling frequencies above 100 MHz require very fast OTAs with settling times less than 4 nanoseconds for good performance [1–24]. High-gain amplifiers use cascode structures or multistage designs with long channel length transistors biased at low current levels while high-bandwidth amplifiers use single-stage designs with short channel length transistors biased at high current levels.

For single-stage amplifiers, the folded-cascode (FC) OTA has a higher signal swing than a telescopic OTA while still presenting a single parasitic pole and relatively large DC gain, and hence it is commonly used for high-frequency applications [5, 7–18]. For such applications the typical FC structure presents some limitations. PMOS drivers are predominately used for their lower flicker noise and higher frequency parasitic pole, but the bandwidth is limited

because of the lower carrier mobility in PMOS devices. If NMOS drivers are used, the settling behavior suffers because of the lower-frequency parasitic pole, and in order to extend the bandwidth, several phase compensation schemes have been reported in literature [8–12]. Another limitation of the FC, regardless of driver type, is that the maximum slewing current is roughly half the total OTA current unlike the telescopic OTA which utilizes the total current. It is shown that the recycling folded-cascode (RFC) OTA can alleviate many of the conventional FC limitations; it can settle faster and more accurately, boost slew rate, and improve overall efficiency.

In multistage amplifiers, cascading of individual gain stages increases the overall amplifier gain, but each stage introduces a low frequency pole, which produces a negative phase shift and degrades the phase margin. Many phase compensation schemes for multi-stage amplifiers have been reported in literature [6, 7, 19–24]. Most of these are variations of the basic Miller compensation scheme for a two-stage amplifier. The NCFF compensation scheme employs a feed-forward path to create LHP zeros but does not use any Miller capacitor [25]. This topology results in

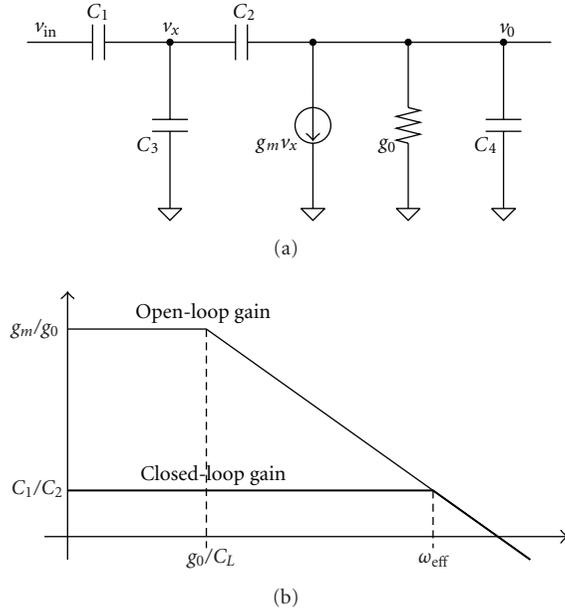


FIGURE 1: Typical OTA-based capacitor amplifier: (a) schematic and (b) typical open and closed loop magnitude response.

a higher-gain-bandwidth product (GBW) with a fast step response.

The theoretical aspects of feed-forward techniques are discussed in Section 2. Section 3 deals with feed-forward techniques associated with the FC OTA and introduces the RFC. A design case study in Section 4 compares several OTA aspects of the FC and RFC. High-gain two-stage amplifiers without Miller compensation are considered in Section 5. Section 6 describes the circuit simulation and experimental results, and the conclusions are drawn in Section 7.

## 2. Settling-Time in the Presence of a Pole-Zero Pair

A macromodel of the capacitive amplifier used in switched-capacitor circuits is shown in Figure 1(a). By using conventional circuit analysis techniques, the small signal transfer function can be calculated and is given by

$$\frac{v_o(s)}{v_{in}(s)} \cong - \left( \frac{1 - sC_2/g_m}{1 + s(C_4 + \beta(C_1 + C_3))/\beta g_m} \right) \left( \frac{C_1/C_2}{1 + 1/\beta A_v} \right), \quad (1)$$

where  $A_v = g_m/g_o$  and  $\beta = C_2/(C_1 + C_2 + C_3)$  are the amplifier open-loop DC gain and the feedback factor, respectively. A typical open and closed loop magnitude response is depicted in Figure 1(b). The location of the pole is given by

$$\omega_{peff} = \frac{\beta g_m}{C_4 + \beta(C_1 + C_3)} = \frac{\beta g_m}{C_L}, \quad (2)$$

where  $C_L (= C_4 + \beta(C_1 + C_3))$  is the effective loading capacitor. The typical step response of the critically/over-damped capacitive amplifier is shown in Figure 2. It consists

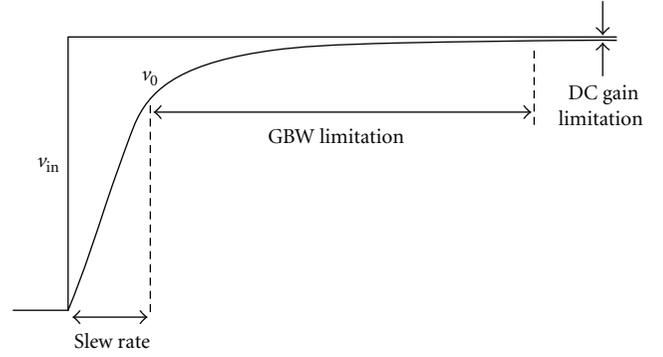


FIGURE 2: Step response of a unity gain amplifier with enough phase margin.

of two phases: the first is limited by the slew rate and the second by the closed loop bandwidth. The error in the final value is determined by the factor  $1/(\beta A_v)$  as can be seen in (1).

Single-stage OTA slew rate (SR) is determined by the amount of current that can be delivered to or extracted from the output and the effective load capacitor ( $SR = I/C_L$ ). The bandwidth limited phase is determined by both the effective pole's frequency  $\omega_{peff}$  and phase margin, and in many practical low-voltage cases dominates the overall settling time. If the slew rate and the RHP zero effects are ignored, the closed-loop pulse response of the amplifier is given by (3), where  $\alpha = C_1/C_2$  is the ideal amplifier's gain:

$$v_o(t) = v_o(t_0) - \left( \frac{1 - e^{-\omega_{peff}t}}{1 + 1/\beta A_v} \right) \alpha v_i(t). \quad (3)$$

A high-performance amplifier should have a high  $\omega_{peff}$  for fast settling and a high DC gain  $A_v$  for final value precision. The analysis of the amplifier impulse response in the presence of a pole-zero doublet is more complex; in [26–28] it was shown that the presence of low-frequency pole-zero pairs may generate slow components that reduces significantly the amplifier's speed. This is not the case if high-frequency pole-zero doublets are present. In order to consider the effects of high-frequency pole-zero pairs, the overall open-loop transconductance of the amplifier can be simplified as

$$G_m(s) = \left( \frac{1 + s/\omega_z}{1 + s/\omega_p} \right) g_m. \quad (4)$$

If the right-hand side zero  $g_m/C_2$  is ignored, using (1) and (4), the closed-loop transfer function is obtained as

$$\frac{v_o(s)}{v_{in}(s)} \cong - \left( \frac{1 + s/\omega_z}{\mathfrak{Q} + (1/\omega_p)(1/\omega_{peff})s^2} \right) \cdot \left( \frac{C_1/C_2}{1 + 1/\beta A_v} \right), \quad (5)$$

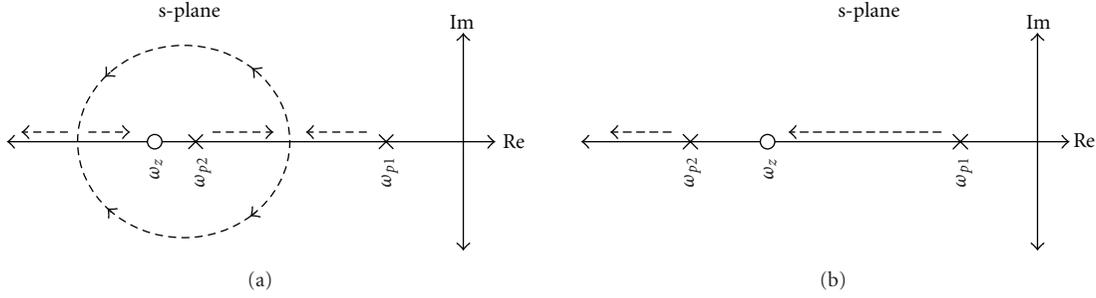


FIGURE 3: Typical root locus for a system with two poles and 1 zero: (a) zero is located at high frequencies, and (b) zero is located between the poles. In both cases the dominant pole is terminated by the zero.

where  $\mathfrak{A}$  denotes  $1 + (1/\omega_z + 1/\omega_{\text{Peff}} + g_0/\beta g_m \omega_p)s$ , and  $\omega_{\text{Peff}}$  is defined by (2). According to (5), the closed-loop poles are located at

$$\begin{aligned} \omega_{p1,2} &\cong -\frac{\omega_p \left(1 + \omega_{\text{Peff}}/\omega_z + (g_0/C_L)(1/\omega_p)\right)}{2} \\ &\times \left(1 \pm \sqrt{1 - 4 \frac{\omega_{\text{Peff}}/\omega_p}{\left(1 + \omega_{\text{Peff}}/\omega_z + (g_0/C_L)(1/\omega_p)\right)^2}}\right). \end{aligned} \quad (6)$$

For real poles, both poles are located above and below  $(\omega_p(1 + \omega_{\text{Peff}}/\omega_z) + g_0/C_L)/2$ . If the poles are complex conjugate, the magnitude of the real part is above  $\omega_p/2$ . Notice that the zero reduces the imaginary part of the poles. Figure 3 shows the typical root locus of a 2-pole and 1-zero system. In both cases, the lowest-frequency pole is close to the frequency of the zero if enough feedback is used. A common case for the feed-forward amplifiers to be discussed in the following sections is shown in Figure 4, which corresponds to the root-locus shown in Figure 3(a). Both open-loop and closed-loop gains are depicted. Notice in this figure that the closed-loop pole-zero doublet appears close to the open-loop zero's frequency if enough feedback factor is present. The closed-loop amplifier's impulse response (assuming that  $\omega_{p1} \neq \omega_{p2}$ ) is given by

$$\begin{aligned} h(t) &= -\left(\frac{C_1/C_2}{1 + 1/\beta A_V}\right) \\ &\times \left(\frac{(\omega_{p1}\omega_{p2})\left((\omega_{p1} - \omega_z)e^{-\omega_{p1}t} + (\omega_z - \omega_{p2})e^{-\omega_{p2}t}\right)}{(\omega_{p1} - \omega_{p2})\omega_z}\right). \end{aligned} \quad (7)$$

Slow output components caused by pole-zero spacing are avoided if both closed-loop poles  $\omega_{p1}$  and  $\omega_{p2}$  are placed at high frequencies to guarantee small time constants; this is possible if and only if the zero is located at high frequencies, which directly impacts the location of  $\omega_{p1}$  and  $\omega_{p2}$  as seen

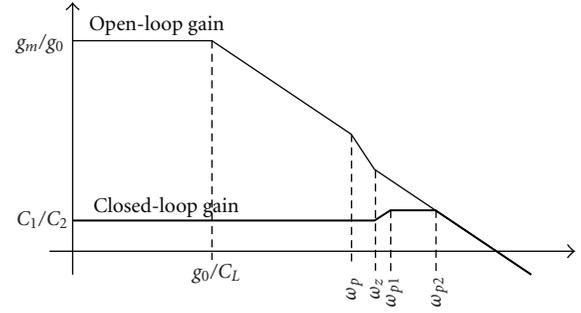


FIGURE 4: Open and closed loop transfer function of a second-order system in presence of a zero. The zero is located after the open-loop poles.

in (6). An important observation here is that if the closed-loop dominant pole is close to the location of the zero, its coefficient (proportional to  $\omega_{p1} - \omega_z$ ) is reduced thereby reducing the effect of possible slow components.

### 3. Feed-Forward Techniques for Folded-Cascode OTAs

The typical FC OTA is shown in Figure 5 [7]. Its small-signal transconductance gain is approximately given by (8), where  $g_{m1}$  is the small-signal transconductance of  $M1$ , and  $C_N$  is the capacitance associated with the source of  $M5$ :

$$G_{mFC} \cong \frac{g_{m1}}{1 + s(C_N/g_{m5})}. \quad (8)$$

The transconductance of the cascode transistors and the equivalent parasitic capacitor  $C_N$  at that node determine the open-loop pole's frequency. For wide band applications, a large unity gain frequency is needed, and therefore the frequency of the parasitic pole  $\omega_p (= g_{m3}/C_N)$  must be as high as possible. PMOS drivers are preferred for FC amplifiers since the parasitic pole of the folding node is then associated with NMOS cascode devices and is located at a higher frequency. When reducing the widths of the cascode transistors, the benefit of increasing the frequency of the parasitic pole might be limited because the saturation voltage must be maintained within the limits dictated by the supply voltages and signal swing. Mobility degradation due

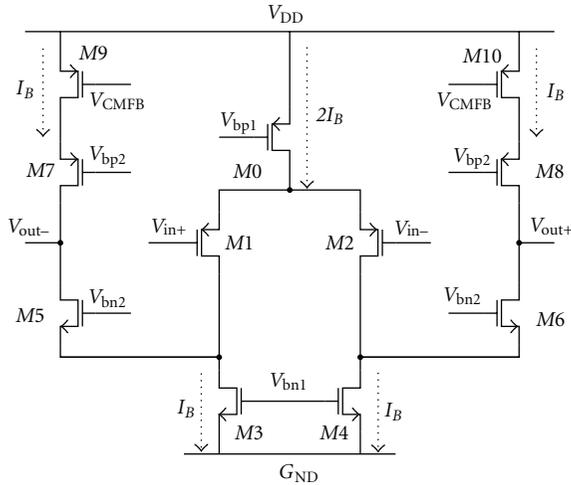


FIGURE 5: Typical folded-cascode OTA.

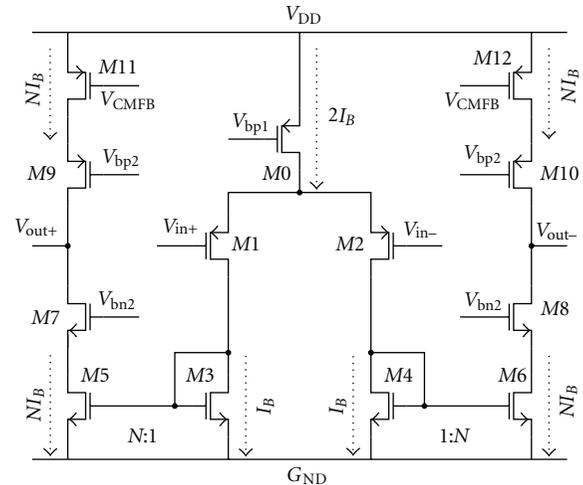


FIGURE 7: Current mirror OTA with cascode output stage.

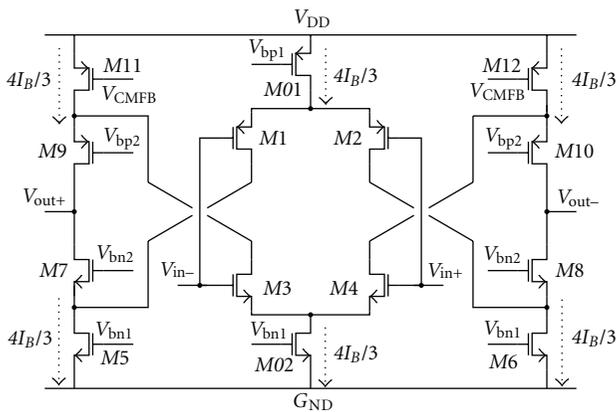


FIGURE 6: Folded-cascode OTA using complementary differential pairs.

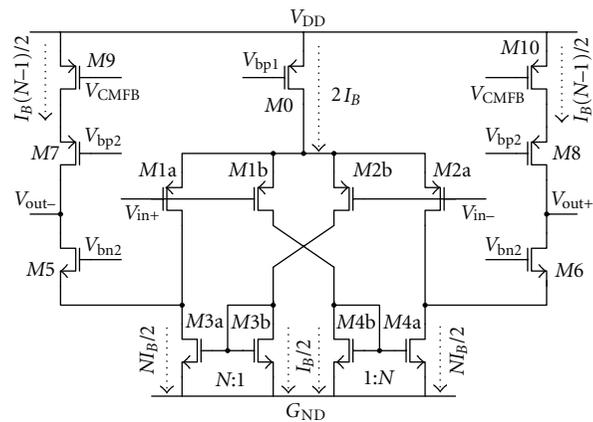


FIGURE 8: Recycling folded-cascode amplifier.

to vertical electrical field becomes more critical in that case as well. Reducing the length of the cascode transistors reduces  $V_{DSAT}$  and increases  $\omega_p$ ; the drawback is the reduction of the OTA DC gain. Increasing the bias current also increases the frequency of the parasitic poles, but the DC gain reduces, and the power consumption increases. Moreover, the choice of PMOS drivers is on the expense of a larger input capacitance for the same  $g_m$  if NMOS drivers were used. Ideally, an OTA should use NMOS transistors for both differential pair and cascode devices, such that both the small signal transconductance and phase margin are increased. This is the major advantage of the telescopic structure [13, 14], but its output swing is limited, especially for low-voltage applications and if low  $V_T$  transistors are not available.

To overcome some of these tradeoffs, a number of feed-forward compensation techniques have been reported [5, 8–12]. The technique proposed in [9] uses RC networks connected to the gate of the cascode transistors; hence a zero is introduced such that the parasitic pole is partially compensated. In the technique proposed in [10], the low-frequency

signal flows throughout the PMOS cascode transistors, and, by using RC networks, the high-frequency signal flows throughout the NMOS cascode transistors. Due to the higher mobility of the NMOS devices, better performances can theoretically be achieved. The additional networks, however, increase silicon area and the capacitance of the parasitic nodes, thus reducing the frequency of the poles; a medium-frequency pole-zero pair may increase amplifier's settling time. In [11], the gate of the cascode transistor is directly connected to the input signals. By using that feed-forward scheme, further improvements in the OTA phase margin are obtained due to the presence of a high-frequency zero. A major drawback of this technique, however, is that the gate-drain capacitors of the cascode transistors affect the precision of the system, especially for SC circuits. This drawback has been partially solved by using cross-coupled capacitors [12].

Complementary differential pairs have been used for a long time in the design of rail-to-rail amplifiers [16]. They can also be used for fast amplifiers [17], where all cascode transistors can be exploited as shown in Figure 6. It

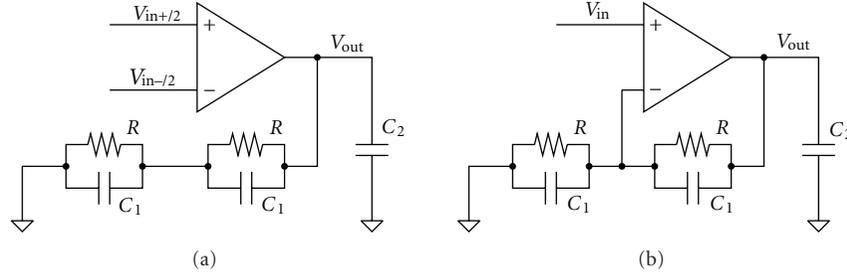


FIGURE 9: Amplifier characterization setup: (a) AC response and noise and (b) transient response.

can be shown that the small-signal transconductance of the complementary OTA is given by

$$Gm_{CFC}(s) \cong \frac{1+s(C_P/g_{m9})(\mathfrak{P}/g_{m1}+g_{m3})}{(1+s(C_P/g_{m9}))(1+s(C_N/g_{m7}))}(g_{m1}+g_{m3}), \quad (9)$$

where  $\mathfrak{P}$  denotes  $g_{m3}(g_{m9}/g_{m7})(C_N/C_P)$ , and  $C_N$  and  $C_P$  are the parasitic capacitors lumped to the source of transistors  $M7$  and  $M9$ , respectively. According to this result, if the poles at the source of  $M7$  and  $M9$  are placed at the same frequency, the overall small signal transconductance becomes  $Gm(0) = g_{m1} + g_{m2}$  with a single pole located at  $\omega = g_{m7}/C_N = g_{m9}/C_P$ . In general, two signal paths generate poles located at different frequencies, leading to the so-called “phantom zero”; this term is used because there is not a physical element generating the zero, but this is a result of the addition of signal components with slightly phase difference.

The overall current consumption is  $4I_B$ , same as the FC OTA previously discussed. For same overall current and same input capacitance, its small signal transconductance is around 15%–20% more compared to the FC OTA. A downside is the introduction of the parasitic pole associated with the PMOS cascode transistor. Moreover, the addition of the signal paths generates a zero at a lower frequency than the pole associated with the NMOS cascode devices. Also, the input common mode range where the transconductance is maximized is limited. The slew rate, on the other hand, is 33% higher because the sourced/sunk current can be as high as  $4I_B/3$ .

The current-mirror cascode OTA shown in Figure 7 has a non dominant pole at gate of  $M3$  in addition to the pole of the cascode transistor  $M7$ . The overall small signal transconductance is given by (10), where  $g_{m3(7)}$  is the transconductance of transistor  $M3(M7)$ ,  $C_{N1}$  ( $= C_{GS3}(1 + N)$ ) is the capacitance associated with the gate of  $M3$ ,  $C_{N2}$  is the capacitance associated with the source of the cascode device  $M7$ , and  $N = g_{m5}/g_{m3}$ .

$$Gm_{CM} = \frac{Ng_{m1}}{(1+s(C_{N1}/g_{m3}))(1+s(C_{N2}/g_{m7}))}. \quad (10)$$

The current-mirror cascode OTA suffers from a similar limitation as the FC OTA; during negative slewing, only half of the drain current of  $M5$  is employed in discharging the load capacitance because the DC current provided by  $M11$  cancels the other half. However, a larger fraction of the

overall current used can be transferred to the load if  $N > 1$ . With a current gain greater than 1 in the current mirror, the size of the input transistors can be reduced for same GBW as the FC OTA. Although this decreases the input capacitance, the parasitic capacitance at the gate of  $M3$  increases, which pushes the non dominant pole to lower frequencies. Also, for the same power consumption,  $N > 1$  increases the current levels at the output stage thereby lowering the OTA’s DC gain. Nonetheless, if the current-mirror OTA is designed with sufficient phase margin, it may settle faster than the FC OTA because of its enhanced slew rate and smaller input capacitance.

A recycling folded-cascode (RFC) OTA built by the combination of the conventional FC and the current-mirror OTAs is depicted in Figure 8 [18]. This architecture shares all the benefits of the two OTAs from which it is created, but without sharing their limitations. It is named the recycling folded-cascode as it reconfigures the same devices of an FC and reuses previously idle current in the signal path with virtually no increase in silicon area. In the FC OTA of Figure 5, the NMOS transistors  $M3$  and  $M4$  conduct the most current yet act as current sinks only. The modifications present in Figure 8 are intended to use  $M3$  and  $M4$  as driving transistors. First the original drivers,  $M1$  and  $M2$  (Figure 5), are split in half to produce transistors  $M1a,b$  and  $M2a,b$  (Figure 8). Each pair of  $M1a,b$  and  $M2a,b$  in Figure 8 is driven by the same input, and thus the input capacitance remains the same as that of the original FC. Next,  $M3$  and  $M4$  (Figure 5) are split with a  $1:N$  ratio, and the diode connected  $M3b$  and  $M4b$  (Figure 8) are used to create an inversion and drive  $M3a$  and  $M4a$ , such that the small signal currents added at the sources of  $M5$  and  $M6$  are in phase. To keep the same current consumption as the original FC and simplify the forthcoming analysis,  $N$  is equal to 3.

Now it can be shown that the transconductance of the RFC is given by (11), where  $g_{m1}$  is the same as that of the original FC ( $g_{m1} = 2g_{m1a}$ ), and  $C_N$  is the lumped capacitance at the source of  $M5$ . By applying the value of  $N = 3$ , the low-frequency transconductance of the RFC is found to be twice that of the original FC for the same power consumption. When compared to the current-mirror OTA, the increase in the RFC transconductance was not on the expense of increasing the output current and reducing the output impedance. As far as bandwidth is concerned, the input signal follows two paths to the output:  $M2b$ – $M3b$ – $M3a$ – $M5$  creates a current-mirror OTA, while the feed-forward

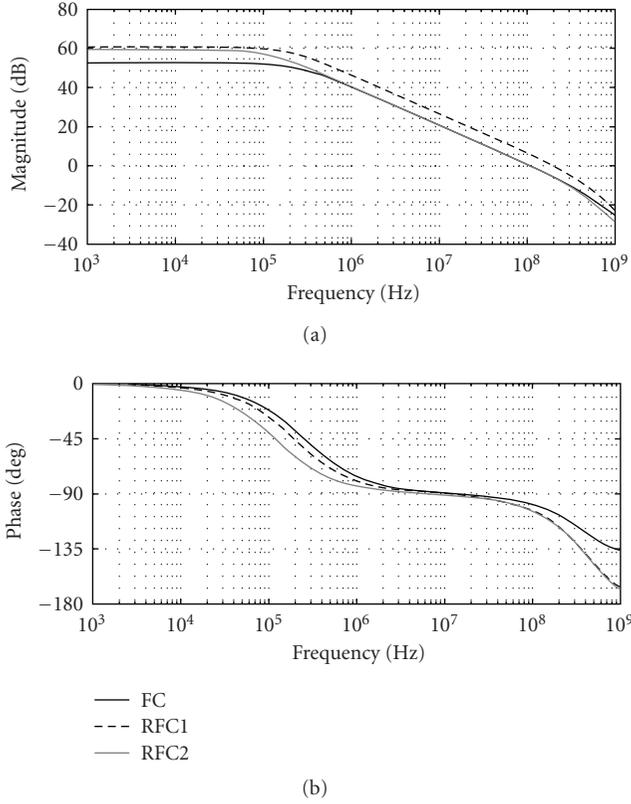


FIGURE 10: Amplifiers AC response: (a) magnitude and (b) phase.

path  $M1a$ – $M5$  creates an FC OTA. Since the signal parts add in phase at the source of  $M5$ , an LHP zero is created by the feed-forward path, which partially compensates the negative phase shift induced by  $\omega_{p1}$ . Since all the poles and zero of the RFC are associated with NMOS devices, they are naturally at high frequencies and will not introduce slow settling components as long as  $N$  is kept moderately small. In fact, the pole-zero pair associated with the current mirrors  $M3a, b$  and  $M4a, b$  can be placed beyond the OTA unity gain frequency,  $\omega_u$ . Suppose that a condition is imposed such that  $\omega_{p1} > 3\omega_u$ , then an upper boundary is placed on  $N$  as described by (12):

$$Gm_{RFC} = \frac{g_{m1}}{2} (1 + N) \frac{(1 + s/\omega_z)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \quad (11)$$

$$\omega_z \cong \frac{g_{m3b}}{C_{GS3b}}, \quad \omega_{p1} \cong \frac{g_{m3b}}{C_{GS3b}(1 + N)}, \quad \omega_{p2} \cong \frac{g_{m5}}{C_N}, \quad (12)$$

$$\omega_{p1} > 3\omega_u \implies N < \sqrt{\frac{g_{m3b}C_L}{3g_{m1a}C_{GS3b}}} - 1.$$

Given the RFC modifications, the slew rate is also improved. Assuming a single-ended load  $C_L$ , the slew rate of the original FC and the current-mirror OTAs is  $2I_B/C_L$  and  $2NI_B/C_L$ , respectively. Now consider the RFC when a large signal is applied at the input. As  $V_{in+}$  approaches  $V_{DD}$ , transistors  $M1a, b$  shut off, which forces transistors  $M4a, b$  and  $M6$  to shut off. Hence the total current available to charge the

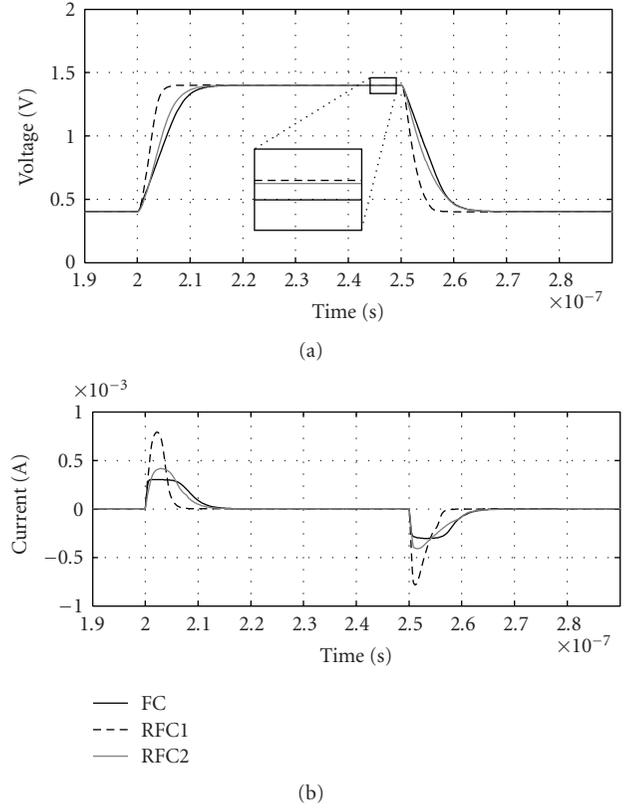


FIGURE 11: OTAs transient response for an output step of 1Vpp: (a) output voltage and (b) output current.

capacitance at  $V_{out+}$  is  $I_B(N - 1)/2$  and is provided by  $M10$ . On the other hand, with  $M4a$  and  $M6$  off,  $M2a$  is pushed into deep triode conducting negligible current and hence all the tail current,  $2I_B$ , is forced to flow through  $M2b$ . This current is in turn mirrored from  $M3b$  to  $M3a$  by a factor of  $N$  ( $= 3$ ). Thus,  $M9$  is sourcing  $I_B(N - 1)/2$  while  $M3a$  is sinking  $2NI_B$ , resulting in the capacitance at  $V_{out-}$  to be discharged by  $I_B(3N + 1)/2$ . This differential imbalance in the charging and discharging of  $V_{out+}$  and  $V_{out-}$  is quickly converted to a common mode error and fixed by the common mode feedback (CMFB), and the result is a maximum symmetrical slew rate of  $2NI_B/C_L$ . While it is clear that the slew rate of the RFC is enhanced over that of the original FC, the same may not be so obvious when it comes to the current-mirror OTA. But, if we consider the same power consumption, the value of  $N$  used in the current-mirror OTA is 1 whereas for the RFC,  $N$  is 3; the slew rate is also enhanced over that of the current-mirror OTA. In the design of any OTA however, the slew rate will be restricted by the size and biasing conditions of the devices in the signal path, which will limit the slew rate to a smaller value than in theory, especially for low-voltage implementations.

An aspect worth examining is the overall efficiency. If we define efficiency as the ratio of generated small-signal current to total DC current, that is,  $Gm(0)/I_{total}$ , then the efficiencies of the original FC, current-mirror, and RFC OTAs can be given by (13). The RFC is clearly the most efficient OTA.

TABLE 1: Comparison of simulation results for the original folded-cascode and the recycling folded-cascode OTAs.

Parameter	Folded-cascode	RFC1	RFC2
Power [ $\mu\text{A}$ ]	796	782	394
DC gain [dB]	52.63	60.91	59.32
GBW [MHz]	106.3	197.2	105.9
Phase margin [deg]	80.6	62.5	75.1
Total capacitive load [pF]	3.6	3.6	3.6
Slew rate ( $\pm$ average) [ $\text{V}/\mu\text{s}$ ]	99.3	231.1	116.5
Input referred noise (1 Hz-100 MHz) [ $\mu\text{V}_{\text{rms}}$ ]	53.16	48.48	69.71
0.1% settling time [ns]	21.7	11.6	21.7

Although the current-mirror OTA is almost as efficient as the RFC, its increased efficiency comes at the expense of a large  $N$  which drastically affects its  $Gm$  pole locations and limits its bandwidth, whereas the efficiency of the RFC is independent of  $N$ . More importantly, the efficiency of the RFC is the same as that of a telescopic OTA (total telescopic current is  $2I_B$ ), but the RFC has a wider input common mode range and larger output swing:

$$\eta_{FC} = \frac{g_{m1}}{4I_B}, \quad \eta_{CM} = \frac{Ng_{m1}}{2(N+1)I_B}, \quad \eta_{RFC} = \frac{g_{m1}}{2I_B}. \quad (13)$$

#### 4. Folded-Cascode OTA Case Study

This enhanced efficiency of the RFC can be viewed from another angle. If the RFC is able to achieve twice the transconductance and more than twice the slew rate ( $N = 3$ ) of the original FC while using the same power and silicon area, then the RFC must be able to achieve the same transconductance and slew rate as the original FC using significantly less power and silicon area. Indeed, if we take the RFC of Figure 8 and reduce the width of all devices by a factor of 2, it will achieve a similar performance to the original FC, but using only half the power and half the area, which also means half the input capacitance. To demonstrate this, three OTAs were designed in TSMC 0.18  $\mu\text{m}$  CMOS technology with a 1.8V supply: an FC and two RFC OTAs. One of the recycling folded-cascodes, RFC1, uses the same power and area as the FC, while the second, RFC2, uses only half the power and half the area.

The setup in Figure 9 was used to characterize the different OTA aspects. To preserve the high-output impedance of the OTAs and limit the DC output current drawn,  $R$  was set to be 560 k $\Omega$ . As for  $C_1$  and  $C_2$  they were set to 2.2 pF and 2.5 pF, respectively, which yields an overall load of 3.6 pF. As seen in Figure 10, RFC1 indeed has a wider bandwidth, whereas RFC2 has virtually the same bandwidth; this was anticipated according to the analysis in the preceding section. While RFC1 has +6 dB gain due to an enhanced  $Gm$ , RFC2 has +6 dB gain because it consumes half the current; the additional 2–4 dB improvement is attributed to the enhanced output impedance. The gain enhancement seen in  $R_{O_{RFC}}$  is due to the increased  $r_{ds}$  of  $M1a$  and  $M3a$ , as they conduct less current compared to their counterparts  $M1$  and  $M3$  of the FC. Therefore, an overall low-frequency gain enhancement

of 8–10 dB can be seen in the RFC compared to the FC as seen in Figure 10.

The phase response shows some degradation for both RFC1 and RFC2 with respect to the FC. This is to be expected. As discussed earlier, the addition of current mirrors in the signal path ( $M3a, b$ - $M4a, b$ ) introduces a pole-zero pair. However, by satisfying the condition set by (12) for the upper limit of  $N$ , the degradation in the phase margin should not significantly affect the transient response of the amplifiers; here the phase margins of the FC, RFC1 and RFC2 are 80.6°, 62.5°, and 75.1°, respectively. For the transient response shown in Figure 11, the input signal was a 500 mVpp 10 MHz pulse with a common mode level of 450 mV. Undoubtedly, RFC1 has a superior slew rate performance than FC as seen in Figure 11(a). RFC2 too has a better slew rate performance, which is seen more clearly in Figure 11(b) as a higher peak output current. Moreover, the settling behavior of both RFC1 and RFC2 was not affected by the phase margin degradation in comparison to FC.

As for noise, RFC1 shows better performance over the FC. Intuitively, the enhanced transconductance of the RFC1 reduces the noise when referred to the input. This, however, is counteracted by an increased output noise due to contributions by  $M3b$  and  $M4b$ , which actually are amplified by  $N^2$ . Considering that the output current thermal and flicker noise PSD of an MOS device can be expressed as (14), it can be demonstrated that the input referred thermal ( $v_{iT}^2$ ) noise PSD of the FC and RFC1 given by (15) and (16).

$$\overline{i_o^2} = 4k_B T \gamma g_m, \quad (14)$$

$$\overline{v_{iT,FC}^2} = \frac{8k_B T \gamma}{g_{m1}} \left[ 1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}} \right], \quad (15)$$

$$\overline{v_{iT,RFC}^2} = \frac{8k_B T \gamma}{g_{m1a}(1+N)} \left[ \frac{(1+N^2)}{(1+N)} + \frac{g_{m3a}}{g_{m1a}} + \frac{1}{(1+N)} \frac{g_{m9}}{g_{m1a}} \right]. \quad (16)$$

The noise performance improvement of RFC1 ( $N = 3$ ) is hence explained by two smaller terms in (17) compared to their counterpart in (15) for the FC:

$$\overline{v_{iT,RFC}^2} = \frac{8k_B T \gamma}{g_{m1}} \left[ \frac{5}{4} + \frac{3}{4} \frac{g_{m3}}{g_{m1}} + \frac{1}{4} \frac{g_{m9}}{g_{m1}} \right]. \quad (17)$$

A summary of the discussed results is shown in Table 1.

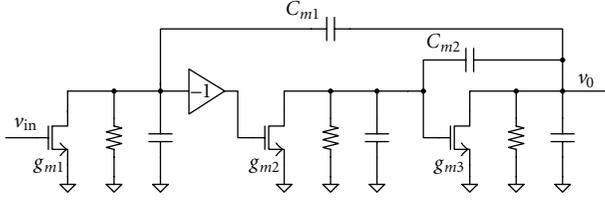


FIGURE 12: Three-stage amplifiers with nested Miller compensation.

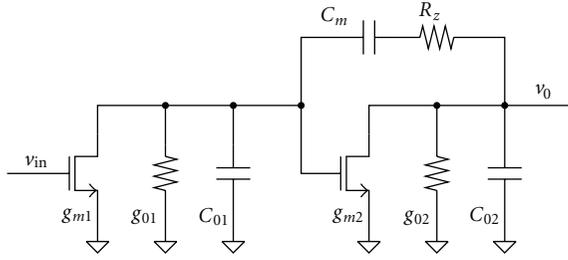


FIGURE 13: Two-stage Miller compensation.

## 5. Multistage OTAs with no Miller Capacitors

Amplifiers with cascaded gain stages are very popular for SC applications as well [6, 19–24]. Several compensation schemes have been reported in literature for multistage amplifiers [22, 23]; one of them is shown in Figure 12. The inverting amplifiers are not needed if differential stages are used. DC gains of 90–100 dB can be achieved. Due to the three high-impedance nodes, double Miller compensation might be required for adequate phase margin. The classic two-stage Miller compensation scheme is shown in Figure 13. The open-loop dominant pole,  $\omega_{p1} \cong g_{01}/A_v 2C_m$ , is pushed to lower frequencies by the increase in effective capacitance formed by the compensation capacitor,  $C_m$ , and the gain of the second stage,  $A_{v2}$ . This decreases the open loop unity gain frequency  $\omega_u$  ( $\sim g_{m1}/C_m$ ) and results in a slower settling time. The nondominant pole is mainly given by  $g_{m2}/(C_{01} + C_{02})$ . For good stability, the condition  $g_{m2}/(C_{01} + C_{02}) > g_{m1}/C_m$  must be satisfied. However, high-frequency SC circuits may require large load capacitors that force a large  $g_{m2}$  and further increase the power consumption and capacitor  $C_{01}$ .

Feed-forward compensation techniques have been used to boost the DC gain of OTAs, especially for low-frequency applications [25], [29]. Figure 14 shows the simplified schematic of the compensation scheme. The NCFE compensation scheme does not employ any compensation capacitor but uses a Left plane (LHP) zero for obtaining good phase response. It can be found that the open-loop small signal transconductance gain is

$$G_m(s) \cong (A_{v1}g_{m2} + g_{m3}) \frac{(1 + s/(g_{m2}/g_{m3})(A_{v1}\omega_p))}{(1 + s/\omega_p)} \quad (18)$$

$$= g_m \frac{(1 + s/\omega_z)}{(1 + s/\omega_p)},$$

where  $A_{v1}$  is the DC gain of the first stage ( $= g_{m1}/g_{01}$ ), and the dominant pole of the first stage is located at  $\omega_p = g_{01}/C_{01}$ . The DC transconductance is approximately given by  $g_m = g_{m1}g_{m2}/g_{01}$ . By using this OTA in the amplifier configuration shown in Figure 1(a), and according to (1), (2), (5), (6), and (25), the closed-loop zero and poles are located at the following frequencies:

$$\omega_z \cong \left( \frac{g_{m2}}{g_{m3}} \right) \left( \frac{g_{m1}}{C_{01}} \right),$$

$$\omega_{p1,2} \cong \left( \frac{g_{m3} + g_{02}}{2C_L} \right) \left( 1 \pm \sqrt{1 - 4 \left( \frac{g_{m1}g_{m2}}{(g_{m3} + g_{02})^2} \right) \left( \frac{C_L}{C_{01}} \right)} \right). \quad (19)$$

Real poles are obtained if  $g_{m3}$  is further increased, but the frequency of the closed-loop zero decreases, and slow components might appear. The dominant pole and zero are close enough (mismatch < 10%) if

$$4 \left( \frac{g_{m1}g_{m2}}{(g_{m3} + g_{02})^2} \right) \left( \frac{C_L}{C_{01}} \right) < 0.25. \quad (20)$$

Additional computations show that under this condition, the poles are located at

$$\omega_{p1} \cong \frac{\beta g_{m1}g_{m2}}{C_{01}(\beta g_{m3} + g_{02})}, \quad \omega_{p2} \cong \frac{\beta g_{m3}}{C_L} = \frac{\beta g_{m3}}{C_4 + \beta(C_1 + C_3)}. \quad (21)$$

Notice that under these conditions, and with sufficient feedback,  $\omega_z$  and  $\omega_{p1}$  are very close to each other regardless of the absolute value of the load capacitors used; the root-locus is similar to the one depicted in Figure 3. The frequency of both  $\omega_{p1}$  and  $\omega_z$  increases, increasing the speed, if the parasitic capacitance at the output of the first stage,  $C_{01}$ , is reduced—this is an important design consideration. If  $C_{01}$  is reduced, then complex poles might appear, but these can be tolerated; although some ringing appears in the transient response, fast response results if the real part of the poles is sufficiently large. The SC amplifier of Figure 1(a) has been simulated using the NCFE architecture with transconductances  $g_{m1}$ ,  $g_{m2}$ , and  $g_{m3}$  set at 1 mA/V, 4 mA/V, and 10 mA/V, respectively. The amplifier DC gain is around 90 dB, because a telescopic amplifier is used for the first stage. Shown in Figure 15(a) is the transient response for the NCFE amplifier for  $C_3 = 0.25$  pF and  $C_4 = 0.5$  pF and

- (1)  $C_1 = 0.5$  pF,  $C_2 = 1$  pF, and  $C_{01} = 0.25$  pF (nominal case);
- (2)  $C_1 = 0.5$  pF,  $C_2 = 1$  pF, and  $C_{01} = 0.5$  pF (large capacitance at the output of first stage);
- (3)  $C_1 = 0.5$  pF,  $C_2 = 1$  pF, and  $C_{01} = 0.75$  pF (largest capacitance at the output of first stage);
- (4)  $C_1 = 1$  pF,  $C_2 = 2$  pF, and  $C_{01} = 0.25$  pF (bigger input and integrating capacitors).

Although the variations in parameters are large, the 0.1% settling time is around 3.2 nanoseconds for cases 1 and 4.

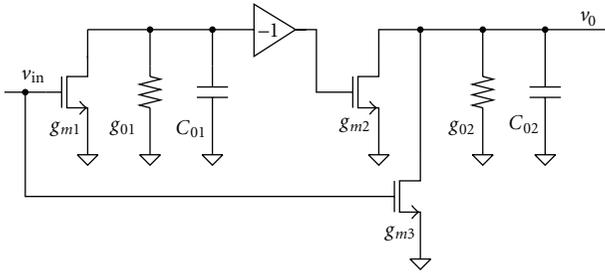
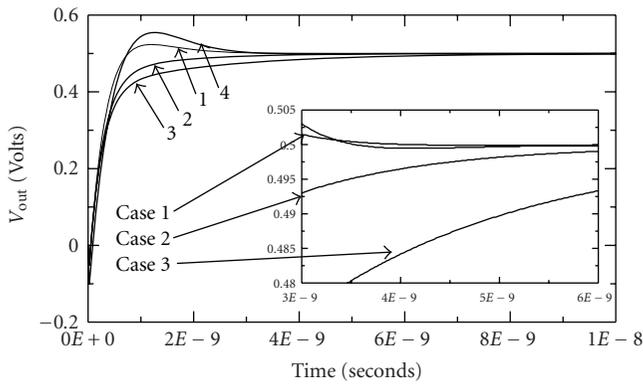
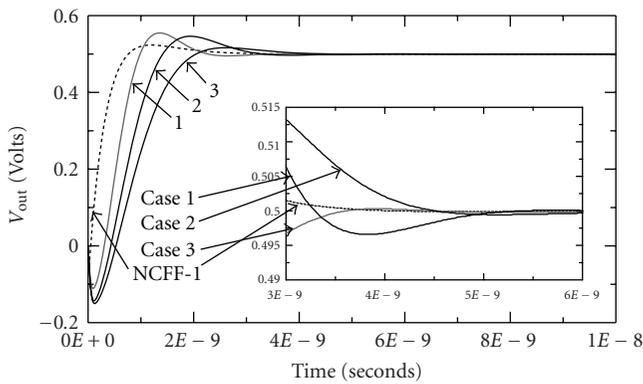


FIGURE 14: No capacitor Feed forward (NCCF) compensated two-stage amplifier.



(a)



(b)

FIGURE 15: (a) Pulse response for the NCCF two-stage amplifier and (b) the Miller amplifier.

The pulse response is slow if  $C_{01}$  increases, cases 2 and 3, where the 1% settling is 3.3 and 7 nanoseconds, respectively. For comparison, a two-stage Miller amplifier with large transconductance stages was designed; the transconductances used are  $g_{m1} = g_{m2} = 10 \text{ mA/V}$  and a nominal  $C_m$  of 2 pF; a nulling resistor optimized for RHP zero cancellation is used. The amplifier DC gain is set at 90 dB. Shown in Figure 15(b) are three simulated cases for the Miller amplifier ( $C_3 = 0.25 \text{ pF}$  and  $C_4 = 0.5 \text{ pF}$ ):

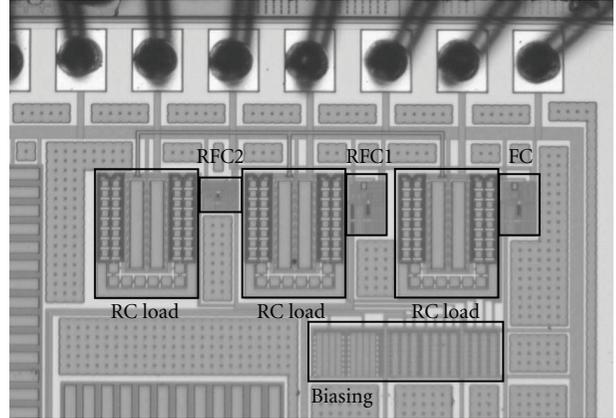


FIGURE 16: Chip microphotograph of the FC, RFC1, and RFC2 OTA prototypes.

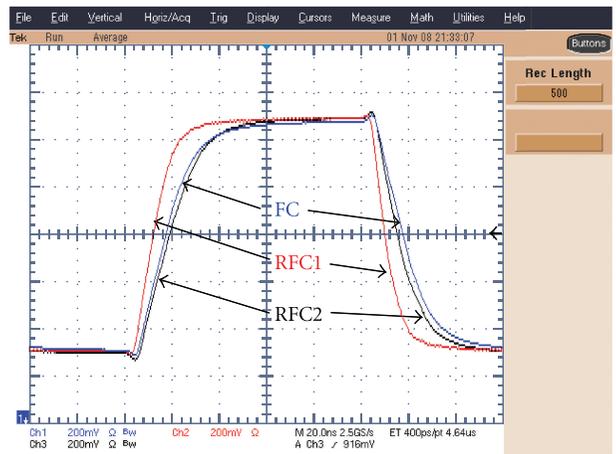


FIGURE 17: Pulse response for FC, RFC1, and RFC2 OTAs.

- (1) input and integrating capacitors of 0.5 pF, 1 pF, and  $C_m = 2 \text{ pF}$ ;
- (2) input and integrating capacitors of 1 pF, 2 pF, and  $C_m = 3 \text{ pF}$ ;
- (3) input and integrating capacitors of 1 pF, 2 pF, and  $C_m = 4 \text{ pF}$ .

Notice that the NCCF approach (nominal case,  $C_{01} = 0.25 \text{ pF}$ ) can be faster than the Miller amplifier, even if the latter structure uses larger transconductances.

## 6. Experimental and Simulated Results

The aforementioned FC, RFC1, and RFC2 OTA prototypes have been fabricated in TSMC 0.18  $\mu\text{m}$  CMOS process; a microphotograph of the chip is shown in Figure 16. The silicon area of the amplifiers is 4700  $\mu\text{m}^2$ , 4950  $\mu\text{m}^2$ , and 3000  $\mu\text{m}^2$ , and they were biased with a total current of 800  $\mu\text{A}$ , 800  $\mu\text{A}$ , and 400  $\mu\text{A}$ , respectively. Input, integrating and load capacitors of 2.2 pF, 2.2 pF, and 2.5 pF, respectively, were used. Equipment and PCB routing parasitics contribute

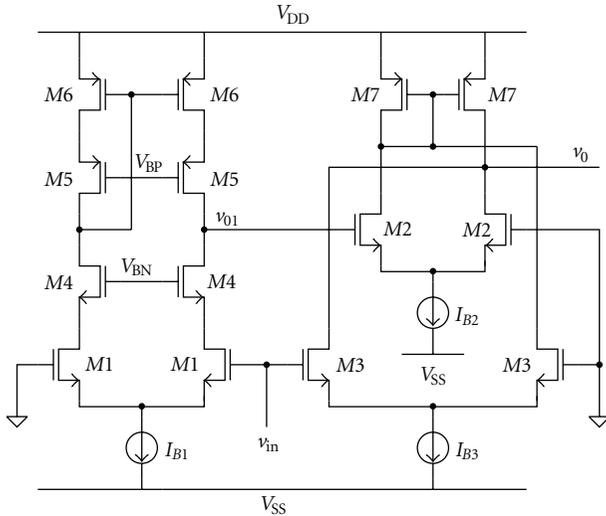


FIGURE 18: Single-ended amplifier with NCCF compensation scheme.

an additional 2.1 pF, 3.4 pF, and 2.2 pF to the FC, RFC1, and RFC2, respectively. The amplifiers pulse response is depicted in Figure 17 with no observable overshoot. The 1% settling-time is 20.7 nanosecods, 13.7 nanosecods and 20.8 nanosecods respectively.

A two-stage OTA using NCCF compensation scheme was implemented in AMI 0.5  $\mu\text{m}$  CMOS technology with supply voltages of  $\pm 1.25\text{ V}$ ; the schematic is shown in Figure 18. The active area for the amplifier is around 0.16  $\text{mm}^2$ . The bias current for the first stage is only  $I_{B1} = 50\ \mu\text{A}$ , and the one used in the second stage is  $I_{B2} = 2\ \text{mA}$ . For the feedforward stage the tail current is  $I_{B3} = 5\ \text{mA}$ . The transistor aspect ratios are  $960\ \mu\text{m}/0.6\ \mu\text{m}$  for the first differential pair,  $600\ \mu\text{m}/0.9\ \mu\text{m}$  for the second stage, and  $120\ \mu\text{m}/0.9\ \mu\text{m}$  for the feedforward path. According to [25] and [27] the polezero matching should be fairly good. Postlayout simulations show that for a load capacitance of 8 pF and a step of 300 mV, the 1% settling time of the OTA was 5.1 nanoseconds. Neither overshoots nor low-frequency components were observed. The postlayout simulation results for a single-ended OTA show a DC gain of 91 dB, GBW of 325 MHz and slew rate of  $140\ \text{V}/\mu\text{s}$ .

An inverting amplifier, similar to the one shown in Figure 1(a), was experimentally tested. For the test setup, external capacitors of 5 pF were employed. The total effective load capacitance was 12 pF (estimated capacitance of measurement equipment probe capacitance and package bond-pad capacitance). Transient postlayout results for a 400 mV peak signal are shown in Figure 19(a); the amplifier response corresponds to a typical first-order system. The 1% settling time is around 6.5 nanosecods; the first 1 nanosecond is associated with slew rate limitations while 5.6 nanosecods correspond to linear settling. The chip was measured and the 1% settling time for an input step of 800 mV was 17 nanosecods, as depicted in Figure 19(b), which divides to roughly 12 nanosecods in the slew rate limited and 5 nanosecods in the bandwidth limited settling phases. For these results, the input edge had a fall time of around 3

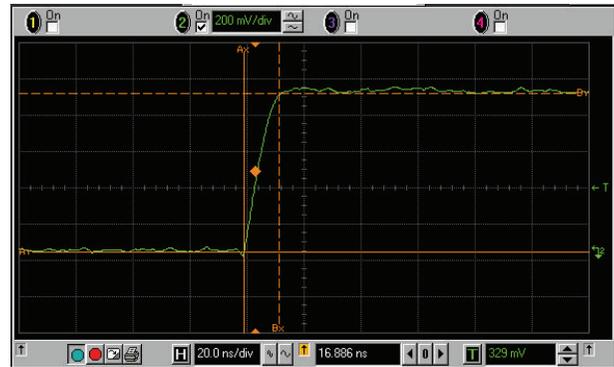
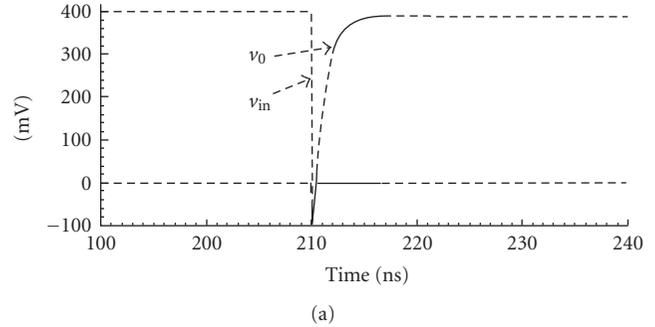


FIGURE 19: (a) Simulation results for the single-ended NCCF amplifier and (b) experimental results.

nanosecods due to PCB, bond-pad parasitic (DIP-40 package was used), and equipment loading effects. The output step response has no ringing, which shows a good phase margin. Postlayout simulation results for the amplifier with a 4 nanosecods fall time input step, and parasitic capacitors at the OTA input of 3pF and load capacitor of 12 pF show a 1% settling time of around 13.5 nanosecods, which is in good agreement with the measured results.

## 7. Conclusions

Feed-forward techniques can improve the speed of closed loop switched-capacitor networks. It has been shown that the recycling folded-cascode OTA presents higher slew rate and superior settling performance than the conventional folded-cascode OTA for the same power consumption. The pole-zero pair present in feed-forward topologies must be placed at high frequencies to avoid slow settling components. Another important advantage of feed-forward schemes is that gain enhancement and smaller parasitic capacitor presented at the input reduce the error after settling than that obtained with the regular folded-cascode OTA. The NCCF compensation scheme enables both high gain and fast settling time, resulting in accurate and fast step response. LHP zeros are used to cancel the phase shift of poles to obtain a good phase margin. The effect of pole-zero mismatches on feed-forward amplifier's performance was studied, and it was

shown that the pole-zero cancellation should occur at high frequencies for best settling time performance. Simulation and experimental results for the amplifiers are in accordance with the theoretical derivations.

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