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Research Article

A New XOR Structure Based on Resonant-Tunneling High Electron Mobility Transistor

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A new structure for an exclusive-OR (XOR) gate based on the resonant-tunneling high electron mobility transistor (RTHEMT) is introduced which comprises only an RTHEMT and two FETs. Calculations are done by utilizing a new subcircuit model for simulating the RTHEMT in the SPICE simulator. Details of the design, input, and output values and margins, delay of each transition, maximum operating frequency, static and dynamic power dissipations of the new structure are discussed and calculated and the performance is compared with other XOR gates which confirm that the presented structure has a high performance. Furthermore, to the best of authors' knowledge, it has the least component count in comparison to the existing structures.

1. Introduction

Resonant-tunneling diodes (RTDs) are of interest for use in different applications [1, 2]. The main reasons are that RTDs exhibit a negative differential resistance (NDR) region in their current-voltage characteristics and in comparison to conventional devices, take advantage of their higher speed of operation and lower power dissipation and possibility of operation at room temperature [3], and can increase circuit integration density because they usually reduce device count per circuit function. Moreover, resonant-tunneling diodes in combination with other high speed three terminal devices such as high electron mobility transistors (HEMTs) can be cointegrated to design a variety of compact and ultra fast digital circuits [4, 5]. While there are many attempts for extending the material and structure based on RTDs, there is a need for work at the logic and architectural levels to fully harness the potentials of RTDs. However, Chen et al. introduced a resonant-tunneling high electron mobility transistor (RTHEMT) with novel current voltage characteristics [6]. The RTHEMT shows the near-flat valley current in the output *I-V* curve at certain gate voltages at room temperature.

The most significant part of a multiplier is adder. XOR gate forms the fundamental building block of full adders, therefore, improving the speed of XOR gate can lead to significant increasing speed of the entire system. The XOR function widely used in ALUs, digital encryption systems [7], and parity checking circuits [8].

In this paper, a new structure for two-input XOR based on RTHEMT is presented. It comprises only two depletion mode FETs and an RTHEMT. It is the first time, to the best of the authors' knowledge, an XOR gate based on the RTHEMT is proposed. The characteristics of the proposed XOR gate are calculated by employing a new SPICE model for simulating RTHEMT. The remainder of this paper is structured as follows. In Section 2, we present a brief survey to the current XOR structures. In Section 3, the proposed XOR structure, its design procedure and performance are explained. Conclusions are drawn in Section 4.

2. Review of Some XOR Gates

Designing new XORs is of much attantion because they are the main part of an ALU and other digital devices. Different structures and designs were presented in literature for XOR gates over the years. Most of XOR gate circuits are based on FET transistors [9–12] also there are some XOR gates based on other logics [13–15]. In this section we briefly describe

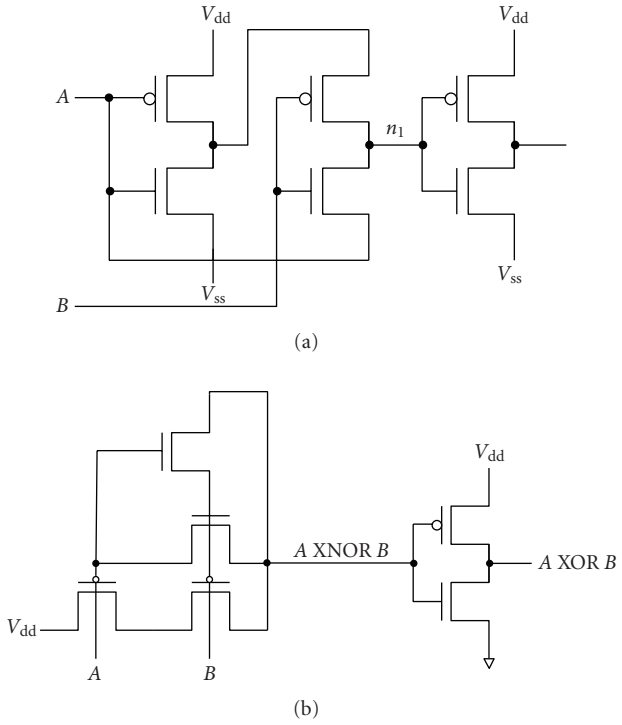

Figure 1: Designing two different XOR gates with six transistors (The figure selected from [9]).

three XOR gates that comprise the least components. Two XOR with six FETs (introduced in 1994), one XOR with 4 FETs (introduced in 2000) and one XOR that uses RTDs (introduced in 2000) are briefly reviewed. To the best of our knowledge these designs are the least component count XOR structures.

2.1. Six-Transistor XOR Design. Wang et al. in 1994 proposed two designs that used four transistors for its basic logic and to achieve good signal level outputs and satisfactory driving capabilities, they cascaded the designs with a standard two FET inverter (six FETs in total) [9]. Figure 1(a) shows the first XOR gates, the tailing inverter can improve the poor signal which comes from node n_1.

Figure 1(b) shows the second design. The average delay for Figures 1(a) and 1(b) circuits was 3.84 nanoseconds and 1.42 nanoseconds respectively. The average power dissipation was reported 400 μW and 310 μW respectively [9].

2.2. Four-Transistor XOR Design. Bui et al. in 2000 proposed the smallest XOR that uses only four transistors [10] and called it powerless XOR, because it has no power supply (Figure 2). They used it in a full adder [11, 12]. The original paper reports that the transistors have a channel length of 0.6 μm and a channel width of 2.4 μm using 3.3 V logic. The reported delay was 350 picoseconds and maximum shown inputs frequency was 200 MHz. Moreover, the propagation delay has been fostered 43% than complementary CMOS [10].

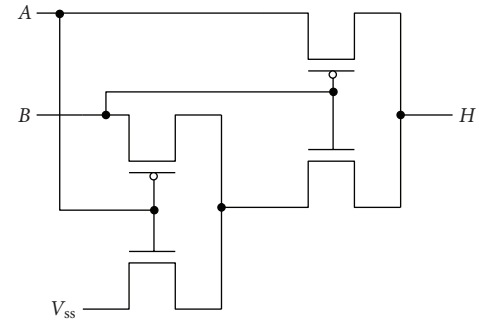

Figure 2: Designing an XOR with four transistors (the figure selected from [10]).

2.3. The XOR Based on Controlled Quenching of Series-Connected Negative Differential Resistance Device. Chen et al. proposed an XOR based on controlled quenching of series connected negative differential resistance (NDR) device [13, 14] (Figure 3). By choosing different areas for RTDs, the peak currents have a relation of $I_{RTD1} < I_{RTD2} < I_{RTD3}$. In the presented circuit, there are three subcircuits called NDR. In total the circuit includes six FETs and three RTDs. Original paper reports that the areas of RTD1, RTD2 and RTD3 are $2 \times 3\,\mu m^2$, $2 \times 4\,\mu m^2$ and $2 \times 5\,\mu m^2$ respectively. All the FETs have a gate length of 7 μm. The gate widths of FET1 and FET3 are 15 μm and the gate widths of FET2 and FET4 are 5 μm. "When both VA and VB are logic 0 (0 V), I_{P1} is the smallest and RTD1 is quenched. As a result, the output is logic 0. When one of the inputs logic 1 (0.5 V) and the other logic 0, I_{P2} is the smallest and RTD2 is quenched. This leads to logic 1 at the output. When both inputs are logic 1, I_{P1} and I_{P2} are increased and both exceed I_{P3}. Thus RTD3 is quenched and the output becomes logic 0 again" [13]. I_{P1}, I_{P2} and I_{P3} are the peak currents of each device. No results reported for the frequency and delay. Only a simulation result has been shown with the maximum input frequency of 10 KHz.

3. New XOR Structure

In this paper, a new XOR gate circuit based on RTHEMT is presented. In this section, the RTHEMT and its modeling in SPICE simulator are introduced at first, then details of the design procedure for the new XOR in three subsections are discussed and finally the performances of the gate are drawn.

3.1. RTHEMT and Its Modeling. "An InP-based resonant-tunneling high electron mobility transistor (RTHEMT) incorporates a pseudomorphic InGaAs/AlAs/InAs RTD into the source of an InGaAs/InAlAs high electron mobility transistor (HEMT)" [16]. Figure 4(a) depicts epitaxial structures of the RTHEMT, grown by molecular beam epitaxy on a semi-insulating InP substrate. The RTHEMT *I-V* curve with its near-flat valley current can be explained as following. According to the integration scheme [6], the HEMT can be considered as the load of the RTD (driver) in the RTHEMT. The *I-V* curve of an isolated RTD is also shown in Figure 4(b). "As V_{DS} increases from *0V* the load line

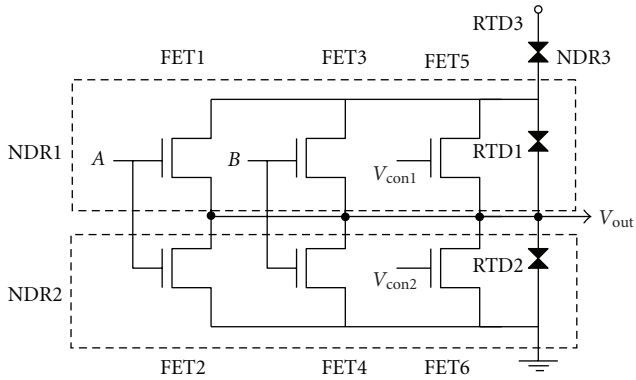

Figure 3: XOR based on controlled quenching of series connected negative differential resistance (NDR) devices (the figure selected from [14]).

intersects with the driver *I-V* curve at the linear region before the resonance, therefore, the RTD serves as a linear resistor and I_{DS} continues to increase until the peak current is reached. As the V_{DS} further increases, the load line only intersects with the driver *I-V* curve at the valley. Therefore, the RTD switches from peak to the valley" [6]. Figure 4(c) illustrates the I_{DS} versus V_{DS} curve for the RTHEMT.

In order to use RTHEMT device in circuit analyzing and simulating the desired circuits, a SPICE model is needed. As discussed in the literature, there are two major categories for simulating RTD circuits: the physics-based models and the nonphasic-based models [17] or macromodels. Although physics-based models are accurate, they need to solve complicated equations, so they are time consuming. In this paper, we have used a new non-physics-based model by exploiting special elements in SPICE. By modeling the RTHEMT in the SPICE, the simulation run time is decreased and also circuit designers are able to present novel and complex circuits without long run time concerns. In the following the SPICE subcircuit for the RTHEMT is presented. This subcircuit includes two sections, a section for HEMT and another for RTD. HEMT is modeled by utilizing a level 3 SPICE model for FET [18] and by adjusting its parameters to match the chosen technology and with the experimental values reported in original paper [19], though RTD model has more details. As shown in Figure 5(a) the RTD conductance is modeled by using a GTABLE and its capacitance is modeled using GPOLY, ETABLE, R and C parts [19]. The ETABLE contains the *Q-V* characteristic of the RTD. The RC circuit is employed as a differentiator and will generate a voltage proportional to the capacitance's current of the RTD. Finally a GPOLY is used to produce the current. This structure can model an arbitrary nonlinear capacitance. FET drain current (I_{DS}) versus gate-source voltage (V_{GS}) for different drain-source voltages (V_{DS}) is drawn in Figure 5(b). This figure helps better understanding of the device functionality as well as the way of producing near-flat valley, with a current which is almost equal to RTD minimum current. Pseudoparabolic part of FET *I-V* characteristic and linear lines in Figure 5(b) depict the saturating region and linear region respectively. In this figure, a RTD characteristic is also illustrated (from V_{gg} point and as a load for FET's input). Hence, this graph fulfills two conditions of the subcircuit: (i) $V_{gg} = V_{GS} + V_{RTD}$ and (ii) $I_{DS} = I_{RTD}$. According to this figure it can be concluded that if the RTD curve has only one intersect with the second-order part of the FET curve (saturation region), at its minimum negative differential resistance (NDR) region, a flat current equal to the minimum current of RTD will be obtained.

3.2. Designing Procedure. Current density waveform of RTHEMT and its nearly flat valley current that are shown in Figure 4(c), enable us to present a two-input XOR gate easily. Figure 6 depicts the proposed circuit for two-input XOR gate. In this design, inputs are in the voltage mode and the output is produced in the current mode. In following the design procedure for proposed RTHEMT XOR is explained in three steps with more details.

3.2.1. Selecting the Technology and Adjusting the RTHEMT Model. The design is based on 90 nm HEMT technology. Since the original paper [6] stated that the RTD area is equal to $2 \times 3\,\mu m^2$, hence the modeling should be repeated. For new modeling, adjusting the RTD area and capacitors and utilizing a new HEMT model for 90 nm technology are necessary. The resulted *I-V* curve is shown in Figure 7 with solid line. This curve exhibits less peaks to valley current ratio with more rising current amount after the valley point than Figure 4(c). These happen due to utilizing 90 nm technology which in contrast with previous technologies, input/output characteristics (corresponding to FET curves in Figure 5(b)) have lower slopes.

3.2.2. Selecting the Load Line Resistances. As an intermediate step and before final design, we replace the FETs, which are shown in Figure 6, with constant linear resistors. Therefore, we aim to find the resistance value in this step. Less power consumption and less speed are obtained by increasing the input resistance; however, it leads to a smaller amount of input margins. In this design, we select a 5 KΩ resistance.

3.2.3. Input and Output Margins. In this step four following variables are defined: $V_{L\text{-Low}}$ (the minimum voltage for logic 0), $V_{L\text{-High}}$ (the maximum voltage for logic 0), $V_{H\text{-Low}}$ (the minimum voltage for logic 1) and $V_{H\text{-High}}$ (the maximum voltage for logic 1). For each variable, a proper value should be assigned in order to obtain good input/output margins. Figure 7 illustrates two lines of *A* and *B* in conjunction with the RTHEMT *I-V* characteristic. The slope of these lines is specified with $R/2 = 2.5\,K\Omega$ and the area between these two lines is unallowable. These lines are tangent with the maximum and minimum point of *I-V* curve as shown in the figure and the voltage of logic 0 and logic 1 should not be selected such that the above load line lies between these two tangent lines. Otherwise there will be a memory behavior in the circuit because the load line will cross the *I-V* curve in

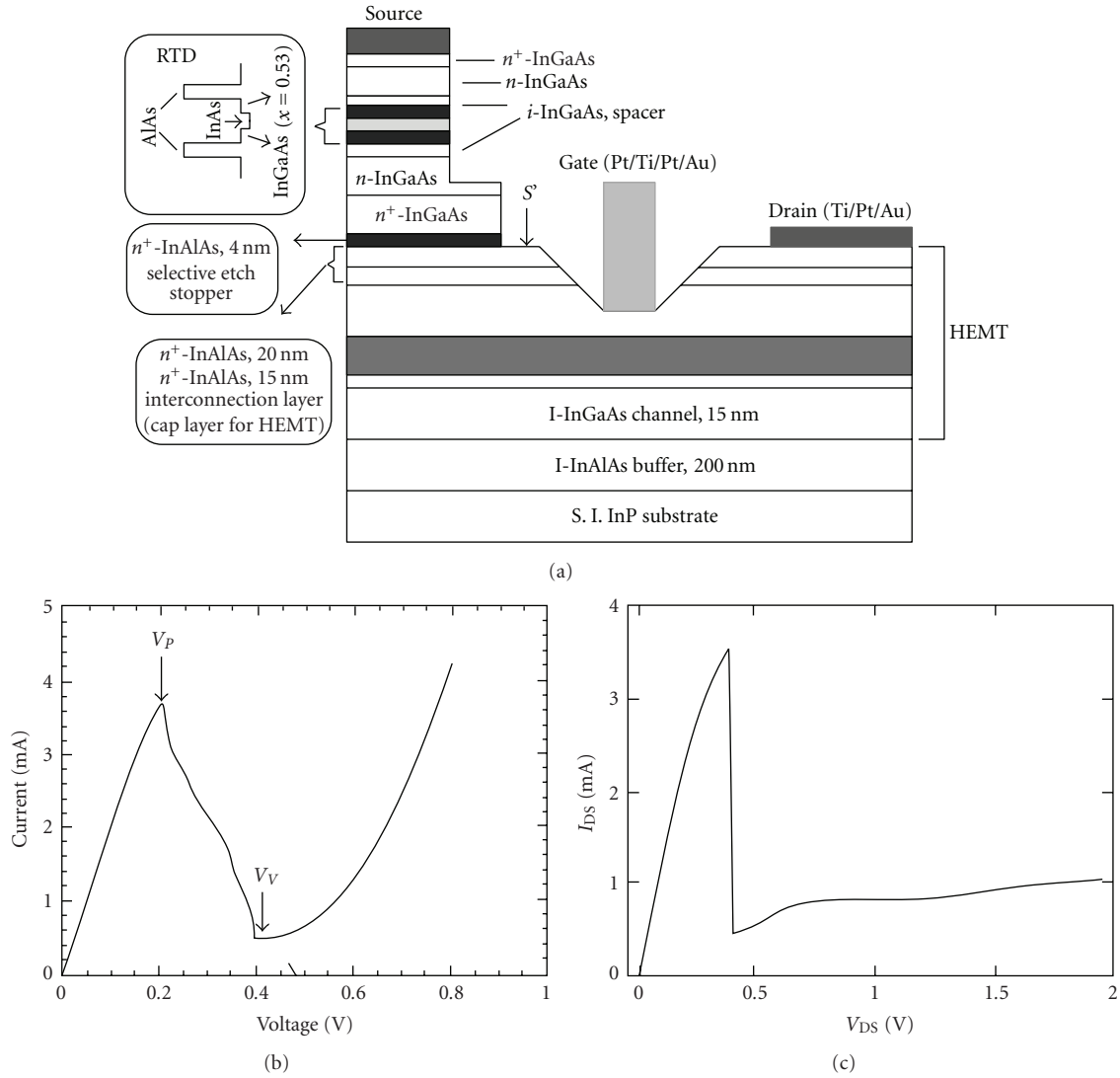

Figure 4: (a) Epitaxial structures of RTHEMT, (b) Isolated RTD *I-V* curve and (b) RTHEMT *I-V* characteristic. As reported in original paper, the RTD has a *P/V* ratio of 8 : 1 at room temperature, with a peak voltage of 0.2 V and valley voltage of 0.4 V. The peak current density is 62 KA/cm^2 (all figures selected from [6]).

three points. The boundary of these variables caused some limitations such as (1):

$$\frac{V_{L\text{-High}} + V_{H\text{-High}}}{2} < 0.88\,V,$$
$$V_{H\text{-Low}} > 1.1\,V. \tag{1}$$

We add another limitation so that the input margins for low and high logics should be equal to each other (2):

$$\left(V_{L\text{-High}}\right) - \left(V_{L\text{-Low}}\right) = \left(V_{H\text{-High}}\right) - \left(V_{H\text{-Low}}\right). \tag{2}$$

By considering the three last equations, there would be only one degree of freedom for selecting the four mentioned variables that we use this one for generating a good margin in the output, consequently, the below values are assigned to variables:

(i) $V_{L\text{-High}} = 0.3\,\text{V}$,
(ii) $V_{L\text{-Low}} = 0$,
(iii) $V_{H\text{-High}} = 1.4\,\text{V}$,
(iv) $V_{H\text{-Low}} = 1.1\,\text{V}$.

Figure 8 shows the valid input margins and the resulted output margin. By considering this graph we calculate the output margins as follows:

(i) $I_{L\text{-High}} = 42\,\mu\text{A}$,
(ii) $I_{L\text{-Low}} = 0$,
(iii) $I_{H\text{-High}} = 59\,\mu\text{A}$,
(iv) $I_{H\text{-Low}} = 90\,\mu\text{A}$.

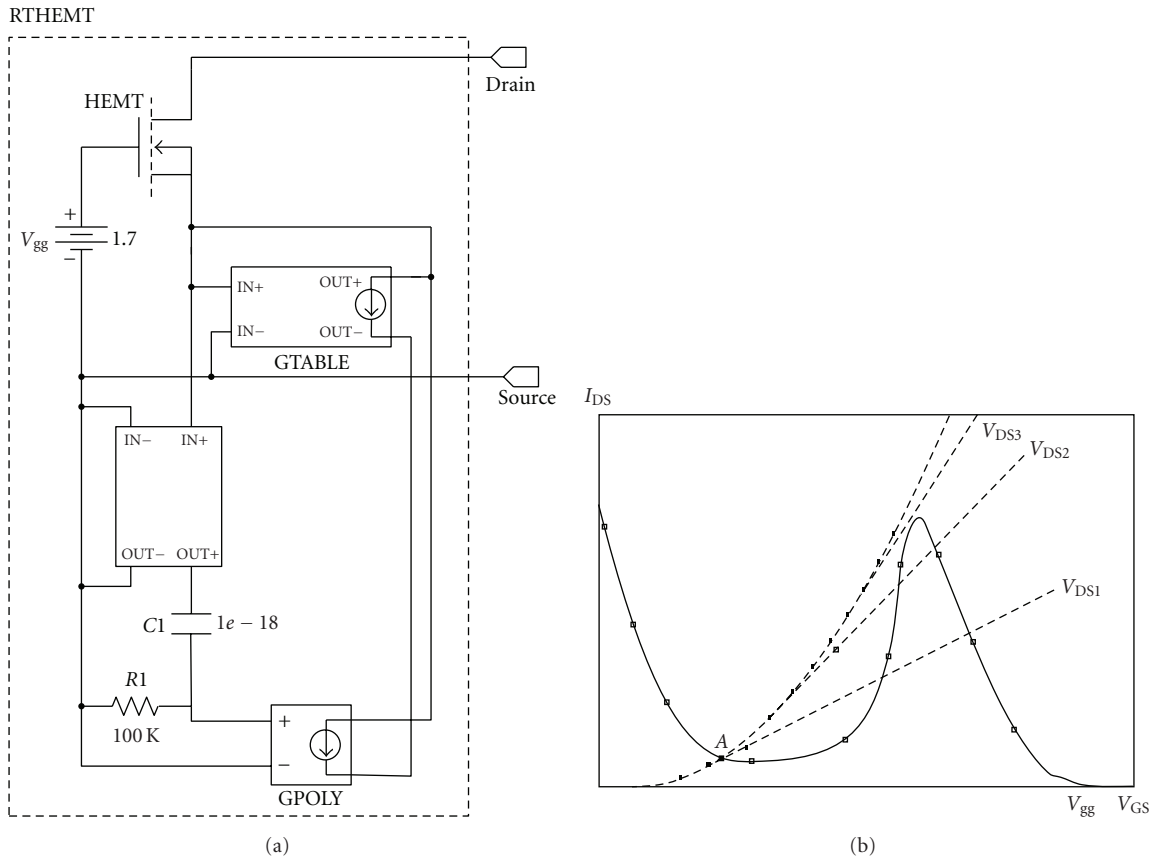

Figure 5: (a) Interior design circuit for modeling RTHEMT. The HEMT characteristics are: Level = 2, $V_{TO} = 0.2$, $Kp = 260e-6$, Gamma = 2 and Lambda = 0.08. The RTD characteristics are: P/V ratio of 8 : 1 at room temperature, the peak current density is 62 KA/cm^2 and the area is 0.145 μm^2. (b) Solid line and dotted lines show a RTD and a FET I-V characteristic respectively. At certain V_{gg} the RTD curve intersects with the saturation FET curve in only one point (point A) which results in the flat current.

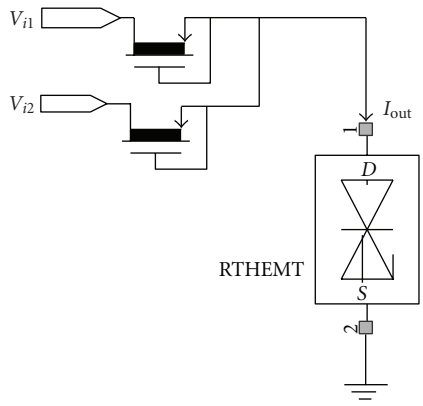

Figure 6: The new two-input XOR gate based on RTHEMT. The RTHEMT charactrestics are the same as Figure 5(a) and the FET characteristic are: Level = 3 SPICE model with $Kp = 406e - 6$ and $V_{TO} = -1.6$ V.

As a last step we rereplace the resistors with two depletion mode transistors in order to achieve the original design. These transistors lead to high scaling and occupied less area in a chip in comparison to resistors. The final design scheme is depicted in Figure 6.

3.3. Simulation Results and Performance. The proposed gate which is designed in previous section is simulated in the SPICE simulator by using the presented model with $1fF$ capacitance load ($C_L = 1fF$). Figures 9 and 10 show the simulation results. Simulations were also run with different component parameters, especially with different resistance values and no sensitivity to any particular component was observed. While NDR and RTD devices had been criticized for their vulnerability to process variations, recent research has demonstrated the feasibility of its use in many application [20–25]. In following subsections the performance of the proposed gate in terms of static power dissipation, dynamic power dissipation, transient energy and latency is calculated.

3.3.1. Static Power. Table 1 shows the static power for four static states of the gate. Assuming equal probability for these four states, we can calculate average static power consumption of the gate which is equal to 151.6 μw.

3.3.2. Transient Energy. For each two-input gate, there are twelve transition possibilities; however, for a gate with symmetric inputs, number of transitions reduces to seven

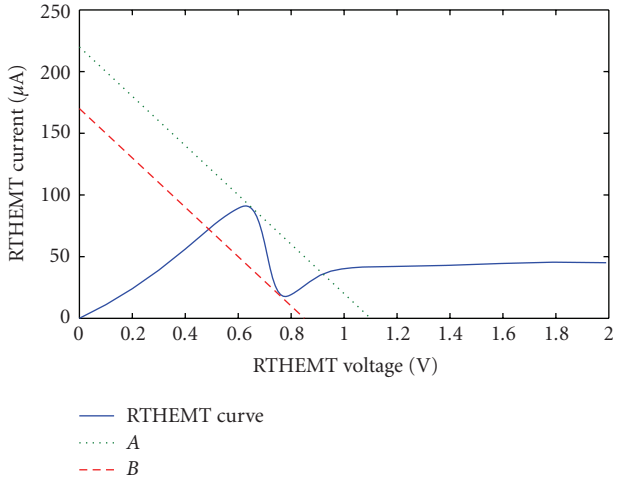

Figure 7: Solid line shows the new RTHEMT characteristics (by employing 90 nm technology) and two other lines show two load lines with 1/2.5 KΩ slopes which are tangent to the minimum and the maximum of the RTHEMT curve. The load lines between A and B lines lead to memory behavior and are invalid.

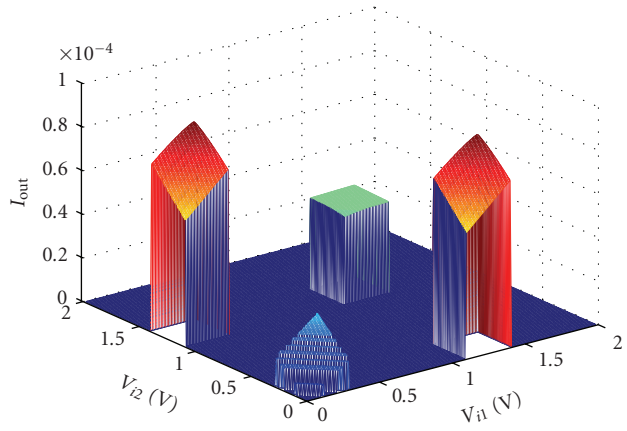

Figure 8: The output gate current (vertical axis) as a function of two input voltages V_{i1} and V_{i2} (two horizontal axes) shows the valid ranges and margins.

Table 1: Static power dissipation.

State	Static power (μw)
00	9.7
01	268
10	269
11	59.7

distinct transitions. Figure 9(a) shows seven different input transitions which applied to the proposed XOR circuit and Figure 9(b) depicts the response to the applied inputs. The

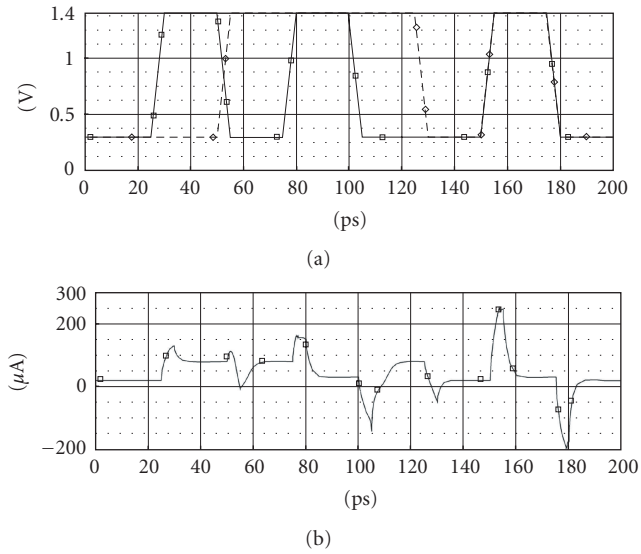

Figure 9: (a) Seven different input voltage transitions and (b) output simulation result waveform in current mode with $1fF$ capacitance load.

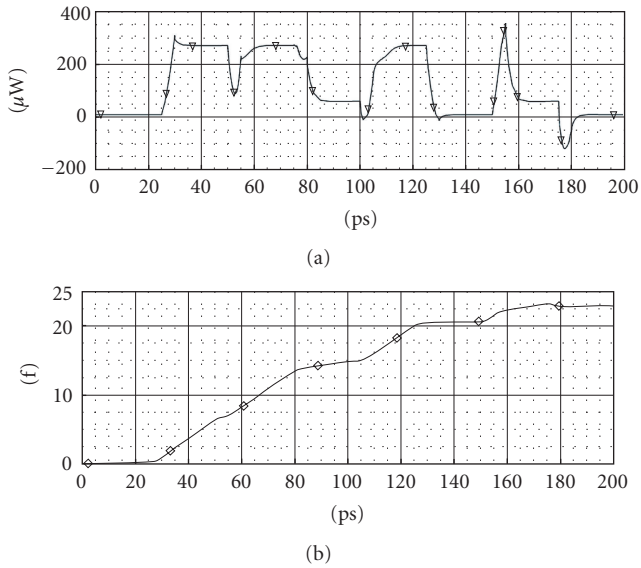

Figure 10: (a) Summation of power of sources in the circuit including input waveform generators and bias sources ($C_L = 1fF$). (b) Integral of total, that is, static and dynamic, power consumption for power of sources (see (3)). The input waveforms are same as Figure 9(a).

dynamic energy dissipation is obtained from this figure and (3).

$$E_T = \int_{-(T/2)}^{T/2} p(t')dt',$$
$$E_t = E_T - \left(\frac{T}{2}\right)\left(P_i + P_f\right), \tag{3}$$

where E_T is the total energy including transition energy and static energy, T is time of the period, $p(t')$ is summation of

Table 2: Dynamic energy dissipation and delay for seven different transitions.

Number	First state	Second state	Transition energy (fj)	Delay (picoseconds)
1	**00**	**01**	0.6	7.2
2	**00**	**11**	0.92	8
3	**01**	**00**	0.41	5
4	**01**	**10**	0.7	8.1
5	**01**	**11**	1.2	7.3
6	**11**	**00**	−0.41	8
7	**11**	**01**	0.16	11

Table 3: The comparison between proposed XORs.

	Input voltages and margins	Output margine	Number of components	Performance	Design consideration
6-transistor XOR	High Logic: 5 V Low Logic: 0 V	Not mentioned	FET : 6	Simulation results up to 50 MHz, Maximum delay: Figure 3(a): 3.98 nanoseconds Figure 3(b): 1.75 nanoseconds	There are two types of implementation with different characteristics
4-transistor XOR	High Logic: 3.3 V Low Logic: 0 V	Not mentioned	FET : 4	Simulation results up to 200 MHz, delay: 350 picoseconds	No power supply (powerless design)
Quenching of series-connected NDR devices	High Logic:0.5 V Low Logic: 0 V	Not mentioned	RTD : 3 FET : 6	Not mentioned	For the XOR function, two FETs can be eliminated by exact design of each RTD area
RTHEMT XOR (This paper)	High Logic: 1.1–1.4 V Low Logic: 0–0.3 V	High logic: 59–90 μA Low Logic: 0–40 μA	FET: 2 RTHEMT: 1	Max Freq: 90.90 GHz Max Delay: 11 picoseconds	1. One state has nearly zero static power dissipation. 2. In highest frequency it dissipates only 201.6 μw

all power sources which is equal to power of the gate (as shown in Figure 10(a)), E_t is the transition energy; P_i/P_f is static power for initial/finite state. The calculation results are shown in Table 2.

3.3.3. Transient Latency. The transient latency for seven different transitions is shown in fourth column of Table 2. According to the Table 2, the maximum delay is happened in response to **11** to **01** transition and is equal to 11 picoseconds and the minimum one is happened in response to **01** to **00** transition and is equal to 5 picoseconds.

3.3.4. Performance. As stated before, the maximum delay is happened in response to 11 to 01 transition and is equal to 11 picoseconds. Therefore, the maximum frequency of the gate is 1/11 picoseconds = 90.90 GHz. Furthermore, by considering the fourth column of Table 2 and by using the (4) the dynamic power will be calculated

$$P_{\text{ac}} = \frac{F}{12}\sum_{i=1}^{12} E_t(i). \tag{4}$$

Figure 10(b) shows the integral of total power dissipation for the proposed circuit in the specific input transitions (Figure 9(b)). As shown in the table the energy dissipation is ranged from −0.41 to 1.2 femto joule (the minus sign means that the power is returned from the gate to the sources). Therefore, the average energy consumption assuming equal probability of occurrences for each twelve transition is about 0.55 fj for each transition. Therefore, if the gate works at its highest frequency (90.90 GHz), it dissipates only 50 μw (0.55 $fj \times 90.90$ GHz = 50 μw) as its dynamic dissipation.

The calculation results demonstrate that static power dissipation (151.6 μw) is much higher than the dynamic

dissipation. Therefore, it can be concluded that there is no restriction caused by the dynamic dissipation and the XOR gate circuit can operate in its highest frequency (90.90 GHz). The power dissipation in FET-based gates is dynamic; however, the proposed approach bears static dissipation. Moreover, one of the input states has near zero static power (state 00 dissipates only 9.7 μw), hence, this state is suitable for standby mode. Figure 10(b) shows the calculation results which are produced by summation of power of independent sources in the circuit including input waveform generators and bias sources (with negative sign). Table 3 briefly comprises the proposed XOR gate with three aforementioned gates. From theoretical stand-point, speed of the gate is simply depends on product of a R and a C where C is the capacitance of RTHEMT (which depends on the employed technology) plus the load capacitance. On the other hand, R is related to the input margins and power dissipation as mentioned before. Therefore, there are tradeoffs between power dissipation, speed and margins.

$$p_{\text{static}} = \sum_{n=1}^{2} \frac{\left(V_{i,n} - V_{\text{RTHEMT}}\right)^2}{R} \tag{5}$$

where p_{static} is the static power dissipation, $V_{i,n}$ is the voltage of nth input, V_{RTHEMT} is the RTHEMT voltage and R is the equivalent resistance of inputs. In this design we use $R = 5\,\text{K}\Omega$ (in the form of depletion FETs) and got proper values for all these factors as reported in the tables.

4. Conclusion

In this paper, a new XOR logic gate based on RTHEMT is presented. To the best of our knowledge it is for the first time that an RTHEMT-based XOR logic gate is presented. In different subsections, the characteristics of the gate including dynamic and static power consumptions and delays are fully covered. In addition, the results were drawn by employing a new subcircuit model for simulating RTHEMT in SPICE. The simulations demonstrate that most features of the proposed XOR gate circuit have superior performance in contrast with other structures. The comparison between the new XOR gate circuit and other ones is summarized in Table 3.

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