Research Article

A SiGe BiCMOS Instrumentation Channel for Extreme Environment Applications

Chandradevi Ulaganathan,¹ Neena Nambiar,¹ Kimberly Cornett,² Robert L. Greenwell,¹ Jeremy A. Yager,³ Benjamin S. Prothro,¹ Kevin Tham,¹ Suheng Chen,¹ Richard S. Broughton,² Guoyuan Fu,² Benjamin J. Blalock,¹ Charles L. Britton Jr.,¹ M. Nance Ericson,¹ H. Alan Mantooth,² Mohammad M. Mojarradi,⁴ Richard W. Berger,⁵ and John D. Cressler⁶

¹ Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996, USA

² Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701, USA

³ Power and Sensor Electronics, Jet Propulsion Laboratory, Pasadena, CA 91109, USA

⁴ Instrument Electronics and Sensors, Jet Propulsion Laboratory, Pasadena, CA 91109, USA

⁵ Space Products and Systems, BAE Systems, Manassas, VA 20110, USA

⁶ School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA

Correspondence should be addressed to Chandradevi Ulaganathan, culagana@utk.edu

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An instrumentation channel is designed, implemented, and tested in a 0.5- μm SiGe BiCMOS process. The circuit features a reconfigurable Wheatstone bridge network that interfaces an assortment of external sensors to signal processing circuits. Also, analog sampling is implemented in the channel using a flying capacitor configuration. The analog samples are digitized by a low-power multichannel A/D converter. Measurement results show that the instrumentation channel supports input signals up to 200 Hz and operates across a wide temperature range of -180°C to 125°C . This work demonstrates the use of a commercially available first generation SiGe BiCMOS process in designing circuits suitable for extreme environment applications.

1. Introduction

There are numerous applications prompting interest in developing SoC (System-on-Chip) integrated systems. Space exploration presents a niche area wherein extreme environmental conditions pose several design constraints. At present, robotic exploration rovers have all the critical electronics inside a temperature-controlled Warm Electronics Box (WEB) [1]. This dictates a centralized architecture wherein data processing happens in the WEB and the generated control signals are communicated to various parts of the rover through extensive cables. Developing electronic circuits that are capable of reliable operation under extreme environmental conditions facilitates the use of a distributed architecture. This eliminates extensive cabling and thus increases the system reliability. In addition, significant reductions in power consumption, launch volume, and weight (and therefore, launch cost) are achieved.

The objective of this work is to develop a highly integrated front-end and signal processing circuitry capable of reliable operation in extreme conditions. In order to efficiently handle data, instrumentation channels (referred to as “universal” channels in this work) are required to interface external sensors with signal processing circuitry. Also, the use of a multi-channel analog-to-digital converter (ADC) aids in allowing high levels of circuit integration. In this work, numerous external sensors are interfaced to a multi-channel ADC via the universal channels as the front-end interface.

This paper presents the design and implementation of a universal channel suitable for low speed signals. Measurement results from the channel are also discussed. Section 2 presents an overview of the channel and its components. Section 3 discusses in detail the design and implementation of the individual components of the universal channel. The design techniques for reliable operation in extreme environment are discussed in Section 4. Section 5 presents

FIGURE 1: Simplified schematic of the universal channel.

the measurement results and finally Section 6 concludes this work.

2. Universal Channel—An Overview

The universal channel is a low-speed instrumentation channel that is capable of interfacing signal processing circuits with various transducers including thermocouples, RTDs (Resistance Temperature Detectors), pressure gauges, and strain gauges. The universal channel is designed to operate across a wide temperature range that includes -180°C through 125°C . Radiation-hardening-by-design (RHBD) circuitry is implemented in the digital circuits while special layout techniques render the analog circuits in the channel to be radiation tolerant. Numerous industrial channel designs [2–4] are available; however, this is the first multi-channel custom IC designed to operate across a wide temperature range extending down to cryogenic temperatures reported in the literature. Several versions of the universal channel were successfully fabricated and tested with the most recent version fabricated and tested in mid-2009 [5].

The channel is capable of supporting high-voltage sensors of up to 12 V and produces a 12-bit digital output from an ADC. Figure 1 shows, the Wheatstone bridge, the high-voltage level shifting buffer, the flying capacitor network, and the level shifting buffer form the front-end of the analog sampling channel.

The Wheatstone bridge is designed to be reconfigurable in order to interface with a variety of external transducers. The bridge includes three matched $350\text{-}\Omega$ resistors that are used in combination with an external resistive sensor to make a complete Wheatstone bridge. The circuit works on the principle that any change in the bridge resistance, corresponding to a physical change in the sensor, is converted into a differential voltage that is sampled and processed.

The high common-mode voltage differential output from the Wheatstone bridge is level shifted to the low-voltage level (below 3.3 V) by a high-voltage level shifting buffer.

The flying capacitor network performs the analog sampling in the universal channel and provides high input common-mode rejection. The circuit includes a “flying” or sampling capacitor and uses a general purpose high-Z input operational amplifier (op amp) within a switched capacitor configuration to provide programmable gain. The flying capacitor’s built-in calibration and correction circuitry, along with the low offset drift op amp, ensure that the sensor signals are sampled and transmitted to an input channel of the Wilkinson ADC [6]. Following this stage, a level shifter shifts the common-mode voltage of the channel to the center of the input range of the Wilkinson ADC, which is the next signal processing stage.

The sampled analog signal from the flying capacitor network is converted to digital data using the Wilkinson ADC. The 12-bit 16-channel Wilkinson ADC is a low-power, high-resolution, analog-to-digital converter capable of conversions at 20 KSps across the wide temperature range of -180°C to 125°C .

3. Design and Implementation

This section describes the design and operation of the individual blocks of the universal channel as well as the Wilkinson ADC.

3.1. Wheatstone Bridge Network. The Wheatstone Bridge Network is designed to interface with various sensors. Figure 2 presents a simplified schematic of the Wheatstone bridge network. This programmable bridge has three signal connections, two of which are used in any given configuration. This structure, in conjunction with the two switches in the bottom legs, provides the flexibility to have different

FIGURE 2: Schematic of the programmable Wheatstone bridge network.

FIGURE 3: Wheatstone bridge network in half-bridge configuration.

configurations that interface with either full-bridge, half-bridge, or quarter-bridge resistive sensors.

By carefully constructing the layout, the 350-Ω resistors in the bridge are closely matched, making it relatively insensitive to temperature [7]. The bridge is biased by an external current source or an on-chip stimulus current that provides up to approximately 30 mA of bias current (Figure 1). The wiring of the bridge is designed to handle up to 35 mA of current. The n-type single-pole single-throw switches, at the bottom legs of the bridge, are designed to provide a low ON resistance (less than 10 Ω) over the operating temperature range. Since matching between the switch resistances is critical, common-centroid layout techniques are utilized. These switches set the bridge configuration used for measurements.

3.1.1. Control and Operation. The Wheatstone bridge network has three input terminals connected to the corners of the bridge. The fourth corner is connected to the “negative stimulus” terminal (typically tied to ground). The differential output voltage is sampled between *Signal 2* and *Signal 3* by the subsequent flying capacitor network.

FIGURE 4: Wheatstone bridge network in full-bridge configuration.

FIGURE 5: Pin-out of switches and gain setting control shift register.

The configuration of the bridge is set by controlling the switches SW1 and SW2. In the quarter-bridge and half-bridge configurations, both switches (SW1 and SW2) are closed. As depicted in Figure 2, the quarter-bridge configuration has an active external sensor connected between *Signal 1* and *Signal 3* as the upper left element of the bridge. The on-chip resistor network provides the bottom two resistor elements and the upper right element. With this setup, temperature variations and lead resistance reduce the accuracy of the sensor measurements. Using a dummy sensor in a half-bridge configuration mitigates these effects. Single element and lead compensated sensors may be used in this configuration [8].

In the half-bridge configuration (Figure 3), two active external sensors are connected between *Signal 2* and *Signal 3* to provide the upper half of the bridge, while the bottom half of the bridge is provided by the on-chip resistors. This configuration provides better sensitivity along with inherent temperature and lead compensation [8].

By setting both switches SW1 and SW2 to open, the on-chip resistors are not used. Four active external sensors are connected between *Signal 2* and *Signal 3* as a full bridge to provide a signal to the flying capacitor network (Figure 4).

FIGURE 6: Simplified schematic of the high-voltage level shifter.

This configuration is known as a full-bridge configuration. This means that the sensor has a full-bridge inside it.

As shown in Figure 1, an on-chip stimulus current (positive stimulus) is applied to the top of the bridge. The stimulus functions as an adjustable current source that sets the common-mode voltage of the bridge. This current source is driven by a high-voltage current mirror that allows for stimulus voltages higher than those supported by the 3.3-V process. A current output digital-to-analog converter (DAC) is utilized to supply the stimulus input current to this current mirror. The circuit provides a $100\times$ multiplication. The available bridge bias current ranges from 1 to 30 mA.

The bridge configuration and/or the gain setting of the channel are controlled by a serially loaded shift register. Figure 5 provides the pin-out of the control register. When a channel is integrated with other active channels in an application, the shift register is included in a scan path for test mode. Shift registers are also employed to program the stimulus and calibration data during testing and setup. These serial shift registers load the corresponding DACs. All of the shift registers contain multiplexers on each output bit. When the Output Enable (OE) control signal is *low*, the output bits are connected to ground irrespective of the data stored or being loaded into the register's latches. This feature protects the rest of the channel's circuitry as the data is loaded. When the data is fully loaded, Output Enable is set *high*. With Output Enable on *high*, the internal multiplexers will output the data that is stored in the register's latches.

3.2. High-Voltage Level Shifter. The high-voltage level shifter is a unity-gain buffer that translates the small differential output voltages (± 200 mV) from the Wheatstone bridge network across a wide input common-mode range (V_{CM}) of 0–10 V to a differential signal at a lower common-mode

voltage range of 1.8–2.2 V. This allows the rest of the analog processing and data conversion to occur at low voltages. A simplified schematic is illustrated in Figure 6.

The basic functionality of the circuit is as follows: the differential signal is fed into the gates of the dual level shifters formed by M_{1-4} . After level shifting (which ensures operation at low common-mode range), the differential voltage signal is converted to current by M_5 and M_6 , and passed down through the V_{CM} level shifters into the current mirrors formed by Q_{1-4} . Once mirrored into the output branches, the differential signal is converted to a voltage by diodes M_{13} and M_{14} , where it is read by standard low-voltage CMOS analog processing circuitry. The pMOS transistors forming the high-side current sources are protected from breakdown by high-voltage N-wells as described by Najafizadeh et al. [9]. The low-voltage current source is formed by LDMOS transistors available in-process, also as described by Najafizadeh et al. [9].

3.3. Flying Capacitor Network. The flying capacitor network [10–12] used for sampling the analog input is implemented as shown in Figure 7. The main components of the circuit include sampling capacitors, C_S , holding capacitor, C_H , and a general purpose high-Z input op amp within a switched capacitor configuration. This circuit incorporates calibration and charge cancellation schemes in order to eliminate pedestal effects from parasitic capacitors and charge injection from the control switches. The array of feedback capacitors used for the op amp provides programmable gain (see Figure 8). During the channel calibration, the channel gain is programmed from -0.6 to -10 V/V using the desired combination of the gain switches. As discussed earlier, the switches are set by the shift register illustrated in Figure 5. An internally generated reference voltage, V_{REF} , is applied to

FIGURE 7: Schematic of the flying capacitor network.

FIGURE 8: Programmable gain circuitry in the flying capacitor network.

the op amp to set the input common-mode voltage. Op amp offset voltage correction is implemented using an adjustable reference voltage, V_{COR} . The V_{COR} voltage is generated by a voltage DAC that is initialized using a serially loaded shift register during the calibration/setup of the channel. When the reference voltages are equal, the op amp's offset is compensated. Using a value for V_{COR} that is different from the reference voltage, V_{REF} , enables offset correction for the entire channel.

The general purpose op amp [13] provides the channel gain and is also employed as a level shifter to match the input range of the ADC. Since the ADC has 12 bits of resolution, the op amp is designed to provide at least 80 dB gain, low noise, and low offset drift. The schematic of the op amp is depicted in Figure 9. The amplifier senses input voltages near the lower supply and also provides rail-to-rail output voltage swing. The output stage is based on the topology presented in [14] and provides good drive capability while using relatively small transistors. Measurement characterizations of this op amp indicate that it provides a stable DC open-loop gain of

80 dB and gain-bandwidth product of 4 MHz across a wide temperature range of -180°C to 125°C [13]. Preliminary proton radiation testing induced negligible variation in its performance [15].

3.3.1. Timing Control and Operation. The switches control the different modes of operation of the flying capacitor network. Figure 10 provides the control signals that coordinate the switching. All switches employ transmission gates to reduce charge injection and eliminate threshold voltage effects on logic levels inherent to nMOS-only or pMOS-only gates.

When the circuit's operation begins with calibration mode, the sampling and holding capacitors are reset to 0 V and the op amp is biased in unity-gain mode. Switches S_{CAL} and S_3 are closed during this stage. The cross-coupling of the sampling capacitors aids in cancellation of charge from parasitic capacitance. Also, the hold capacitor (C_f) has its bottom plate connected to the output of the op amp rather than the inverting input, thereby reducing parasitic capacitance at the input of the op amp.

Calibration is followed by a calibration-hold stage (Figure 11). This phase incorporates a prehold phase for charge cancellation. Further, the switches have a "break-before-make" action which is essentially nonoverlapping control signals that aid in discharging the parasitic capacitors. The order of switching begins with the opening of the S_{CAL} switch and the closing of the S_2 switch. With switch S_2 closed, harmless discharge paths are formed for the parasitic capacitors found at the bottom and top plates of the sampling capacitors, whereas the sampling capacitors retain their charge. After the parasitic discharge is complete, switch S_3 opens to place C_f in the op amp's feedback loop.

FIGURE 9: Schematic of the general purpose op amp [13].

FIGURE 10: Coordination of timing signals for the flying capacitor circuit.

Then switch S_4 closes which allows charge from the sampling capacitors to move to the feedback capacitor. As a result, now the output of the op amp reflects the op amp's offset voltage.

After a cycle of calibration and hold, the circuit enters the sampling phase in which the switches S_1 and S_3 are closed and all others are opened. Figure 7 illustrates this phase. The sampling capacitors charge to the bridge's differential output

voltage while the offset correction capacitor, C_{COR} , is reset. Next, the circuit enters the hold stage (Figure 12), in which the parasitic charges are canceled in the pre-hold phase and followed by the transfer of charge from the sampling to the holding capacitor, C_f . Also, C_{COR} is connected to a voltage equal to V_{REF} so that the voltage across the capacitor C_{COR} is equal to the op amp's offset voltage. With this correction voltage applied to the op amp's inverting input, the output voltage during the hold stage is $V_{REF} - V_{CF}$, where V_{CF} is the sampled analog input. Thus, the flying capacitor circuit performs analog sampling and also incorporates offset and parasitic charge cancellation.

The V_{REF} voltage is internally generated and V_{COR} is set during channel calibration. The switched capacitor's control signals, the 6-phase clocks, are brought into the chip from external sources. The next version of this chip includes a 6-phase clock generation circuit that provides the necessary control signals from a single input clock that is synchronized with the chip's master clock. This improves the signal integrity by minimizing crosstalk, substrate noise injection, and IR drop from long routes. It also reduces the required number of external pins. The 6-phase clock generator circuit halves the input clock frequency and employs it as an additional phase reference to generate the required control signals. Current-starved inverter delay cells [16] are used to provide the required delays for the non-overlapping clock phases.

In order to match the output range of the flying capacitor stage with the input range of the ADC, an op amp-based level shifter is employed. Figure 13 shows the two-stage level shifter that uses the general purpose high- Z input op amp

FIGURE 11: The flying capacitor network in charge cancellation mode in “pre-hold phase”.

FIGURE 12: The flying capacitor network in hold phase.

of Figure 9. The first stage sets the required dc bias for the next stage such that the output of the second stage is centered about 0.6 V. This op amp configuration also increases the gain by a factor of two. A simplified schematic of the full universal channel is illustrated in Figure 13.

3.4. Multichannel Wilkinson ADC. The universal channel is interfaced to one of the 16 channels of the Wilkinson ADC [6]. The architecture of the Wilkinson ADC is based on [17]. The functional block diagram of the ADC is provided in Figure 14. The main components of the ADC include a single ramp generator and a single 12-bit Gray code counter that are shared across the multiple channels, thereby reducing the total power consumption. Additionally, an auto-zeroing comparator is integrated within each channel. This low-power comparator also incorporates the analog sampling function within the ADC.

3.4.1. Timing Control and Operation. To function properly, the ADC depends on precise synchronization of various

signals that control the key components of the ADC. The clock to the Gray code counter is supplied via a low-voltage differential signaling (LVDS) link [18] to minimize the noise injected into the system by the clock. Figure 15 illustrates the timing sequence of the control signals for a conversion cycle. The analog signal from the universal channel is input directly to the comparator.

The conversion begins with a sampling phase, wherein the analog input is sampled while also auto-zeroing the comparator's offset. Signals *ICS* and *AZ* control this phase. The integration capacitor in the ramp generator is also reset during this phase by the *RAMP_FB* signal. Next, the comparator is connected to the ramp generator by the *RAMP_CONNECT* signal. The actual start of conversion begins with the release of the *RAMP_FB* switch and the start of the counter by the *COUNTER_ENABLE* signal. This generates a ramp voltage that linearly varies from 0 to 1.2 V that is proportional to the digital count. When the sampled voltage becomes equal to the ramp voltage, the comparator trips. The value of the counter is stored on latches for reading out the data. During the next sampling/auto-zero phase, the stored data is moved to another set of storage latches by the *REFRESH* signal and the first set of latches are reset by the *RESET* signal, thus preparing for the next conversion. Multiple universal channels can be connected to the ADC and the data can be read out using the channel select signals.

Since the flying capacitor network produces a discrete time output that is valid only during the hold phase (Figure 12), proper synchronization is essential to ensure that the ADC samples reflect the sensor output. This is accomplished by generating all the control signals from the same master clock through clock dividers. Thus the ADC's input sampling signal, *ICS*, is enabled only when the flying capacitor's *SCOR* signal is high.

4. Discussion

Designing circuits for extreme environment operation demands implementation of numerous design strategies at

FIGURE 13: Simplified schematic of the Universal Channel along with the control blocks.

FIGURE 14: Functional block diagram of Wilkinson ADC.

the system level as well as at the individual circuit level, along with special layout techniques. The individual circuits in the channel are designed to operate reliably across the required temperature range of -180°C to 125°C . The choice of bias circuits is critical for the circuit's performance across

temperature. This mixed-signal system includes a constant-current reference and a constant-inversion coefficient (IC) [19] current reference [20] for providing the bias currents. Using the constant-IC current reference to bias the op amps helps maintain a constant MOSFET IC across temperature,

FIGURE 15: Timing diagram for the ADC.

FIGURE 16: Die Photo of the chip ($6 \times 6 \text{ mm}^2$).

thus minimizing performance variations. Circuits such as the ADC's comparator and LVDS link that require a constant bias current employ the constant-current reference circuit. The next version of this chip also includes a temperature compensation scheme within the ADC that maintains the accuracy across temperature.

Reliability and device life time depend on the operating temperature and tend to degrade at low temperatures. SiGe HBTs offer better performance across temperature and ionizing radiation when compared to CMOS devices [21]. Further, pMOS transistors exhibit better performance at cryogenic temperatures than nMOS transistors [22]. Thus, circuits designed with only pMOS transistors and HBTs operate more reliably across extreme environmental conditions. The reliability of CMOS circuits is improved by using longer channel length devices that reduce the increase

FIGURE 17: Output voltage versus resistance of the sensor at various temperatures. (quarter-bridge configuration, gain = -20 V/V) [5]. FIGURE 18: Output voltage versus resistance of the sensor at various temperatures. (quarter-bridge configuration, gain = -10 V/V).

in substrate current at low temperatures caused by the hot carrier effect [23]. To meet the device lifetime reliability specification in CMOS circuits for this work, all the 3.3-V powered nMOS transistors have a channel length $\geq 1 \mu\text{m}$.

Radiation effects include total-ionization dose (TID), single-event upset (SEU), and single-event induced latch-up (SEL) [24]. In order to mitigate SEU, the digital circuits in the universal channel employ radiation-hardened-by-design (RHBD) cells such as DICE flip-flops and latches [25]. For the ADC's low-power Gray code counter (where DICE cells could not be used), local redundancy with voting logic is implemented to provide SEU tolerance. The TID effects are mitigated by layout techniques. The nMOS and pMOS transistors are surrounded by guard rings to alleviate the TID-induced leakage currents. The guard rings, along with n-well and substrate contacts, provide isolation to different transistors as well as circuits. This offers latch-up immunity and lower substrate noise coupling. Use of deep trench

isolation (DTI) also enhances the latch-up immunity of the circuits.

The low-power ADC also incorporates system-level SEL detection and mitigation using a radiation aware power management scheme. This scheme includes a voltage regulator that provides the power supply for the ADC's digital section. In the event of an SEL, the supply voltage is automatically collapsed and then restored, resetting the digital blocks. Therefore, SEL mitigation is implemented at the system level.

Electromigration is another failure mechanism that is addressed, wherein at high-current densities and temperatures, interconnects experience degradation due to the transport of metal ions [26]. The selected process's electromigration rules that govern current density limit, wire width, and minimum required contacts are strictly followed to improve the reliability and the life time of metal connections.

5. Measurement Results

Previous versions of the universal channel along with the 12-bit 16-channel Wilkinson ADC were fabricated and verified in a 0.5- μm SiGe BiCMOS process. The die photo of the most recently tested circuits is shown in Figure 16. The layout is designed to minimize noise and crosstalk in the chip. The analog and digital sections have separate power supplies and are isolated by guard rings. The high-frequency clock signal for the ADC is supplied as a complementary signal and is well shielded from other signals. Also, the bottom plate of the op amp's feedback capacitors in the flying capacitor circuit is connected to the output of the op amp so that the substrate-to-bottom plate crosstalk is reduced due to the low output impedance of the op amp.

A multilayer test board is designed to test the universal channel and the ADC. The control signals are generated from a master clock using an onboard reprogrammable FPGA. Separate ground planes and routing layers are provided for the analog and digital signals. Variable resistors are used as an input to the channel and the output of the ADC is recorded using a National Instruments data acquisition interface card [27].

The measurements of the channel are taken at different temperatures across the range of -180°C to $+125^\circ\text{C}$. The output voltages of the channel, depending on the resistance of the sensor in the quarter-bridge configuration at various temperatures and gains, are shown in Figures 17, 18, and 19. Depending on the gain setting of the channel, the system can measure a maximum resistance change of approximately $67\ \Omega$, and a minimum change of less than $1\ \Omega$.

Figure 20 provides the output voltage of the channel across temperature. The variation in the output voltage results from the bridge becoming unbalanced when the resistance of the sensor remains unchanged at room temperature while the rest of the bridge varies with temperature.

The operation of the on-chip stimulus current is verified across temperature. The output current is measured by sweeping the current DAC over the 8-bit range. Figure 21 depicts the measured stimulus current at $+27^\circ\text{C}$ and -174°C . The simulation data at $+27^\circ\text{C}$ is also shown in this figure.

FIGURE 19: Output voltage versus resistance of the sensor at different gains. (quarter-bridge configuration, temp = -180°C).

FIGURE 20: Output voltage versus temperature. (quarter-bridge configuration, gain = $-10\ \text{V/V}$).

FIGURE 21: Measured and simulation data of the positive stimulus over the current-DAC 8-bit range [5].

FIGURE 22: Measured output from universal channel at room temperature with manually adjusted sensor.

FIGURE 23: Measured output from universal channel at -174°C with manually adjusted sensor.

A potentiometer is used as a quarter bridge sensor to interface with the channel. This potentiometer is manually adjusted to represent a dynamically changing sensor. Figures 22, 23, and 24 illustrate the measured analog output of the channel before it is applied to the ADC. During the five seconds that these images were captured, the potentiometer was manually adjusted to provide an oscillating sensor input signal. As seen in the figures, the channel correctly samples the sensor as the resistance of the potentiometer is adjusted. Across the wide temperature range of $+125^{\circ}\text{C}$ to -174°C , the universal channel demonstrates full sampling functionality. The channel is designed for low-speed sensors that support input signals up to 200 Hz. The sampling frequency of the channel is approximately 20 kHz in these figures. Characterization of the Wilkinson ADC shows the differential-non-linearity (DNL) to be less than ± 0.5 LSB across the temperature range [6].

Table 1 provides the estimated power consumed by the individual blocks and the total estimated power consumption of one universal channel. The bridge configuration circuits include the voltage DAC and three shift registers used for the calibration and configuration of the channel. It is evident that the input stage of the channel dominates the total power consumed. This is set by the bias requirements of the sensor.

In the final version of the universal channel and Wilkinson ADC, additional wide temperature testing of the circuits is expected to demonstrate full operation.

FIGURE 24: Measured output from universal channel at 125°C with manually adjusted sensor.

TABLE 1: Estimated power consumption.

Circuit Block	Simulated Average Power (mW)
Wheatstone Bridge	12–384 (204 typ.)
Current DAC	4
High-Voltage Level Shifter	1.2
Bridge Configuration circuits	4
Flying Capacitor Network	2.2
Level Shifting Buffer	3
ADC	≈ 1.1 per channel
Total Power	28–400 (220 typ.)

6. Conclusion

The design of the instrumentation channel requires many novel techniques in order to make it stable and reliable across a wide temperature range. This paper demonstrates the operating principles and experimental results of a channel which can be used in sensor data acquisition applications down to cryogenic temperature. In the future, the instrumentation channel will be integrated into a 16-channel Remote Electronics Unit Sensor Interface (RSI) ASIC for use in space applications.

Dedication

This paper is dedicated to the memory of Hung Hoang, Department of Electrical Engineering, University of Arkansas, Fayetteville, who contributed to the development of this work.

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