Research Article

Architecture and Implementation of Fading Compensation for Dynamic Spectrum Access Wireless Communication Systems

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This paper proposes an efficient architecture and implementation of fading compensation dedicated to dynamic spectrum access (DSA) wireless communication. Since pilot subcarrier arrangements are adaptively determined in wireless communication systems with DSA, the proposed architecture employs piecewise linear interpolation to the channel response estimation for data subcarriers in order to increase the channel estimation accuracy. The fading compensation for an orthogonal frequency-division multiplexing (OFDM) symbol is performed within the time for one OFDM symbol to make increase of latency smaller. The proposed architecture guarantees real-time processing with 76 MHz or higher clock frequency. The FPGA implementation of the proposed architecture occupies 1,577 slices and works up to 121 MHz.

1. Introduction

In ambient information society, the ICT infrastructure interacts with each person in order to make the one's surrounding space more comfortable. In this kind of interaction, various types of information are exchanged, ranging from small size such as the control data of air conditioners and room lights to large size of data like video streaming.

Here, wireless mesh networks that use unlicensed radio frequency bands have been the focus of attention as one of the *ambient networks*. Among various wireless mesh networks, IEEE 802.11 WLAN series and ZigBee using carrier sense multiple access with collision avoidance (CSMA/CA) are expected to achieve popularity due to their capabilities to interconnect. However the following problem arises by using the technique of CSMA/CA. Let us assume that there are two nodes, *A* and *B*, that use IEEE 802.11g [1] for the former and ZigBee [2] for the latter, and the radio resource that *A* has requested partially overlaps with that of *B*. In this situation, even if the node *B* uses far fewer radio resources than node *A* requests, the node *A* judges that the band are not available in case the node *B* performs transmission and does not start to transmit data despite the presence of many unused radio

resources. This causes the degradation of total transmission performance of the heterogeneous wireless infrastructure.

In order to solve this problem, the so-called *cognitive radio systems* have been proposed [3, 4], which introduce various techniques with dynamic spectrum access (DSA). These techniques are based on the concept of exploiting spatial and temporal spectrum white space. Among them, [4] proposed dynamic subcarrier selection technique based on CSMA/CA with orthogonal frequency division multiplexing (OFDM). In this technique, wireless nodes select the radio resources being used in the units of subcarriers by referring to the result of subcarrier level carrier sensing as shown in Figure 1. This adaptive subcarrier selection technique enables transmission by utilizing unused subcarriers even if there are occupied spectrum components for other transmissions.

Generally in wireless communication, received signals are distorted by fading and noise. Therefore, receivers need to compensate the distortion in order to decode data correctly. If the wireless communication is based on OFDM, known training signals called pilots are utilized in order to estimate the channel response and compensate the distortion [5]. In the IEEE 802.11g, four of the fixed subcarriers are utilized for pilot signals, and the channel responses of data subcarriers

FIGURE 1: Mapping.

are estimated by interpolating the channel responses of pilot subcarriers [6].

However it is decided adaptively which subcarriers are utilized as data subcarriers or pilot subcarriers in target wireless communication with DSA [7]. Figure 2 outlines the arrangements of pilot subcarriers for IEEE 802.11g and DSA [7]. Although increasing the number of pilot subcarriers enables channel responses to be accurately estimated, it also degrades the data rate. Therefore, it is necessary to estimate the channel responses for data subcarriers by interpolation with the estimated channel responses for pilot subcarriers in order to accurately estimate the channel responses with limited pilot subcarriers. Since the interpolation function for communication differs from the functions for other communications, a dedicated channel compensation circuit for DSA is necessary to accomplish high-speed operation to determine both decisions of interpolation function and fading compensation.

Motivated by these tendencies, this paper describes an efficient architecture and implementation of fading compensation for an OFDM baseband transceiver with DSA. Piecewise linear interpolation is utilized in order to estimate the channel responses for data subcarriers by using the channel responses for pilot subcarriers.

2. OFDM Wireless Communication with Dynamic Spectrum Access

This paper assumes that DSA wireless communication with subcarrier selection-type CSMA/CA [4] is employed. Table 1 summarizes the system parameters for the target DSA wireless communication system. This system is designed by taking into account its compatibility with OFDM in IEEE 802.11a [8] and IEEE 802.11g [8]. In this condition, FFT size and the maximum bandwidth are twice as large as those of IEEE 802.11g. However the number of subcarriers used for data transmission is the same as that for IEEE 802.11g in order to avoid exclusive use of radio resources.

Figure 3 shows the OFDM frame structure. The OFDM frame consists of a physical layer convergence protocol (PLCP) preamble, which is used for synchronization detection, header symbols, that is, coded communication parameters, and data symbols including transmission data. The PLCP preamble is made up of a short preamble for timing detection and a long preamble for phase compensation. The

TABLE 1: System parameters.

No. of efficient subcarriers	48
No. of pilot subcarriers	4
FFT size	128
Max bandwidth	40 MHz
Symbol length	4 μ s
Cycle prefix length	32 samples
Carrier modulation	BPSK, QPSK, 16QAM, 64QAM
Coding rate	1/2, 2/3, 3/4

short preamble is a ten times iteration of the reference pattern, and one reference pattern is 32 samples. In the receiver side, symbol timing detection is performed by using correlation between the reference pattern and the received short preamble signal. The long preamble signals are for phase compensation, whose amplitude and phase are known. The header symbol indicates the used modulation mode and the length of data symbols.

Figure 4 shows a block diagram of the target OFDM baseband transceiver with DSA [7]. In the transmitter, the first process is forward error correction (FEC), which adds redundant data to input data so that the amount of data is set according to the coding rate. Interleaving is the second process, and it reorders data to avoid burst error. Modulated data are assigned to subcarriers in mapping process based on information on subcarrier assignment obtained from subcarrier level sensing. The mapping function is given by

$$idx = M(p), \quad (1)$$

where p and idx are subcarrier indices before and after mapping, respectively. While idx ranges from 0 to 127, p ranges from 0 to 51. M is a transform function based on subcarrier information obtained from subcarrier level carrier sensing. After mapping, IFFT transforms the frequency domain data to the time domain data. Here the number of data from mapping to IFFT is 52, and the size of IFFT is 128. Mapping should pass dummy data (i.e., 0's) to IFFT for 76 (= 128 - 52) unused subcarriers. The increased number of input data to IFFT increases the computational cost to be more than that for conventional IEEE 802.11g. A cycle prefix (CP) whose length is greater than the channel delay spread is added prior to transmission by copying part of the IFFT output to mitigate the effects of intersymbol interference. Finally, through digital-analog converter (DAC), the samples are passed to a radio frequency (RF) unit that amplifies the signals and upconverts them to the required center frequency.

The receiver operates in reverse to the transmitter. In the receiver, the first process is timing synchronization. The timing synchronization process detects the beginning of a frame by calculating the correlation between the sequential data from the analog-digital converter (ADC) and the short preamble sequence, which is the known pattern signal. After symbol timing is synchronized, the added CP is removed, and FFT transforms the time domain data to the frequency domain data. Next, the demapping process, which is the reverse operation of mapping, selects 52 outputs of FFT

FIGURE 2: Pilot subcarrier arrangement.

FIGURE 3: The OFDM frame structure.

based on subcarrier information from 128 subcarriers. In other words, the demapping process discards many data signals. The equalization process eliminates the effect of the transmission channel by using the channel transfer function estimated from long training sequences. Finally, Viterbi decoding process after demodulation and deinterleaving outputs the reconstructed version of the original data.

3. Fading Compensation

The received signals through the wireless channel are distorted by fading or noise as shown in Figure 5. Therefore fading compensation, which estimates and compensates received signal distortion, is necessary in order to accurately decode the received data.

This section describes the fading compensation for DSA we propose after explaining an example of preamble-based fading compensation [6] for OFDM transmission.

3.1. Preamble-Based Fading Compensation. Figure 6 shows an overview of preamble-based fading compensation. After FFT, received preamble signals R_{pr_m} are expressed as

$$R_{pr_m} = a_{pr_m} H_m + Z_m \quad (0 \leq m \leq M-1), \quad (2)$$

where m is the index of used subcarriers, a_{pr_m} is the known preamble signal, and H_m and Z_m represent ideal channel response and noise channel response, respectively [9]. Received preamble signal R_{pr_m} is compared to known

signal a_{pr_m} , and estimated channel response $\hat{H}_m$ is calculated as

$$\hat{H}_m = \frac{R_{pr_m}}{a_{pr_m}} = H_m + \frac{Z_m}{a_{pr_m}} \quad (0 \leq m \leq M-1). \quad (3)$$

The primary compensated signal $\hat{a}_m$ is calculated by using $\hat{H}_m$:

$$\hat{a}_m = \frac{R_m}{\hat{H}_m} \quad (0 \leq m \leq M-1), \quad (4)$$

where R_m is the received signal.

Next, secondary compensation with pilot subcarriers is carried out to cope with microvariations in channel responses in one OFDM symbol time. The estimated microvariation in channel response $\hat{P}_{d_m}$ is expressed as

$$\hat{P}_{d_m} = F(m, l(n), \hat{a}_{pi,l(n)}), \quad (5)$$

where m is the index of data subcarriers, $l(n)$ is the index of pilot subcarriers and $\hat{a}_{pi,l(n)}$ is that of the estimated microvariation for pilot signals, and F is their interpolation function. The secondary compensated signals $\hat{\hat{a}}_{d_m}$ are given by

$$\hat{\hat{a}}_{d_m} = \frac{\hat{a}_{d_m}}{\hat{P}_{d_m}} \quad (0 \leq k \leq M-L-1), \quad (6)$$

where L is the number of pilot subcarriers.

3.2. Fading Compensation for DSA. In the IEEE 802.11g, four of the subcarriers are dedicated to pilot signals in order to make coherent detection robust against frequency offsets and phase noise. These pilot signals are placed in ideal locations [10]. Therefore, the arithmetic mean can be utilized as the function to estimate channel microvariations. However the arithmetic mean is not always efficient for OFDM with DSA since DSA utilizes different distributions of pilot subcarriers in different communications. This paper adopts piecewise linear interpolation as the interpolation function to estimate the channel responses for microvariations and evaluates the efficiency by comparing with the arithmetic mean. The details are described in the next subsection.

FIGURE 4: Block diagram of OFDM baseband transceiver with DSA.

FIGURE 5: Example of received signal distortion.

3.2.1. Microvariation Estimation with Piecewise Linear Interpolation. The estimated microvariation for the target subcarrier is calculated by linear interpolation between the estimated microvariation values for the left and right pilot subcarriers shown in Figure 7. The proposed interpolation function is given by

$$F(m, \hat{P}_{idx_left}, \hat{P}_{idx_right}) = \frac{(idx_right - m) \hat{P}_{idx_left} + (m - idx_left) \hat{P}_{idx_right}}{idx_right - idx_left}, \quad (7)$$

where m is the index of the target subcarrier, idx_left and idx_right correspond to the index of the left and right pilot subcarriers, and $\hat{P}_{idx_left}$ and $\hat{P}_{idx_right}$ are the estimated variation values for the left and right pilot subcarriers, respectively. $\hat{P}_{idx_left}$ and $\hat{P}_{idx_right}$ are expressed as

$$\begin{aligned} \hat{P}_{idx_left} &= \frac{\hat{a}_{idx_left}}{a_{idx_left}}, \\ \hat{P}_{idx_right} &= \frac{\hat{a}_{idx_right}}{a_{idx_right}}. \end{aligned} \quad (8)$$

TABLE 2: Parameters for Rayleigh fading model.

No. of multipath	32
Delay spread	50 ns
Delay attenuation model	Exponential decay
Maximum Doppler frequency	20 Hz
Variation period of multipath	0.025 s (40 Hz)
Frequency offset	0.03 Hz/symbol

TABLE 3: Conditions for preliminary experiment.

No. of efficient subcarriers	52/128 (including 4 for pilot)
Modulation	BPSK, QPSK
No. of processed OFDM symbol	Two million
Physical layer frame size	1500 byte
SNR	0~25 dB, 5 dB step
Channel model	Rayleigh fading (Table 2)

3.2.2. Preliminary Experiment. The preliminary experiment was carried out through software simulation to confirm that piecewise linear interpolation had an advantage over the arithmetic mean in respect to the Bit Error Rate (BER). Software with floating points emulates the behavior of the transceiver, but symbol timing error is not taken into consideration.

The Rayleigh fading model was used in the software simulation whose parameters are summarized in Table 2, and simulation conditions are listed in Table 3. Figure 8 plots the experiment results for BER, which is generally used as an indicator of the channel estimation accuracy. This indicates that piecewise linear interpolation is more efficient than the arithmetic mean, which is generally utilized in the 802.11a/g PHY. Therefore, we adopted piecewise linear interpolation to estimate microvariations.

4. Proposed Architecture of Fading Compensator for DSA

Figure 9 is a block diagram of the proposed fading compensator architecture. The proposed architecture consists of channel estimator, linear interpolator, coefficient calculator, linear projector, and five memories.

First, the coefficient calculator stores idx_left and idx_right obtained from mapping information in the idx_left

FIGURE 6: Preamble-based fading compensation.

FIGURE 7: Microvariation estimation with piecewise linear interpolation.

FIGURE 8: Preliminary experiment results.

memory and *idx_right* memory, respectively, while receiving PLCP preamble signals. Next, the primary compensated signals are input and stored in the data buffer. After all signals corresponding to one OFDM symbol have been stored, one data at a time is read from the data buffer. If the data is

FIGURE 9: Block diagram of proposed fading compensator.

for the pilot, the channel estimator calculates the estimated microvariation value for the pilot, and the value is written to both left and right coefficient memories. After all estimated microvariation values for the pilots have been obtained, the Linear interpolator calculates each estimated microvariation value for data by piecewise linear interpolation with the distance between the target data subcarrier and two adjacent pilot subcarriers. Finally the secondary compensated signals for data $\hat{a}_{d_m}$ are calculated from the primary compensated signals and estimated microvariation values for data in the Linear projector.

4.1. Channel Estimator. The block diagram of the channel estimator is shown in Figure 10.

This block treats $\hat{P}_{pi,l(n)}$ as amplitude variation α and phase shift $\Delta\theta$ in a polar coordinate system in order to enable microvariations to be easily calculated. Therefore, received signals (I, Q) in a rectangular coordinate system are transformed to (R, θ) in a polar coordinate system in this block. The transformation from a rectangular coordinate to a polar coordinate is given by

$$R = \sqrt{I^2 + Q^2},$$

$$\theta = \begin{cases} \tan^{-1} \frac{Q}{I} & (Q \leq I), \\ \frac{1}{2}\pi - \tan^{-1} \frac{I}{Q} & (Q > I). \end{cases} \quad (9)$$

FIGURE 10: Channel estimation block.

The input size of the $\tan^{-1}$ function is restricted to 11-bit by comparing I with Q so that the $\tan^{-1}$ function can be constructed with a lookup table (LUT). All modules in this block adopt a pipelined architecture, and the square root and divider both take seven cycles each. Performing abs and square add take 1 cycle. As a result, the latency of this block is 15 cycles.

4.2. Coefficient Calculator. The two data idx_right and idx_left can be calculated with mapping information only. Therefore, the coefficient calculator obtains idx_right and idx_left and stores them in memories while receiving long preamble signals since the mapping information cannot be changed in a physical layer (PHY) frame.

The mapping information has two 128-bit data, where each bit corresponds to each subcarrier. The first data are called a utilization mask and indicate which subcarriers are used (1)/unused (0). The second are called a pilot mask and indicate which subcarriers are pilot subcarriers (1) or not (0). Figure 11 is the block diagram of the coefficient calculator. This block consists of subcarrier index generator, subcarrier type checking block, and coefficient generator. The subcarrier index generator and the coefficient generator are created by 7-bit counter, and the subcarrier type checking block is based on a barrel shifter. The two memories that have write access from this block are dual port RAMs since these memories also have read access from the linear interpolator. How idx_right and idx_left are determined by using these data is described hereinafter.

FIGURE 11: Block diagram of coefficient calculator.

FIGURE 12: Contents of memory after step 1.

- (1) First, the 128-entry memory called the Right coefficient memory is initialized to 1's. Next, the utilization and pilot masks are forward scanned with the subcarrier index generator and subcarrier type checking block. The contents of the Right coefficient memory remain unchanged until the first detection of a pilot subcarrier. When a pilot subcarrier is detected, the corresponding entry in the right coefficient memory is changed to 0, and then incremented values are written to the memory until the next pilot subcarrier is detected. Figure 12 shows the contents of memory after this step has finished.
- (2) Since only $\hat{P}_{idx_right}$ is utilized for the data subcarriers that are at the right of the last pilot subcarrier, corresponding entries for the Right coefficient memory to the data subcarriers are overwritten by zero after step

1 has finished Figure 13 shows the contents of memory after this step has finished.

- (3) The left coefficients are determined in the same way as those in step 1 with backward scanning, and they are stored in the left coefficient memory.
- (4) The entries corresponding to the subcarriers at the left of the first pilot subcarrier are overwritten by zero in the same way as that in step 2.

Figure 14 shows the contents of memories after all steps are executed.

This step includes forward and backward scanning of mapping information, and each scan takes 128 cycles since utilization of the subcarrier index, f , as memory read address enables one cycle reading of pair coefficients from the Left and Right coefficient memories. The execution cycles of steps 2 and 4 are determined according to the pilot subcarrier arrangement. The maximum execution cycle is 129 cycles when only one of 128 subcarriers is dedicated to the pilot

FIGURE 13: Contents of memory after step 2.

FIGURE 14: Contents of memory after coefficient calculation.

signal. The total execution cycles is at most 387 cycles since one cycle initialization and one cycle termination process are included.

4.3. Linear Interpolator. Figure 15 shows the block diagram of the linear interpolator. This block has four multipliers and three adders, and all of them have registered outputs. Therefore the linear interpolator has ten pipeline stages since this block has a divisor that has seven pipeline stages.

The linear interpolator performs two functions. One is preparing the left and right estimated microvariation values $\hat{P}_{idx_left} = (\hat{a}_{idx_left}, \hat{\theta}_{idx_left})$ and $\hat{P}_{idx_right} = (\hat{a}_{idx_right}, \hat{\theta}_{idx_right})$. The other is calculation of the estimated microvariation value for data subcarriers $\hat{P}_{d_m} = (\hat{a}_{d_m}, \hat{\theta}_{d_m})$.

First, the estimated microvariation values for pilot subcarriers are written in the left estimated microvariation memory, which is the output of the channel estimator. The entries corresponding to the subcarriers on the left of the first pilot subcarrier are written as zeroes. The entries for the other subcarriers are written as the estimated microvariation values for the nearest pilot subcarrier on the left. After all of the 128 entries have been written to, the right estimated microvariation values are obtained in the same way as the left estimated microvariation values by backward-scanning the left estimated microvariation memory and pilot mask. Each of the estimated microvariation values for the data subcarriers is calculated by linear interpolation (7) with the left and right coefficients and the left and right estimated microvariation values.

These operations are executed at 285 cycles including 128 cycles for writing, 128 cycles for scanning, 10 cycles for microvariation calculations, and 19 cycles for the initializing and terminating processes.

Figure 16 shows how to utilize the left and right estimated value.

4.4. Linear Projection Block. The secondary compensation is carried out by linear projection operation with the estimated microvariation value in the rectangular coordinate system. The linear projection operation is given by

$$\begin{pmatrix} \hat{I} \\ \hat{Q} \end{pmatrix} = \frac{1}{a} \begin{pmatrix} \sin(-\Delta\theta) & -\cos(-\Delta\theta) \\ \cos(-\Delta\theta) & \sin(-\Delta\theta) \end{pmatrix} \begin{pmatrix} I' \\ Q' \end{pmatrix}. \quad (10)$$

TABLE 4: Maximum execution cycles.

Blocks	Maximum execution cycles
Channel estimation	15
Coefficient calculator	387
Linear interpolation	285
Linear projection	4

TABLE 5: Implementation result.

Occupied slice	1,577/14,336 (11%)
Used SRAM	234 kbits
Max frequency	112 MHz

The block diagram of linear projection block is shown in Figure 17. This block can input data every cycle and table access, and multiplication and addition take 1 cycle. As a result, the latency of this block is 4 cycles.

4.5. Execution Cycles and Operation Frequency. Table 4 summarizes the maximum execution cycles for each block in a fading compensation circuit.

When a block needs to terminate its process within N OFDM symbol time (one OFDM symbol time is $4 \mu s$) during real-time operation, the minimum operation frequency, F_{min} , for real-time operation is given by

$$F_{min} = \frac{n}{N \cdot (4.0 \times 10^{-6})}, \quad (11)$$

where n is the number of execution cycles.

Since it is necessary for the coefficient calculator to terminate its process within two OFDM symbol times to receive all long preamble signals, the minimum operation frequency for real-time operation is 48.3 MHz ($= 2/(387 \times (4.0 \times 10^{-6}))$). The execution time for the channel estimator, linear interpolator, and linear projector is 304 cycles for an OFDM symbol since they need to perform their operations for the same OFDM symbol. Therefore the minimum operation frequency is 76.0 MHz for these blocks.

As a result, the minimum operation frequency for the proposed fading compensator is 76.0 MHz since the minimum operation frequency of blocks excluding the coefficient calculator is 76.0 MHz and the minimum operation frequency of the coefficient calculator is 48.3 MHz.

5. FPGA Design of Fading Compensator

5.1. Implementation Result. The proposed architecture of the fading compensation circuit has been implemented in an FPGA (Xilinx Virtex-II xc2v3000), and Table 5 summarizes implementation results. This result surpasses the 76.0 MHz demanded for real-time operation.

5.2. Performance Evaluation. We simulated the performance of this fading compensator without Viterbi decoding under the conditions listed in Table 6 to confirm the behavior

FIGURE 15: Block diagram of linear interpolator.

FIGURE 16: Left and right estimated values.

FIGURE 18: Mapping condition.

FIGURE 17: Linear projection block.

FIGURE 19: SNR versus BER.

TABLE 6: Simulation conditions.

No. of efficient subcarriers	52/128 (including 4 for pilot)
Modulation	BPSK, QPSK
No. of Processed OFDM symbol	Two million
Physical layer frame size	1500 byte
SNR	0~25 dB, 5 dB step
Channel model	Rayleigh fading (Table 2)

of the proposed architecture. Figure 18 shows the mapping condition in this simulation.

Figure 19 plots the simulation results for BER with hardware implementation. These results show that the hardware implementation achieves comparable performance to the 802.11a-based system without the diversity reported in [11] even though our architecture utilizes a discontinuous

spectrum, and its performance is almost the same as the theoretical performance.

6. Conclusion

In this paper, a hardware architecture of fading compensation circuit for DSA was proposed. The proposed architecture adopted piecewise linear interpolation in order to accurately estimate channel responses for data subcarriers. Fading compensation for an OFDM symbol was executed in one OFDM symbol time in order to make increase of latency

smaller. The results of FPGA implementation indicated that the proposed circuit occupied 1,577 slices and achieved 112 MHz operation frequency which overcame the 76.0 MHz demand for real-time operation on a single chip.

Future work is the performance evaluation of the OFDM transceiver with DSA combined with the proposed fading compensator.

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