Research Article

Improved Quantization Error Compensation Method for Fixed-Width Booth Multipliers

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A novel quantization error (QE) compensation method is proposed in design of high accuracy fixed-width radix-4 Booth multipliers, which will effectively reduce the QE and save the area of multipliers when they are employed in cognitive radio (CR) detector and digital signal processor (DSP). The truncated partial-products of the proposed multipliers are finely divided into three sections: reserved section, adaptive compensation section, and constant compensation section. The QE compensation carries of the multipliers are generated by applying probability estimation based on a shrunk minor truncated section which is a combination of the constant compensation and adaptive compensation. The proposed compensation method not only reduces the QE of the fixed-width Booth multipliers, but also avoids the exhaustive computing resources (time and memory) during getting the compensation carries by statistical simulation. The proposed method can achieve higher accuracy than the existing works under the same area and power budgets. Simulation and experiment results show that the improved compensation method has the minimum power-delay products compared with the existing methods under the same area and can save up to 30% area for realization of full-width radix-4 Booth multipliers.

1. Introduction

The fixed-width multipliers have been widely used in the design of digital signal processor (DSP) due to their smaller area and lower power dissipation [1–3]. In order to reduce the chip area of channel detector for cognitive radio, many fixed-width Booth multipliers have been used. However, they reduce the detection accuracy because of truncated partial-products. Therefore, a quantization error compensation (QEC) technique is required in the design of fixed-width Booth multipliers.

The traditional methods of QEC for fixed-width multipliers can be divided into three categories. The first category is constant compensation [4]. In this method, the value of QEC is a constant, and it has the advantage of simplicity, but leads to large quantization error (QE). The second category is adaptive QEC [5]. This method can reduce the truncated error by using variable compensation value. The third category is hybrid error compensation, which uses both constant and adaptive QEC techniques together to reduce the truncated error. Compared with the first two categories, this category

is more accurate [6]. In [7, 8], two new QEC methods have been presented, respectively. However, these two methods are usually used in the design of Baugh-Wooley multiplier and are not applicable for the design of Booth multipliers. Another QEC method using binary threshold algorithm has been presented in [9], but its accuracy is lower compared with the method presented in [1]. In [2], the statistical analysis and linear regression analysis are adopted to generate QEC value, and the adaptive QEC method is introduced into the design of fixed-width radix-4 Booth multipliers for the first time. The adaptive QEC method has higher accuracy compared with [1] but is very complex. In order to overcome the disadvantages of [2], [10] has presented a method of dividing the truncated partial-products into the major truncated section and the minor truncated section. The major truncated section is adjacent to the reserved section, while the QEC of the minor truncated section is realized by adaptive method. In [11], a new QEC method based on [10] is proposed. Its truncation error is more symmetric, but its quantization accuracy is not improved distinctly. Reference [12] has proposed an adaptive QEC method with conditional-probability estimator instead

of the time-consuming exhaustive simulation of the previous works, especially for large bit-width Booth multipliers. One closed form formula was derived in [13] with the traditional method of probabilistic estimation to estimate the QEC. However, the closed form formula is only an approximation of the mean of the minor truncated section, which decreased the compensation accuracy.

The compensation carries of the minor truncated section in [10–13] are generated by exploiting adaptive QEC methods based on all the truncated partial-products. In [10, 11], the compensation carries are generated by all the truncated partial-products, and hence the simulation statistics will consume large amount of computer resources (time and memory requirements). The demanded resources are almost an exponential function of the bit-width. Therefore, for the multipliers with wider bits, an ordinary computer cannot compete for the simulations. Although the resources are decreased in [12, 13], their QEC accuracy cannot be effectively improved.

Based on the trade-off between the accuracy and computer resources, the minor truncated section is divided into two parts in this paper: the lower partial-products and the upper partial-products. In fact, the compensation carries are less affected by the lower partial-products of the minor truncated section. Therefore, we propose that a compensation constant of the lower partial-products can be generated by statistical analysis, and then the compensation constant is incorporated into the upper partial-products to form a shrunken minor truncated section. Finally, the quantitative compensation carries are created by applying probability estimation based on the shrunken minor truncated section; hereafter, this multiplier is called shrunken partial-products compensation (SPPC) Booth multiplier. The proposed QEC method not only reduces the QE of the multipliers, but also avoids the exhaustive simulation resource requirements. Simulations and experiments show that, comparing with the previous works [9–13], the proposed QEC method can effectively improve the QE and performances of the fixed-width Booth multipliers. In order to verify the proposed QEC method we have also designed different width SPPC multiplier circuits and have compared them with other same width multipliers based on TSMC 0.18 μm process. The experiments show that the proposed SPPC Booth multipliers have smaller die area as the width of multipliers increases.

The rest of the paper is organized as follows. Section 2 introduces the principle of the modified radix-4 Booth multiplier. Proposed QEC method is discussed in Section 3 along with circuit realization. Simulation results, comparisons, and an application experiment are presented in Section 4. Section 5 concludes the paper.

2. Modified Radix-4 Booth Multiplier

The modified radix-4 Booth recoding method was proposed in [14], which is a common method used in Booth multiplier designs.

TABLE 1: The modified Booth recoding.

$y_{2i+1}y_{2i}y_{2i-1}$	y'_i	$X_{i,\text{sel}2}$	$X_{i,\text{sel}1}$	$S_{i,\text{sel}}$	y''_i
000	0	0	0	0	0
001	$\times 1$	0	1	0	1
010	$\times 1$	0	1	0	1
011	$\times 2$	1	0	0	1
100	$\times(-2)$	1	0	1	1
101	$\times(-1)$	0	1	1	1
110	$\times(-1)$	0	1	1	1
111	0	0	0	1	0

The N -bit multiplicand X and M -bit multiplier Y of the 2-complements' multiplier are expressed as follows:

$$X = -x_{N-1} + \sum_{i=1}^{N-1} x_{N-1-i} 2^{-i}, \quad (1)$$

$$Y = -y_{M-1} + \sum_{i=1}^{M-1} y_{M-1-i} 2^{-i}. \quad (2)$$

According to modified radix-4 Booth recoding, from the most significant bit (MSB), every three bits form a group and adjacent groups overlap by one bit. When M is odd, $y_M = y_{M-1}$ is assumed for proper recoding for sign extension. In any case, $y_{-1} = 0$. Y in (2) can be rewritten as

$$Y = \sum_{i=0}^{M/2-1} y'_{M/2-1-i} 2^{-(2i+1)}, \quad (3)$$

where

$$y'_{M/2-1-i} = -2y_{2i+1} + y_{2i} + y_{2i-1}. \quad (4)$$

The recoding radix upon (1) is listed in Table 1. $X_{i,\text{sel}1}/X_{i,\text{sel}2}$, $S_{i,\text{sel}}$, and y''_i denote the binary expression, signs, and nonzero states of recoding values, respectively. The scheme of the modified radix-4 Booth recoding is shown in Figure 1.

In a radix-4 Booth multiplier, each partial-product ($p_{i,j}$) associates with two adjacent bits in X . The partial-products of four possible combinations of x_j and x_{j-1} are shown in Table 2.

A 16×16 radix-4 Booth multiplier will be used as a demo in the following discussion. Its partial-product array is shown in Figure 2. The s_i can be concluded by Table 3, the sign extension bit e_i ($i = 0, \dots, 7$) can be described as the following expression [15]:

$$e_i = \begin{cases} 0, & (X_{i,\text{sel}2}, X_{i,\text{sel}1}, s_i) = (0, 0, 0), \\ 1, & (X_{i,\text{sel}2}, X_{i,\text{sel}1}, s_i) = (0, 0, 1), \\ s_i \oplus p_{i,15}, & \text{others,} \end{cases} \quad (5)$$

where $\oplus$ is the exclusive-OR operator.

FIGURE 1: Scheme of modified radix-4 Booth recoding.

FIGURE 2: Partial-product array of radix-4 Booth multiplier (with 16×16 bits).TABLE 2: Partial-products and multiplicands $(p_{i,j}/x_j x_{j-1})$.

$y_{2i+1} y_{2i} y_{2i-1}$	$p_{i,j}/00$	$p_{i,j}/01$	$p_{i,j}/10$	$p_{i,j}/11$
000	0	0	0	0
001	0	0	1	1
010	0	0	1	1
011	0	1	0	1
100	1	0	1	0
101	1	1	0	0
110	1	1	0	0
111	1	1	1	1

TABLE 3: Partial-products of different y'_i .

y'_i	$p_{i,16}$	$p_{i,15}$	$p_{i,14}$	$\dots$	$p_{i,2}$	$p_{i,1}$	$p_{i,0}$	s_i
0	0	0	0	$\dots$	0	0	0	0
1	x_{15}	x_{15}	x_{14}	$\dots$	x_2	x_1	x_0	0
-1	$\bar{x}_{15}$	$\bar{x}_{15}$	$\bar{x}_{14}$	$\dots$	$\bar{x}_2$	$\bar{x}_1$	$\bar{x}_0$	1
2	x_{15}	x_{14}	x_{13}	$\dots$	x_1	x_0	0	0
-2	$\bar{x}_{15}$	$\bar{x}_{14}$	$\bar{x}_{13}$	$\dots$	$\bar{x}_1$	$\bar{x}_0$	1	1

Assuming that a decimal point is between P_M and P_L , which does not affect the results of discussion, then

$$\text{Sum}(P_{L,M}) = 2^{-1} (p_{0,15} + p_{1,13} + p_{2,11} + p_{3,9} + p_{4,7} + p_{5,5} + p_{6,3} + p_{7,1}), \quad (7)$$

$$\begin{aligned} \text{Sum}(P_{L,A}) = & 2^{-2} (p_{0,14} + p_{1,12} + p_{2,10} + p_{3,8} \\ & + p_{4,6} + p_{5,4} + p_{6,2} + p_{7,0} + s_7) \\ & + 2^{-3} (p_{0,13} + p_{1,11} + p_{2,9} + p_{3,7} \\ & + p_{4,5} + p_{5,3} + p_{6,1}) \\ & + 2^{-4} (p_{0,12} + p_{1,10} + p_{2,8} + p_{3,6} \\ & + p_{4,4} + p_{5,2} + p_{6,0} + s_6), \end{aligned} \quad (8)$$

3. Proposed QEC Method

3.1. Generation of QEC Carries. The partial-products of modified Booth multipliers can be divided into two sections: reserved section P_M and truncated section P_L , as shown in Figure 2. To improve the accuracy of fixed-width multipliers, an additional column $P_{L,M}$ following P_M is reserved, and the compensation carries are derived by the simulated statistic results [10]. In this paper, we further divide the rest of P_L into $P_{L,A}$ and $P_{L,C}$, and then the product of the multiplier is

$$\begin{aligned} P &= \text{Sum}(P_M) + \text{Sum}(P_L) \\ &= \text{Sum}(P_M) + \text{Sum}(P_{L,M}) + \text{Sum}(P_{L,A}) + \text{Sum}(P_{L,C}). \end{aligned} \quad (6)$$

$$\begin{aligned}
\text{Sum}(P_{L,C}) &= 2^{-5} (p_{0,11} + p_{1,9} + p_{2,7} + p_{3,5} + p_{4,3} + p_{5,1}) \\
&\quad + 2^{-6} (p_{0,10} + p_{1,8} + p_{2,6} + p_{3,4} \\
&\quad \quad + p_{4,2} + p_{5,0} + s_5) \\
&\quad \vdots \\
&\quad + 2^{-16} (p_{0,0} + s_0).
\end{aligned} \tag{9}$$

In the proposed method, the QE of $P_{L,A}$ is compensated by adaptive QEC, and the QE of $P_{L,C}$ is compensated by constant QEC. As a rule of thumb, 3~5 columns of partial-products are needed to compose $P_{L,A}$ when the width of multipliers is 8~32 bits.

In Table 1, we have defined

$$y_i'' = X_{i,\text{sel1}} \oplus X_{i,\text{sel2}}. \tag{10}$$

If Booth recoding is nonzero $(-2, -1, 1, 2)$, that is, $y_i'' = 1$, then the probability of $p_{i,j} = 0$ equals that of $p_{i,j} = 1$.

Supposing that both the probabilities of $p_{i,j} = 1$ and $s_i = 1$ are $1/2$, then

$$E[p_{ij}] = E[s_i] = \frac{1}{2}, \tag{11}$$

where $E[\cdot]$ is the expected value. Substituting (11) in (9) we can obtain

$$\begin{aligned}
E[\text{Sum}(P_{L,C})] &= 2^{-5} \left(\frac{1}{2} + \dots \right) + 2^{-6} \left(\frac{1}{2} + \dots \right) \\
&\quad + \dots + 2^{-16} \left(\frac{1}{2} + \frac{1}{2} \right) = \frac{3}{16}.
\end{aligned} \tag{12}$$

Thus, the constant $3/16$ acts as the QEC value of $P_{L,C}$. Similarly, the expected value of s_7 is $1/2$. We replace s_7 with $1/2$ in (8), obtaining its equivalent decimal value of $1/8$.

Based on the above proposed SPPC multiplier, the $P_{L,A}$ with carries in Figure 2 can be redisplayed in Figure 3, which is denoted by $P'_{L,A}$.

The maximum carries will be generated if all $p_{i,j}$ in $P_{L,A}$ are 1. In Figure 3, the maximum carries need 7 bits; therefore we register the carry output states of $P_{L,A}$ in the variable r_i ($i = 0, \dots, 6$) temporarily. In the following, we propose one method that associates the nonzero recoding label y_i'' with the compensation carries.

According to the number of 1 in y_i'' , we divide the shrunk partial-product section $P'_{L,A}$ in Figure 3 into 9 categories. If there is only one 1 in y_i'' , such as $y_7'' y_6'' y_5'' y_4'' y_3'' y_2'' y_1'' y_0'' = 00000001$, then only one row in $P'_{L,A}$ is nonzero, which is the first category (cate-1). We count the total numbers of $r_i = 1$ in all the simulation cases. If there are two 1's in y_i'' , such as $y_7'' y_6'' y_5'' y_4'' y_3'' y_2'' y_1'' y_0'' = 00000011$, then there are two rows in $P'_{L,A}$ that are nonzero. As discussed above, once again we count the total numbers of $r_i = 1$ in all the cases by simulation, which is named the second category (cate-2). The remaining seven categories are

FIGURE 3: Rebuilt shrunk adaptive section.

deduced as above. Compared with [10, 11], the method can greatly reduce the simulation cost. The statistical results of different categories are listed in Table 4 (note that the middle bit between $p_{7,0}$ and s_6 in $P'_{L,A}$ is still regarded as a partial-product in simulation).

We then encode each category with 4-bits to associate y_i'' with compensation carries. For example, cate-0 is encoded $z_3 z_2 z_1 z_0 = 0000$, cate-1 is encoded $z_3 z_2 z_1 z_0 = 0001$, and so on. The compensation carries c_i are derived by Table 4, which comply with the following rule: if the numbers of $r_i = 1$ are larger than a half of the numbers of simulations (NoS), then $c_i = 1$, otherwise $c_i = 0$. The corresponding relations between the code $(z_3 z_2 z_1 z_0)$ and c_i are listed in Table 5.

According to Table 5, the carries $c_0 \sim c_3$ are

$$\begin{aligned}
c_0 &= z_3 \bar{z}_2 \bar{z}_1 \bar{z}_0 + \bar{z}_3 \bar{z}_2 \bar{z}_1 \bar{z}_0, \\
c_1 &= z_3 \bar{z}_2 \bar{z}_1 \bar{z}_0 + \bar{z}_3 z_2 + \bar{z}_3 z_1 z_0, \\
c_2 &= z_3 \bar{z}_2 \bar{z}_1 \bar{z}_0 + \bar{z}_3 z_2 (z_1 + z_0), \\
c_3 &= z_3 \bar{z}_2 \bar{z}_1 \bar{z}_0 + \bar{z}_3 z_2 z_1 z_0.
\end{aligned} \tag{13}$$

3.2. Architecture Design of SPPC Booth Multipliers. The circuit implementation of category encoding is shown in Figure 4, where the 2Bs-Adder and 3Bs-Adder denote the two-bit adder and three-bit adder, respectively.

In light of (13), one implementation of carry generation circuits is shown in Figure 5.

According to the above discussions, a modified radix-4 Booth fixed-width multiplier with the proposed QEC circuits is shown in Figure 6. The traditional Booth recoding encoder, circuits of the proposed category encoding, and carry generation compose the QEC circuits to generate the QEC carries.

TABLE 4: The statistic of carry output states for different categories.

Category	Total numbers of $r_i = 1$							NoS
	r_0	r_1	r_2	r_3	r_4	r_5	r_6	
cate-0	0	0	0	0	0	0	0	0
cate-1	7		0	0	0	0	0	8
cate-2	63	21	0	0	0	0	0	8^2
cate-3	511	350	35	0	0	0	0	8^3
cate-4	4095	3605	1225	35	0	0	0	8^4
cate-5	32767	31486	18844	2898	21	0	0	8^5
cate-6	262143	259147	205534	71022	4963	7	0	8^6
cate-7	2097151	2090724	1897019	1048576	200133	6428	1	8^7
cate-8	16777215	16764354	16144677	11782380	4146393	438834	6435	8^8

TABLE 5: Relations between category code and c_i .

$z_3 z_2 z_1 z_0$	c_0	c_1	c_2	c_3
0000	0	0	0	0
0001	1	0	0	0
0010	1	0	0	0
0011	1	1	0	0
0100	1	1	0	0
0101	1	1	1	0
0110	1	1	1	0
0111	1	1	1	1
1000	1	1	1	1

4. Comparisons and Discussions

4.1. Quantization Accuracy Simulations. The comparison of various errors between the proposed SPPC Booth multipliers and the ideal truncated Booth multiplier and other previous works is listed in Table 6. These errors include the average error ϵ_{mean} , maximum error ϵ_{max} , and variance ϵ_{var} . In accuracy simulation, all the pair data samples are inputted to estimate the QE of the SPPC multiplier. The ϵ_{mean} , ϵ_{max} , and ϵ_{var} are defined as follows:

$$\begin{aligned}
 \epsilon_{\text{mean}} &= E[P - P_q], \\
 \epsilon_{\text{max}} &= \max\{|P - P_q|\}, \\
 \epsilon_{\text{var}} &= E[(P - P_q)^2] - (E[P - P_q])^2,
 \end{aligned} \tag{14}$$

where P and P_q are the ideal product and the quantized product of Booth multipliers, respectively; $|\cdot|$ and $\max\{\cdot\}$ are the absolute and maximum operators, respectively.

The adaptive estimation methods in [9–11] have been adopted to improve the truncation error. Instead of exhaustive computing resource simulation methods in previous works [9–11], the QE of SPPC multipliers is analyzed and derived from a simpler statistical method. It is seen from Table 6 that the proposed SPPC multipliers have almost the best error performance compared with previous works, except [11] that has the highest performance of ϵ_{mean} . The reason is that it uses more information from Booth encoder

to alleviate the truncation errors [11]. Nevertheless, the area cost in [11] is increased from the extra information of compensation circuits. Even though ϵ_{max} and ϵ_{var} of the multipliers in [13] are smaller than other multipliers, their ϵ_{mean} is larger compared with the proposed SPPC multiplier and multipliers in [10–12].

The distributions of QE have been calculated in different multipliers. The sample ratios of QE value (i.e., ϵ) are listed in the last three columns of Table 6. It is seen from the statistical results that the sample ratios of $|\epsilon| < 1$ in the SPPC Booth multipliers are higher than that in [9–11] by about 13%. On the other hand, this shows that the quantization accuracy of the proposed SPPC multiplier is higher compared with those four methods.

4.2. Performance Simulation. A comparison of performances between the proposed SPPC and previous works is implemented by using their own compensation circuits. Multipliers with different widths are synthesized by Synopsys Design Compiler using a standard cell library of TSMC 0.18 μm CMOS process. Their area, delay, and power dissipation are listed in Table 7.

In general, there exists a trade-off between the hardware overhead and the accuracy in these compensation circuits. The multiplier proposed in [11] has the highest accuracy in ϵ_{mean} , but it has a larger area, delay, and power. However, the SPPC multiplier has the same area as the multipliers in [12, 13] and lower area compared with the multipliers in [9–11]. As a result, the proposed SPPC multipliers achieve higher accuracy at the cost of the lower area.

In order to comprehensively compare the performances of different multipliers, we consider their power-delay products as the standard of comparisons, which are listed in the last column of the Table 7. It is shown that the power-delay products of multipliers proposed in [9–11] are larger than that of other multipliers distinctly. Compared with the other two multipliers in [12, 13], the proposed SPPC multipliers have better comprehensive performances.

4.3. Verification in FIR Filter. The QEC performance of the proposed SPPC is verified by means of a 20 taps low-pass direct form FIR filter. The filter is designed to have 8 MHz pass-band (with a 40 MHz sampling frequency) and 70 dB

FIGURE 4: Category encoding circuits.

FIGURE 5: Carry generation circuits.

attenuation in the stop-band for a CR detector. All the widths of input, output, and coefficient of the FIR filter are 16 bits, and the internal adders of the FIR filter are 22 bits. The input for test is a 5 MHz sinusoidal signal with a sampling rate of 40 MHz.

Four different multipliers (16×16 bits) including the SPPC multiplier and three other multipliers in [11–13] are instantiated in the filter. The error mean and error variance of the output samples in different instantiated multipliers are listed in Table 8. It is seen from Table 8 that the error mean of [11] is the smallest, and the error mean of SPPC is better

than that of [12, 13], whereas the error variance of SPPC is the smallest. These results are consistent with the QE accuracy simulation results in the previous section.

In CR detectors, it is very important to detect the signal's spectral peak-values for determining whether the channel is idle [16]. The relative errors of the average spectral peak-values (with 100 times of simulations) with respect to the ideal spectral peak-values of the FIR filter outputs are listed in the last column of Table 8. Table 8 shows that the spectral peak-values of the proposed SPPC multiplier are closer to the ideal peak-value.

FIGURE 6: Partial-product array of fixed-width Booth multiplier with proposed QEC.

TABLE 6: Comparisons of QE.

Width (bits)	Multiplier	$\epsilon_{\max}$	ϵ_{mean}	ϵ_{var}	Sample ratios in QE values (%)		
					$ \epsilon < 1$	$1 \leq \epsilon < 2$	$2 \leq \epsilon < 3$
8	Ideal	0.5	0	0.0833	100%	—	—
	[9]	1.1641	0.1768	0.1459	79.9	21.1	0
	[10]	1.5000	0.1328	0.1664	77.2	22.797	0.0031
	[11]	1.1680	0.0078	0.1367	81.5	18.5	0
	[12]	1.1680	-0.1152	0.1237	87.7	12.3	0
	[13]	0.7502	0.1534	0.0961	92.74	7.26	0
10	SPPC	1.4308	0.0941	0.1365	90.3	9.698	0.0016
	[9]	1.3652	0.2028	0.1713	74.9	25.1	0
	[10]	1.5000	0.1211	0.1713	74.0	22.558	0.0121
	[11]	1.5000	-0.0039	0.1542	77.43	22.57	0
	[12]	1.5000	-0.1284	0.1379	80.28	19.72	0
	[13]	0.9998	0.1637	0.0923	90.81	9.181	0.009
12	SPPC	1.5525	0.1074	0.1417	89.9	10.08	0.0084
	[9]	1.5649	0.2203	0.1960	72.50	27.50	0
	[10]	2.0000	0.1270	0.1950	73	26.65	0.018
	[11]	1.6667	0.0020	0.1671	76.83	23.17	0
	[12]	1.6667	-0.1229	0.1521	78.60	21.384	0.016
	[13]	1.2493	0.1763	0.1114	90.00	9.987	0.013
16	SPPC	1.6302	0.1135	0.1532	89.70	10.287	0.013
	[9]	1.9650	0.2384	0.2409	67.71	32.29	0.005
	[10]	2.5000	0.1255	0.2235	70.10	29.83	0.07
	[11]	2.1667	0.0005	0.1961	73.13	26.85	0.02
	[12]	2.1667	-0.1245	0.1806	74.46	25.52	0.02
	[13]	1.5000	0.1754	0.1167	89.37	10.614	0.016
16	SPPC	1.9903	0.1228	0.1859	87.60	12.37	0.03

5. Conclusion

By further dividing the minor truncated section of Booth multiplier into the adaptive compensation and constant compensation sections, we rebuilt the adaptive QEC for fixed-width multipliers. According to the numbers of 1 in the

sequence of nonzero Booth recoding label we propose a new QEC method to generate the compensation carries. The simulation results have shown that the QE of the SPPC is smaller compared with the existing methods. The proposed QEC method and SPPC are useful for the DSP system with a large width multipliers and higher precision requirements.

TABLE 7: Comparisons of performances with other methods.

Width (bits)	Multiplier	Area (μm^2)	Power (mW)	Delay (ns)	Power-delay product (mW·ns)
8	Ideal	3392	1.030	5.82	5.995
	[9]	2396	0.667	6.14	4.095
	[10]	2238	0.639	5.81	3.713
	[11]	2251	0.628	5.85	3.674
	[12]	2246	0.636	5.80	3.689
	[13]	2307	0.682	5.16	3.519
	SPPC	2242	0.633	5.22	3.304
10	Ideal	5154	1.293	6.60	8.534
	[9]	3758	0.833	6.97	5.806
	[10]	3479	0.789	6.26	4.940
	[11]	3395	0.777	6.62	5.144
	[12]	3252	0.715	6.13	4.383
	[13]	3351	0.842	5.91	4.982
	SPPC	3358	0.712	6.09	4.336
12	Ideal	7455	1.773	7.24	12.837
	[9]	5286	1.137	7.61	8.653
	[10]	5144	1.064	6.67	7.097
	[11]	5161	1.099	7.43	8.166
	[12]	4942	0.974	6.60	6.428
	[13]	4923	1.040	6.56	6.822
	SPPC	5056	1.012	6.63	6.710
16	Ideal	13554	2.562	8.06	20.650
	[9]	10058	1.563	8.41	12.145
	[10]	9692	1.486	7.84	11.650
	[11]	9508	1.476	8.08	11.926
	[12]	9390	1.310	7.81	10.230
	[13]	9297	1.403	7.58	10.635
	SPPC	9312	1.329	7.67	10.193

TABLE 8: Comparisons of experimental results.

Multiplier	Mean	Variance	Relative error of peak-value (%)
[11]	0.015	0.315	0.0082
[12]	0.054	0.327	0.0101
[13]	0.069	0.417	0.0094
SPPC	0.043	0.306	0.0084

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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