Editorial

Advanced VLSI Design Methodologies for Emerging Industrial Multimedia and Communication Applications

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Along with the rapid development of emerging industrial applications, such as new-generation wireless communications, multimedia, and microprocessors, very-large-scale-integration (VLSI) design methodologies need to advance to a new technology era to meet the stringent requirements and specifications of the diversified applications. Modern wireless communications, with the trends of high data rates and low power consumption, are developing well. Multimedia applications require high resolution, high video bit rates, and complex video compression. There is an increasing interest in microprocessor applications, with the requirements of low power and high speed. There are many industrial applications driving the VLSI design methodologies to an advanced horizon.

This special issue contains six papers focusing on advanced VLSI design methodologies for emerging industrial applications. These papers involve analog circuit, digital circuit, or system-on-a-chip (SoC) design. Some papers address the low-power test and resource-sharing issues from different perspectives. Some papers discuss the emerging issues in SoC design and present interesting new challenges.

In the paper entitled “A high-efficiency monolithic dc-dc PFM boost converter with parallel power MOS technique,” the authors present a high-efficiency dc-dc boost converter for a portable supply. A novel load current detector and parallel power metal-oxide-semiconductor (MOS) technique is proposed to accurately adjust the number of parallel power MOS transistors used, based on the load conditions, to achieve high power efficiency.

In the paper entitled “A prototype-based gate-level cycle-accurate methodology for SoC performance exploration and estimation,” the authors present an SoC gate-level cycle-accurate performance methodology based on the SoC prototype. The framework is a three-phase design process; it can meet the gate-level cycle-accurate requirement, which concurrently covers the effects of the embedded processor, on-chip bus structure, intellectual property (IP) design, embedded operating system (OS), graphic user interface (GUI) systems, and application programs.

In the paper entitled “Design a bioamplifier with high CMRR,” the authors present a bioamplifier with high gain and high common-mode rejection ratio (CMRR). According to the obtained performance properties, it is promising that a process independent performance can be obtained for this amplifier.

In the paper entitled “Design example of useful memory latency for developing a hazard preventive pipeline high-performance embedded-microprocessor,” the authors present that additional in-board memory can be well utilized to handle hazardous conditions. When the instruction meets hazardous issues, the memory latency can be used to prevent performance degradation due to the hazard prevention mechanism. By the proposed technique, a better architectural design can be rapidly validated by a field-programmable gate array (FPGA) at the start of the design stage.

In the paper entitled “Discrete wavelet transform on color picture interpolation of digital still camera,” the authors

integrate discrete wavelet transform (DWT) into the interpolation algorithm. The method developed is based on edge weight and partial gain characteristics and uses the basic wavelet function to enhance the edge performance and processes of the nearest or larger and smaller direction gradients.

In the paper entitled “*High-accuracy programmable timing generator with wide-range tuning capability*,” a high-accuracy programmable timing generator with wide-range tuning capability is proposed and designed. With the aid of dual delay-locked loops (DLLs), the timing generator can provide accurate subgate resolution with closed-loop delay control and instantaneous switching capability.

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