Research Article

The Design of Low Noise Amplifiers in Deep Submicron CMOS Processes: A Convex Optimization Approach

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With continued process scaling, CMOS has become a viable technology for the design of high-performance low noise amplifiers (LNAs) in the radio frequency (RF) regime. This paper describes the design of RF LNAs using a geometric programming (GP) optimization method. An important challenge for RF LNAs designed at nanometer scale geometries is the excess thermal noise observed in the MOSFETs. An extensive survey of analytical models and experimental results reported in the literature is carried out to quantify the issue of excessive thermal noise for short-channel MOSFETs. Short channel effects such as channel-length modulation and velocity saturation effects are also accounted for in our optimization process. The GP approach is able to efficiently calculate the globally optimum solution. The approximations required to setup the equations and constraints to allow convex optimization are detailed. The method is applied to the design of inductive source degenerated common source amplifiers at the 90 nm and 180 nm technology nodes. The optimization results are validated through comparison with numerical simulations using Agilent's Advanced Design Systems (ADS) software.

1. Introduction

The low-noise amplifier (LNA) is the critical component in the analog front-end of a radio frequency (RF) receiver. The LNA is responsible for providing sufficient amplification of weak input signals while minimizing the amount of added electronic noise and distortion. As a result, the characteristics of the LNA set the upper limit on the performance of the overall communication system. The optimization of the LNA is a complex task involving tradeoffs that must be made among several competing parameters including noise figure, linearity, and impedance matching [1]. While bipolar technologies have traditionally dominated RF designs due to their superior switching frequency and gain, they are not particularly suited for low power design and are not directly compatible with scaled digital CMOS processes. In the late 1990s, the transit frequency of CMOS devices reached the 40 GHz range, which enabled the design and implementation of RF CMOS circuits that could process signals on the order of 4 GHz [2]. A combination of improved

processing technology, suitable MOS circuit architectures, and amenable wireless standards have helped push CMOS technology to the forefront for RF circuit implementations [3–5]. Implementing high quality RF analog circuits on scaled digital processes is a desired goal for a couple of reasons. First, a prime motivation is the increased integration densities and resulting lower costs. Second, it allows the realization of a complete RF transceiver on a systems-on-a-chip (SoC) implementation, which would further improve design flexibility and system optimization [6]. An SoC design with digital, analog, and RF components will pave the way for radio systems that are largely software-controlled digital devices [3]. While the digital components dominate in a software-defined radio (SDR) architecture, the analog front-end including the LNA will remain the critical component that determines the overall system performance.

In the rapidly growing consumer demand for portable wireless devices with long battery life, obtaining sufficient receiver sensitivity while minimizing power dissipation is a major design objective. As process scaling continues to shrink

the dimensions of the CMOS transistors, RF circuits will benefit from the improved switching frequencies. However, the main issue will be the reduction in performance due to increased thermal noise from MOSFETs implemented in scaled digital CMOS processes and lower gain and signal swing headroom as voltage supplies are inevitably decreased. With reduction in the analog voltage supplies, an increase in power dissipation is required in order to maintain constant performance [7]. Hence, innovations in circuit topologies and optimization methods will be required to maintain low power and high performance as device scaling continues deep into the nanometer-scale dimensions.

A common design methodology is to determine the minimum noise that can be obtained given constraints on impedance matching and power dissipation. Using classical two-port noise theory, the optimum impedance that must be presented at the source of the LNA in order to achieve the minimum noise figure (NF) can be calculated. An appropriate matching network is inserted between the source and the LNA to help achieve this goal as illustrated in Figure 1. It is well known that maximum power transfer between the source and the amplifier input occurs when the complex conjugate of Z'_{in} matches the source impedance Z_s [1]. Common-source (CS) amplifiers have been the most popular CMOS LNA circuit topologies due to their good low-noise performance and high gains. However, when using a CS amplifier, the input impedance Z_{in} presented by the MOSFET makes it difficult to optimally match with the external impedance Z_s , which is generally resistive in nature [8]. Hence, tradeoffs in terms of noise performance and gain must be made with this architecture.

The basic amplifier architecture illustrated in Figure 2 allows the noise figure to be minimized while achieving input matching under power constrained conditions. The addition of inductive source degeneration and an input impedance matching inductive component, denoted by L_s and L_g , respectively, allows improved impedance matching to be obtained over a narrow band of interest. The addition of the capacitance C_e gives the added design flexibility of meeting a given power dissipation and input matching specification while maintaining a very low noise performance [9]. The cascode device M_2 provides isolation with the load.

Efficient and accurate optimization techniques for implementing analog integrated circuits are a critical facet of a CAD-based design flow. This is essential when the goal is to minimize the time-to-market for a product, and thus have working designs on first silicon [10]. While the noise analysis of a linear two-port network provides some insight into how to optimize the noise figure (NF) of an amplifier [11], this classical approach does not provide any guidance on the sizing of the devices. Various approaches that incorporate suitable FET device characteristics and noise models into the design process have been developed [12–14]. In order to account for second order effects in devices as scaling occurs, two general optimization strategies can be used: simulation-based and equation-based methods. A simulation-based approach allows more general topologies and circuit parameter variations to be explored. However, there are a couple of drawbacks to this approach. First, as metaheuristic algorithms, such as

FIGURE 1: Generalized block diagram of the low noise amplifier as the key front-end component.

FIGURE 2: Schematic of a CMOS cascode low noise amplifier with inductive source degeneration.

genetic algorithms and other evolutionary techniques, are often used, this approach is very computationally intensive. This is due to the large number of iterations that require detailed circuit simulations to be executed [15–18]. Second, there is no guarantee that a globally optimum solution is found. On the other hand, equation-based methods attempt to formulate a solution for a more restricted set of parameters and usually for a predetermined circuit topology. Geometric programming methods are able to find a globally optimum solution very efficiently for a well-formulated problem [19]. The trade-off in this case is that certain approximations must be made to ensure that the device equations are in a form suitable for numerical optimization. However, once the system is set-up, a globally optimum design can quickly be found.

In this paper, the focus is on the optimization of a specific topology, the CS CMOS LNA, when short-channel effects such as excess thermal noise must be taken into consideration. As such, we will make use of convex optimization, a form of geometric programming. Geometric programming (GP) has been previously employed to optimize a variety of integrated circuit designs, including both analog and digital circuits [20–25]. For a comprehensive overview and list of GP applications, see [19]. The approach in this paper is to optimize the NF of the CS LNA subject to various constraints

such as input circuit quality factor, power consumption, and input impedance matching, similar to [12]. The optimization procedure will allow the globally optimum selection of device parameters. Geometric programming has been used to optimize the design of RF CMOS low-noise amplifiers at the 0.35 μm technology node [26] using the design proposed in [9]. While the work by [26] results in globally optimum solutions with an extremely small computational cost, it does not take into account MOSFET submicron device characteristics and the issue with excess noise in the nanoscale regime is not addressed.

The main contribution of this study is the incorporation of important MOSFET short-channel effects including excess noise into a GP framework to enable the optimization of LNAs designed in deep submicron processes [27]. An extensive review and evaluation of the various approaches used to model the excess noise in nanoscale devices is given. In addition, the approximations required to convert the relevant device equations into a form required by the GP algorithms while minimizing the amount of accuracy lost in the noise and current-voltage model equations are detailed. This paper is outlined as follows. The second section provides the background theory on modeling MOSFET noise, including the various models used to explain the sources of excess thermal noise in MOSFETs with nanoscale dimensions. The third section describes the optimization method for designing the RF LNA using geometric programming. The fourth section presents the results from applying geometric programming to obtain the globally optimal solution for RF LNA designs in 90 nm and 180 nm processes. The generated optimal solutions are compared with results from Agilent's Advanced Design Systems (ADS) software. Finally, the implication of geometric programming for short-channel CMOS designs is discussed and future work in this area is described.

2. Noise in Deep Submicron CMOS Processes

While MOSFETs in aggressively scaled CMOS processes have sufficiently high transit frequencies (f_T) for RF circuit applications, issues with increased noise levels may prevent low noise operation. This section discusses the issues with excess noise that have been experimentally observed. A review of basic noise theory is first undertaken, followed by a discussion of the relevant observations in the literature regarding the issue of excess MOSFET noise. This section concludes with a summary of the key parameters used to model this excess thermal noise in deep submicron processes.

2.1. Basic MOSFET Noise Theory. An expression for the power spectral density due to the thermal noise in a MOSFET is derived in this subsection. The relationship between the channel current and the local channel conductivity of the MOSFET is considered first. The drain current of a MOSFET can be expressed by the following relationship:

$$I_d = g(V(x)) \cdot \frac{dV(x)}{dx}, \quad (1)$$

where $V(x)$ is the channel potential at position x in the device's channel as shown in Figure 3, $dV(x)$ is the dc voltage

FIGURE 3: Cross-section of an n -channel MOSFET transistor.

difference in the electron quasi-Fermi level in the inversion layer and the hole quasi-Fermi level in the substrate at position x , and $g(V(x))$ is the local channel conductivity.

For a simple long-channel MOSFET using the gradual channel approximation, the following relationships can be written [8]:

$$g(V(x)) = \mu C_{ox} W (V_{od} - V(x)), \quad (2)$$

$$V_{od} = V_{gs} - V_{th},$$

where V_{gs} is the gate-to-source voltage, V_{th} is the threshold voltage, V_{od} is the gate overdrive voltage, W is the width of the MOSFET, μ is the carrier mobility, and C_{ox} is the oxide capacitance per unit area.

Assuming a differential segment Δx of the channel, a small noise voltage contribution $v(x)$ across the segment Δx is observed, which is added to the dc voltage $V(x)$. This voltage can cause noise in the drain current, which leads to a change in the dc current through the MOSFET. In the following analysis, a couple of assumptions are made. First, noise sources of the different channel segments are local and not correlated. Second, the charge carriers are in thermal equilibrium. The boundary conditions of the small voltage contribution $v(x)$ are $v(x)|_{x=0,L} = 0$ [8]. The power spectral density S_{i_d} for the thermal noise of a long-channel MOSFET is then expressed by the Klaassen-Prins equation [28]:

$$S_{i_d} = \frac{4kT}{L^2 I_d} \int_0^{V_{ds}} g^2(V) \cdot dV, \quad (3)$$

where I_d is the drain current of the device. The impact of hot electron effects can be modeled by replacing the lattice temperature with carrier temperature, $T_e(x)$ [8]:

$$S_{i_d} = \frac{4kT}{L^2 I_d} \int_0^{V_{ds}} \frac{T_e(x)}{T} g^2(V) \cdot dV. \quad (4)$$

For noise analysis, it is often convenient to treat the MOSFET as a resistive element:

$$S_{i_d} = 4kT \gamma g_{d0}. \quad (5)$$

The parameter γ is known as the white noise gamma factor, given the relationship between the thermal noise power spectral density and the output conductance at different bias conditions [27]:

$$\gamma = \frac{1}{g_0 I_d L} \int_0^{V_{ds}} \frac{T_e(x)}{T} g^2(V) \cdot dV. \quad (6)$$

In (6), g_0 is the channel conductance per unit length at the source and g_{d0} is the channel conductance at zero drain bias. The value of γ is unity for zero drain bias in long-channel devices and decreases toward 2/3 in saturation. The expression in (6) is commonly used to express the thermal noise in long-channel MOSFETs. In practice, the white noise gamma parameter continues to be used as a common metric to allow experimental or theoretical results to be compared from different research groups when describing the degree of excess channel thermal noise in short-channel transistors [29].

The variation of the channel charge due to thermal noise is capacitively coupled to the gate terminal, resulting in a noisy gate current. Just as the white noise gamma parameter provides a convenient way to express the power spectral density of the thermal noise, the introduction of a beta parameter allows the induced gate noise to be expressed in a similar manner [8]:

$$S_{i_g} = 4kT\beta g_g. \quad (7)$$

The parameter β is basically independent of the substrate conductivity, and its value is 4/3 in the saturation region for long-channel MOSFETs. The conductance g_g is given by

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}, \quad (8)$$

where C_{gs} is the intrinsic gate capacitance of the transistor. In the circuit model representation illustrated in Figure 4, the conductance g_g is connected between the gate and source shunted by the gate noise current $\tilde{i}_{ng}$. From (8), it can be observed that the conductance g_g increases with frequency, indicating that the induced gate noise can dominate at radio frequencies. The conductance g_g is also proportional to the square of C_{gs} , so a small value of C_{gs} will favor a lower induced gate noise.

Since the induced gate noise is correlated with the drain thermal noise, the correlation coefficient is defined as [8]:

$$c = \frac{\overline{\tilde{i}_{ng} \cdot \tilde{i}_{nd}^*}}{\sqrt{\overline{\tilde{i}_{ng}^2} \cdot \overline{\tilde{i}_{nd}^2}}}, \quad (9)$$

where $\overline{\tilde{i}_{ng} \cdot \tilde{i}_{nd}^*}$ is the spectrum of the cross-correlation of the drain thermal noise and the induced gate noise. The complex correlation coefficient c is theoretically $0.395j$ for long-channel MOSFETs as noted in Appendix C [8].

The finite resistance of the gate material also contributes to this noisy gate current and can become the dominant source of gate thermal noise in short-channel MOSFETs [30]. Two factors tend to minimize this source of gate noise. First, modern CMOS processes use silicided gate material which helps reduce the resistance in the gate. Second, for wide MOSFETs, a multifinger layout can be used whereby several devices (i.e., “fingers”) are connected in parallel, giving the gate resistance as [31]:

$$R_g = \frac{R_{sh}}{12 \cdot n_f^2} \frac{W}{L}, \quad (10)$$

FIGURE 4: Circuit model for the gate noise [1, 8].

where R_{sh} is the sheet resistance of the gate material, n_f is the number of fingers, and the factor of 12 is due to the distributed nature of the gate resistance when it is contacted on both ends [12, 32]. As devices scale to submicron dimensions, the interface resistance between the silicide and polysilicon layers becomes an important component of R_g which is not significantly impacted by layout optimizations [33].

2.2. Modeling Thermal Noise in Short-Channel Devices.

Excess thermal noise for scaled devices must be taken into account when designing LNAs operating at RF frequencies. In this subsection, we review recent methods used to model this noise. This provides the background on the current understanding of the excess thermal noise issue in deep submicron devices. While this issue is still a matter of open debate among researchers [34, 35], the development of models will provide the reader with the context to understand the comparisons in the following subsection as well as the rationale for the use of an empirical fit to the data for our optimization method. Here the emphasis is on extending the classical theory of thermal noise to submicron devices by including short-channel effects such as velocity saturation, channel-length modulation, and hot carriers. The Klaassen-Prins equation for the noise power spectral density in (3) can be modified to include channel-length modulation and velocity saturation effects as follows:

$$S_{i_d} = \frac{4kT}{L_{elec}^2 I_d} \int_0^{V_{ds}} g_c^2(V) \cdot dV, \quad (11)$$

where L_{elec} is the electrical channel length of the MOSFET, replacing the effective channel length L_{eff} in the long-channel expression [29, 30, 35]. The parameter L_{elec} is defined as $L_{elec} = L_{eff} - \Delta L$ where ΔL is the length of the velocity saturated region. The parameter g_c is the revised conductivity taking velocity saturation into consideration. The noise contribution of the pinch-off region is assumed to be negligible as experimental evidence indicates that the channel thermal noise is practically independent of the drain-to-source voltage beyond the saturation voltage [30].

The approach by Han et al. [36, 37] is to consider the effects of velocity saturation and carrier heating. While the carrier mobility is considered independent of the bias conditions and is usually modeled as a constant in long-channel MOSFETs, it is degraded in short-channel devices due to the high lateral electric field from drain to source [38] and is thus dependent on the bias conditions. The impedance field method [39] was used to recalculate the thermal noise

for short-channel MOSFETs. The drain current of a MOSFET with the effect of mobility degradation is then given by [37]

$$I_d = g_0(V) \frac{(dV/dx)}{1 + (dV/dx)/E_C}, \quad (12)$$

where the local channel conductance $g_0(V) = \mu_{\text{eff}} W C_{\text{ox}} (V_{\text{od}} - \alpha V)$. The parameter $E_C = 2v_{\text{sat}}/\mu_{\text{eff}}$ is the critical field at which velocity saturation occurs, v_{sat} is the saturation velocity of carriers, μ_{eff} is the effective mobility, and α is a coefficient describing the bulk-charge effect. The bulk-charge effect is the variation of threshold voltage caused by nonuniform channel depletion and the dependence of the threshold voltage on the channel potential. The impact of the carriers in the velocity saturation region on the drain thermal noise current is ignored in this analysis. Applying a similar procedure as [30], the channel noise of the MOSFET takes the form of [37]

$$S_{i_d} = \frac{4kT}{L_{\text{elec}}^2 I_d (1 + V_{\text{ds}}/(L_{\text{elec}} E_C))^2} \cdot \int_0^{V_{\text{ds}}} g_0^2(V) \left(1 + \frac{E}{E_C}\right) \cdot dV, \quad (13)$$

where the electrical channel length of the MOSFET is $L_{\text{elec}} = L_{\text{eff}} - \Delta L$. In order to obtain a compact analytical equation, a closed-form expression is given by [37]

$$S_{i_d} \approx 4kT g_{d0} \frac{1 - u + u^2/3}{1 - u/2}, \quad (14)$$

where g_{d0} is the drain conductance at $V_{\text{ds}} = 0$ V, $u = \alpha V_{\text{ds}}/V_{\text{od}}$. The coefficient of the bulk-charge effect α has a typical value of 1.2 [40].

Based on [36], the longitudinal electric field (E) along the channel was examined by Deen et al. [31]. The longitudinal electric field (E) is now expressed as a function of the position x along the channel instead of simply being constant:

$$E(x) = \frac{E_C V_d}{[(2V_{\text{od}} - V_d)^2 - 4\alpha E_C V_d x]^{1/2}}, \quad (15)$$

where $V_d = I_d/(W C_{\text{ox}} v_{\text{sat}})$ and V_{od} is the gate overdrive voltage given in (2). The revised total channel charge can be obtained by integrating the drain current from 0 to L_{elec} with the expression of $E(x)$ in (15). The total drain current noise power spectral density is then obtained:

$$S_{i_d} = 4kT \frac{4V_{\text{od}}^2 + V_d^2 + V_{\text{od}} V_d}{3V_{\text{od}}^2 (V_{\text{od}} - V_d)} \alpha I_d. \quad (16)$$

An analytical thermal noise model following [41] was developed by Jeon et al. [42], which includes short-channel effects such as channel-length modulation, velocity saturation, and hot carrier effects. The ac conductance g_{ac} is a small signal conductance with the consideration of velocity saturation. It expresses the current noise source spectrum of a small segment of the channel length Δx :

$$\overline{\Delta i_n^2} = 4kT_c g_{\text{ac}} \Delta f, \quad (17)$$

where T_c is the carrier effective temperature. The carrier temperature has shown a dependency on the electric field when a high electric field is present in short-channel MOSFETs. The relation of T_c and the electric field is given as

$$\frac{T_c}{T_0} = \left(1 + \frac{E}{E_C}\right)^n, \quad (18)$$

where T_0 is the lattice temperature. When $n = 0$, the carrier is in thermal equilibrium without any carrier heating effect while the heating effect is considered for $n = 1$ or $n = 2$ [8]. Experimental measurements with devices having channel lengths of 130 nm indicate that the carrier heating effect with $n = 2$ gives the most accurate results [42].

2.3. Results and Comparisons of Modeling Noise in Short-Channel Devices. While the expressions for the power spectral density in (11) and (13) include short-channel effects, they are not compatible with the form required by geometric programming. A simpler noise formula which captures the essence of the noise issues at the deep submicron technology nodes is required. As previously noted, the channel thermal noise can be conveniently expressed using the white noise gamma expression given in (6). Since this expression is a simple closed-form equation, it has been widely used for noise analysis by circuit designers. For long-channel MOSFETs, the theoretical values of γ are well known. It is equal to unity at zero drain bias and 2/3 in the saturation region.

The analysis and experimental measurements by Scholten et al. [30] have shown that the channel thermal noise constant γ and the gate current noise parameter β are independent of the operating frequencies up to moderately high frequencies (around 10 GHz), and they are not very sensitive to bias conditions for high bias voltages. However, both parameters are expected to increase as channel lengths scale down in the submicron range. The values of γ are expected to be larger than their theoretical long-channel values due to excess channel thermal noise discussed previously for short-channel MOSFETs. Due to induced gate noise related to channel noise and the increased significance of the resistivity of the gate material at short-channel lengths, the parameter β will experience a similar increase in value.

Based on the measurements of Jeon et al. [43], the channel thermal noise power spectral density can still be expressed by use of the white noise parameter γ when short-channel effects account for

$$\gamma = \frac{g_{\text{ds}}}{g_{d0}} \left(1 + \frac{\bar{E}}{E_C}\right), \quad (19)$$

where g_{ds} is the conductance of the channel, and $\bar{E}$ is the average longitudinal electric field which is equal to $V_{\text{ds}}/L_{\text{elec}}$. The parameter E_C is the critical electric field, which is equal to $2v_{\text{sat}}/\mu_{\text{eff}}$. Based on the model of (19), γ is a function of the drain bias for different channel lengths.

For nanoscale devices with feature sizes below 100 nm, it is still debated whether short-channel effects, as discussed above, are adequate for describing the effects of short-channel noise [44]. Some researchers have suggested that

FIGURE 5: Thermal noise comparison of different analytical noise models.

shot noise is better able to describe the noisy behavior for FETs below 40 nm [34, 45, 46]. As this study focuses on LNA design optimization down to the 90 nm node, it will be assumed that excess thermal noise can be adequately handled through modification of the white noise gamma parameter γ . Experimental results from a number of researchers appear to support this approach [31, 34, 43]. A comparison between the expression for the channel thermal noise in (16) [31] with the thermal noise calculation using the two γ models from [30, 43] have been made. As shown in Figure 5 with the numerical data in Table 1, their results are comparable with a similar trend regarding different channel lengths. Since Scholten et al. [30] and Jeon et al. [43] have completed a relatively in-depth study of the noise parameters and there is relatively good agreement of their work with the analytical model of Deen et al. [31], the noise calculations in this work are carried out based upon the results of [30, 43].

3. Optimization Methods

The optimization of the CMOS LNA design in terms of minimizing its noise figure as the main cost function is considered in this section. The maximum allowed power dissipation is used as the main design constraint as this is a chief concern for modern systems, especially those intended for mobile electronic systems. The influence of other design constraints, such as the quality factor of the input circuit and the input impedance matching requirement, is taken into account during the optimization process. The noise analysis of the LNA and the parameters used to model the noise characteristics of submicron MOSFETs are considered first. Then the device equations needed to model the drain

FIGURE 6: Small signal circuit for noise analysis.

TABLE 1: Thermal noise comparison of different analytical noise models.

Gate length	Power spectral density of channel thermal noise (A^2/Hz)		
	Deen et al. [31]	Scholten et al. [30]	Jeon et al. [43]
90 nm	9.07×10^{-24}	1.04×10^{-23}	1.07×10^{-23}
180 nm	4.22×10^{-24}	4.63×10^{-24}	4.54×10^{-24}
350 nm	9.86×10^{-25}	1.17×10^{-24}	1.41×10^{-24}

current I_{ds} as well as the transconductance g_m and the output conductance g_{d0} are described. Finally, the overall method used to optimize the LNA design within a geometric programming framework is detailed.

3.1. Noise Analysis of the LNA. This subsection describes how the noise figure of the LNA given in Figure 2 can be calculated by small signal analysis. Also, the design parameters used to describe the noise characteristics of short-channel MOSFETs are given. The thermal noise is the major concern at RF intermediate frequencies for MOSFETs. Four noise sources have been considered in this study: the thermal noise of the source resistance ($\bar{i}_{n,R_s}$), the channel thermal noise ($\bar{i}_{n,d}$), the gate noise ($\bar{i}_{n,g}$), and the thermal noise of the output resistance ($\bar{i}_{n,R_{out}}$). These are depicted in Figure 6. The noise contributions due to the gate resistance are factored into the elevated value for the parameter β as discussed below [30]. Neglecting the effect of the gate-to-drain capacitance C_{gd} on the noise calculations introduces a small error but allows closed-form equations to be derived. This error is minimized through the use of a cascode topology, where M_2 mitigates the Miller effect of C_{gd} [12]. The noise contributions of the cascode device M_2 in Figure 2 are considered to be negligible compared to the contributions of the main FET M_1 . Following the observations by [30], the noise contributions of the MOSFET source and bulk resistance are taken to be minimal and are neglected in this analysis.

The contributions of these four noise sources referred to the output are denoted by $\bar{i}_{n,o,R_s}$, $\bar{i}_{n,o,d}$, $\bar{i}_{n,o,g}$, and $\bar{i}_{n,o,R_{out}}$, respectively. Table 2 summarizes the expressions for these noise sources [9, 47].

TABLE 2: Output-referred noise equations.

Noise source	Expression	Output-referred expression
R_s	$\bar{i}_{n,R_s}^2 = 4kT \frac{1}{R_s} \Delta f$	$\bar{i}_{n,o,R_s} = \frac{g_m}{j2\omega_0 C_{tot}} \bar{i}_{n,R_s}$
$\bar{i}_{n,d}$	$\bar{i}_{n,d}^2 = 4kT \gamma g_{d0} \Delta f$	$\bar{i}_{n,o,d} = -\frac{1}{2} \bar{i}_{n,d}$
$\bar{i}_{n,g}$	$\bar{i}_{n,g}^2 = 4kT \beta g_g \Delta f$	$\bar{i}_{n,o,g} = \frac{g_m}{j\omega_0 C_{tot}} \frac{1 - jR_s \omega_0 C_{tot}}{j2R_s \omega_0 C_{tot}} \bar{i}_{n,g}$
R_{out}	$\bar{i}_{n,R_{out}}^2 = 4kT \frac{1}{R_{out}} \Delta f$	$\bar{i}_{n,o,R_{out}} = \bar{i}_{n,R_{out}}$

The correlation between the induced gate noise and the channel thermal noise is represented by $\bar{i}_{n,o,corr}$. Therefore, the LNA noise factor can be expressed as

$$F = \frac{\bar{i}_{n,o,R_s}^2 + \bar{i}_{n,o,d}^2 + \bar{i}_{n,o,g}^2 + \bar{i}_{n,o,corr}^2 + \bar{i}_{n,o,R_{out}}^2}{\bar{i}_{n,o,R_s}^2}. \quad (20)$$

Then, the noise factor at resonance is obtained as

$$F = 1 + \frac{(1/4) \gamma g_{d0} + g_m^2 (C_{gs}/C_{tot})^2 (Q^2 + 1/4) \beta / (5g_{d0}) + g_m c (C_{gs}/C_{tot}) \sqrt{(\gamma \cdot \beta) / 20} + 1/R_{out}}{g_m^2 R_s Q^2}, \quad (21)$$

where γ is defined by (5), β is the gate noise parameter, c is the correlation coefficient, C_{gs} is the intrinsic gate capacitance, C_{tot} is the sum of C_{gs} and C_e , and Q is the quality factor of the input circuit.

Based on the studies by [30, 31, 43], the white noise factor γ is assumed to be independent of the operating frequencies up to 10 GHz and to be independent of bias conditions. A comparison of the values γ versus FET channel length is given in Figure 7.

The measured and analytical γ compare favorably when observed at various gate lengths (e.g., 90 nm, 180 nm, and 350 nm), as shown in Figure 7. As expected, the white noise factor γ increases when the channel length decreases. For long-channel devices (channel lengths greater than 1 μ m), the traditional value for γ is 2/3.

Numerical values for the gate noise parameter β and correlation coefficient c are estimated from [30, 43] and are summarized, along with the parameter γ , in Table 3. There is a significant increase in the value of the parameter β as the channel length decreases due to the contribution from the gate resistance, which consists of the resistance of the vias, the effective resistance of the silicide, and the contact resistance between the silicide and polysilicon layers [30, 33]. The value of β is close to 4/3 for long-channel devices, but more than doubles in value for 180 nm devices. Therefore, a significant increase is predicted for devices at the 90 nm node. The magnitude of the correlation coefficient is 0.395 for long-channel devices [8], and it decreases due to larger γ and β when channel length reduces in size as can be inferred from (C.3) in Appendix C. A reasonable approximation is that the values for the parameters β and c are relatively independent of frequency and variations with bias conditions for strong inversion. Scholten et al. [30, 48] have shown that modeling the gate noise power spectral density S_{i_g} with a constant value for β using (7) gives a good fit to experimentally measured results for short-channel devices over a range of applied voltages up to 10 GHz. They also show that the correlation coefficient c is relatively independent of frequency and bias voltage.

In order to determine the sensitivity to γ and β in the calculation of the minimum noise figure, the effect of varying these parameters was analyzed (see Appendix D for further details). When a $\pm 10\%$ variation is applied to γ , a small percentage of variation (around 4%) occurs to the minimum noise figure. Similarly, less than 4% variation occurs on the minimum noise figure when a $\pm 10\%$ change is applied to β . This gives confidence to the assumption that the parameters γ and β can be modeled as constants for a given technology node without adversely affecting the optimization results.

3.2. Device Equations for Submicron FETs. This subsection outlines how the device models that take into account short-channel effects can be developed in a form suitable for geometric programming. As device geometries approach submicron dimensions and below, various high field effects such as velocity saturation and channel length modulation must be taken into consideration. A piece-wise model of the drain current I_{ds} which includes these effects has been used in this analysis [38]:

$$\begin{aligned} I_{ds} &= \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \cdot \frac{V_{od} V_{ds} - (m/2) V_{ds}^2}{1 + (\mu_{eff} V_{ds}) / (2v_{sat} L)}, \\ I_{dsat} &= \frac{\mu_{eff} C_{ox} (W/L) (V_{od}^2 / (2m)) (1 + \lambda V_{ds})}{1 + \mu_{eff} V_{od} / (2mv_{sat} L)}, \\ \mu_{eff} &= \frac{\mu_0}{1 + \theta V_{od}}, \end{aligned} \quad (22)$$

where m is the body effect factor, v_{sat} is velocity saturation, μ_{eff} is effective mobility in m^2/V , μ_0 is normal field mobility, and θ is normal field mobility degradation factor in V^{-1} . In (21), the transconductance g_m and the output conductance g_{d0} are the two main technology-dependent parameters. Analytical solutions are obtained for g_m and g_{d0} by taking the derivative of the closed-form analytical drain current solutions for

FIGURE 7: White noise factor γ versus gate length.

TABLE 3: Noise parameters for the noise analyses for 90 nm and 180 nm CMOS processes.

Parameters	90 nm design	180 nm design
White noise factor (γ)	1.2	1.05
Gate noise parameter (β)	7.5	3.8
Correlation coefficient (c)	0.2	0.2

short-channel CMOS transistors (see Appendix A), yielding the following equations:

$$g_m = \frac{C_{ox}\mu_0 W v_{sat} \cdot (1 + \lambda V_{ds}) (4m v_{sat} L V_{od} + (2m v_{sat} L \theta + \mu_0) V_{od}^2)}{(2m v_{sat} L + (2m v_{sat} L \theta + \mu_0) V_{od})^2}, \quad (23)$$

$$g_d = \frac{\mu_{eff} C_{ox} (W/L) [V_{od} - m V_{ds} - (m/2) (\mu_{eff} / (2v_{sat} L)) V_{ds}^2]}{(1 + (\mu_{eff} V_{ds}) / (2v_{sat} L))^2}.$$

Then the channel conductance at zero bias condition is

$$g_{d0} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) V_{od}. \quad (24)$$

The final expressions for g_m and g_{d0} will need to be placed in a form suitable for geometric programming as described below.

3.3. Geometric Programming Optimization of the LNA. A geometric program solves an optimization problem where the objective function is in the form of a posynomial function and the constraints are expressed as posynomial inequalities and monomial equalities. All design parameters are nonnegative variables. A monomial function has the following form [19]:

$$g(x) = c x_1^{a_1} x_2^{a_2} x_3^{a_3} \cdots x_n^{a_n}, \quad (25)$$

where c is a positive constant ($c > 0$), $x_1, x_2, \dots$, and x_n are real positive variables, and $a_1, a_2, \dots$, and a_n are constants known as the exponents of the monomial. Any positive constant is a monomial. Monomials are closed under multiplication and division. A posynomial function is a sum of one or more monomial functions as shown in the following equation:

$$f(x) = \sum_{k=1}^K c_k x_1^{a_{1k}} x_2^{a_{2k}} x_3^{a_{3k}} \cdots x_n^{a_{nk}}, \quad (26)$$

where $c_k > 0$. Note that posynomial functions are also closed under addition and multiplication. A standard form for a geometric programming can be defined as an optimization problem with the following form:

Minimize an objective function: $f_0(x)$
subject to constraints:

$$\begin{aligned} f_i(x) &\leq 1, \quad i = 1, \dots, m, \\ g_i(x) &= 1, \quad i = 1, \dots, p, \end{aligned} \quad (27)$$

where $x = (x_1, \dots, x_n)$ is a vector with components x_i , $f_0(x)$ is an objective function with the form of a posynomial function, $f_1(x), f_2(x), \dots, f_m(x)$ are posynomial functions, $g_1(x), g_2(x), \dots, g_p(x)$ are monomial functions, and x_i are the optimization variables (x_i are always greater than zero) [19].

The objective function for this optimization problem is to minimize the noise figure NF, which is already in a posynomial form. Most of the design constraints are either in a posynomial form or monomial form. The main challenge is to translate the analytical expressions for the device transconductance (g_m) and output conductance (g_{d0}) in (23) into a form suitable for geometric programming. Following the work of [19], a curve-fitting approach is used to obtain monomial expressions for g_m and g_{d0} :

$$\begin{aligned} g_m &= A_0 L^{A_1} W^{A_2} I_{ds}^{A_3}, \\ g_{d0} &= B_0 L^{B_1} W^{B_2} I_{ds}^{B_3}. \end{aligned} \quad (28)$$

The details on the curve fitting and the resulting fitting parameters are given in Appendix B.

Process-dependent parameters for 90 nm and 180 nm technology nodes were derived from the SPICE model files provided by a predictive technology model (PTM) [49, 50]. Furthermore, the vertical field mobility degradation factor θ , the channel-length modulation parameter λ , and the body effect coefficient m were extracted from the device characterizations provided by running SPICE simulations using the PTM models. The relevant parameters are summarized in Table 4.

In addition to the noise figure, the major design constraints for LNAs include the quality factor, input impedance matching, and power consumption. Due to the resonant behavior of the circuit, the quality factor of the input circuit at the resonant frequency ω_0 is given by

$$Q = \frac{1}{R_{tot} \omega_0 C_{tot}} = \frac{1}{2R_s \omega_0 C_{tot}}. \quad (29)$$

TABLE 4: Technology parameters for 90 nm and 180 nm CMOS processes.

Parameters	90 nm	180 nm
Electron mobility μ_0	0.0179 m ² /V	0.0288 m ² /V
Electron velocity saturation v_{sat}	1.10×10^5 m/s	9.18×10^5 m/s
Oxide capacitance per unit area C_{ox}	0.014 F/m ²	0.00857 F/m ²
Body effect coefficient m	1.21	1.18
Vertical field mobility degradation factor θ	0.3 V^{-1}	0.2 V^{-1}
Channel-length modulation parameter λ	0.4 V^{-1}	0.3 V^{-1}

To maximize the power transfer, the input impedance of the LNA is required to match the source input impedance, which is assumed to be 50Ω . The impedance matching constraints can be expressed as

$$\omega_0 = \frac{1}{\sqrt{L_{\text{tot}} \cdot C_{\text{tot}}}}, \quad (30)$$

$$R_s = \frac{g_m}{C_{\text{tot}}} L_s = 50 \text{ ohms},$$

where L_{tot} is the sum of L_g and L_s .

The optimization problem using geometric programming can then be expressed as follows:

Minimize an objective function: Noise factor F in (20)
subject to design constraints:

$$L = L_{\text{feature size}},$$

$$1 \mu\text{m} \leq W \leq 100 \mu\text{m},$$

$$\frac{C_{\text{gs}}}{C_{\text{tot}}} \leq 1,$$

$$\frac{3}{2} \frac{C_{\text{gs}}}{C_{\text{ox}} W L} = 1, \quad (31)$$

$$\frac{g_m L_s}{C_{\text{tot}}} = 50 \Omega,$$

$$I_{\text{ds}} \cdot V_{\text{DD}} \leq P_{\text{Dmax}},$$

$$g_m = A_0 L^{A_1} W^{A_2} I_{\text{ds}}^{A_3},$$

$$g_{d0} = B_0 L^{B_1} W^{B_2} I_{\text{ds}}^{B_3}.$$

For the 90 nm process, $L_{\text{feature size}} = 90 \text{ nm}$, $V_{\text{DD}} = 2 \text{ V}$, and the maximum power dissipation P_{Dmax} is set at 1 mW. For the 180 nm process and $L_{\text{feature size}} = 180 \text{ nm}$, $V_{\text{DD}} = 3 \text{ V}$ and $P_{\text{Dmax}} = 1.5 \text{ mW}$. The current I_{ds} is the drain-to-source current through device M_1 in this design.

4. Results and Discussion

The optimal design of the CMOS LNA has been computed using CVX, a package for specifying and solving geometric

TABLE 5: Optimal design results for low-noise amplifier when input circuit quality factor $Q = 4$ and output circuit quality factor $Q_{\text{out}} = 5$.

Parameters	90 nm	180 nm
Output conductance (g_{d0})	0.0082 S	0.0063 S
Transconductance (g_m)	0.0069 S	0.0052 S
Gate width (W)	22.172 μm	27.006 μm
Gate length (L)	90 nm	180 nm
P factor ($P = C_{\text{gs}}/C_{\text{tot}}$)	0.1128	0.1681
Gate intrinsic capacitance (C_{gs})	18.696 fF	27.87 fF
Additional capacitance (C_e)	0.147 pF	0.13792 pF
Source inductor (L_s)	1.2063 nH	1.5828 nH
Gate inductor (L_g)	25.32 nH	24.943 nH
Drain current (I_{ds})	0.5 mA	0.5 mA
Minimum noise figure (F_{min})	0.6076 dB	0.8229 dB

programming problems [51]. The average execution time was about 1.45 seconds on a 3.23 GHz PC with 4 GB memory. The resulting optimal design parameters are shown in Table 5.

The results from the optimal design using geometric programming have been compared with results from Agilent's Advanced Design System (ADS) software, a numerical simulation tool used for RF design. The input FET M_1 was biased at 0.5 mA and the power supply was set to 2 V with the values of L_g , L_s , and C_e determined by the constraints used in the GP optimization. The output parallel RLC values are calculated by the output circuit quality factor, which is given as 5 in this study. For the 90 nm design, ADS simulations indicate that the minimum noise figure is 0.2799 dB for a gate width of 27 μm , while the optimal width from the optimization of geometric programming is 22.172 μm with a minimum noise figure of 0.6076 dB. For the 180 nm design, a minimum noise figure of 0.7708 dB was obtained for a gate width of 20 μm , while the optimal width from the optimization of geometric programming is 27.006 μm with a minimum noise figure of 0.8229 dB. As shown in Figure 8, the minimum noise figures from the ADS simulations are smaller than the minimum noise figures from the GP results. These discrepancies likely are caused by the lack of implementation of the excess thermal noise in the BSIM3 MOSFET models. The 90 nm design displays relatively larger differences than the 180 nm design, which is not unexpected as excess noise is more significant in shorter channel devices. The optimal widths for minimizing the NF from the GP optimization and ADS simulations are not an exact match, but the overall trends are fairly close. This indicates that geometric programming, which can rapidly find an optimal point, can be used to guide the design of short-channel CMOS LNAs. A good design methodology will then use detailed circuit simulations to fine tune the design and verify its performance. As current simulation models do not adequately account for excess thermal noise, some additional analysis based on experimentally determined FET noise characteristics will be required by the designer to ensure that the optimal design is found.

FIGURE 8: Variations of noise figure with different gate width and $Q = 4$.

It should be noted that the inductor value of 25 nH for L_g would not be economical in terms of area when implemented as an on-chip planar spiral inductor. A prudent design choice would be to implement part of the inductance on the chip and the rest through the bond wire; alternatively, one could use the bond wire plus an external inductor on the printed circuit board [1]. Also advances in materials and fabrication technologies have made it possible to embed high quality inductors on the order of 20 nH to 30 nH in a package substrate that are suitable for RF applications [52, 53].

Tradeoff analyses were performed to examine the influence of the quality factor and drain current on the design of short-channel CMOS LNAs. As the optimization results for LNAs designed in 90 nm and 180 nm processes are similar, the trade-off analysis for the 90 nm case is presented in this paper. An inverse relationship is observed between the quality factor and the minimum noise figure, as seen in Figure 9(a). When the input quality factor increases from 2 to 8, the minimum noise figure decreases from 1 dB to 0.39 dB. The quality factor not only affects the minimal noise figure but also influences the optimal width of the LNAs. When the quality factor varies from 2 to 8, the optimal width changes almost 10 times from 75 μm to 6.7 μm , as seen in Figure 9(b). This considerable change in the optimal width indicates the importance of the quality factor in determining the optimal width of M_1 .

The drain current appears to have great influence on the noise figure when the drain current is at a relatively small scale (i.e., less than 0.5 mA). However, there is not much variation in the noise figure when the drain current increases from 1 mA to 5 mA, as shown in Figure 10. Such an observation is true at different levels of channel width. This suggests that, for this 90 nm process, the best balance between power dissipation, area, and noise figure exists when the LNA is biased with 0.5 to 1.0 mA of current. When the channel width is set to 20 μm , the optimal range for the input circuit quality factor is from 4 to 6. This observation is consistent with the results reported in [9].

FIGURE 9: (a) Variation of minimal noise figure with different input quality factors Q and (b) variation of the optimal width with different quality factors.

FIGURE 10: Effect of drain current and channel width on the noise figure (90 nm).

Variations in the frequency of operation also have a significant influence on the noise figure (Figures 11 and 12). In many applications, an RF LNA will be optimized for a particular narrowband of operation, for example, at 2.4 GHz. Therefore, the influence of operational frequency on the noise figure will be limited, and there is a clear choice for the optimum device width for minimizing the noise figure.

In sum, our results show that the use of geometric programming allows the global optimal design optimization of an LNA to be obtained with great efficiency. This study has focused on the common LNA configuration that uses source inductive degeneration. Short-channel effects have been taken into account when modeling the electronic noise in the MOSFETs as well as in the device characteristics. While some approximations must be made to put the equations in the proper form required by a GP framework, the results are guaranteed to return a globally optimum solution. Various trade-off analyses can be efficiently run as well under given constraints, such as power dissipation and input quality factor. For example, the input circuit quality factor has a great influence on not only the minimum noise figure but also the optimal width. Our results, in general, align well with other results in the literature. In the particular case of the 90 nm technology node used in this study, one can

FIGURE 11: Effect of channel width on the noise figure at different frequencies.

FIGURE 12: Effect of operational frequency and channel width on the noise figure.

quickly determine the “sweet spot” in the design. The trade-off analyses in this case indicate that the best designs in terms of power and noise figure for the LNA design occur when the drain current is in the range of 0.5 mA to 1 mA with an input circuit quality factor around 5.

5. Summary and Future Directions

This paper has examined the use of geometric programming for obtaining the globally optimum design of RF CMOS LNAs implemented with short-channel devices. The main contribution of this work has been the development of a framework for noise modeling of short-channel devices by including short-channel effects including velocity saturation and channel-length modulation. This noise model forms the basis of the objective function for geometric programming to minimize the noise figure of CMOS LNAs. In addition, the noise figure is minimized subject to the design constraints of input circuit quality factor, power consumption, and input impedance matching. Specific results from the optimization procedure are applied at the 90 nm and 180 nm technology nodes to determine the optimal channel width and noise figure for RF CMOS LNAs. Trade-off analysis indicates some important relationships among the design parameters such as the inverse relationship between noise figure and input circuit

quality factor. The relationship between the noise figure and channel width at a given power dissipation and the input circuit quality factor are consistent with simulations from Agilent’s ADS software. The overall design trends are also consistent with other studies reported in the literature. Hence, this study has validated the use of geometric programming as an efficient method to guide the optimal design of CMOS LNAs targeted for implementation at nanoscale technology nodes.

Future work will focus on the enhancement of noise modeling for short-channel CMOS LNAs. For example, the noise contributions from the gate inductor (L_g) and the source inductor (L_s) due to their finite quality factor caused by parasitic effects should be included in the analysis. As devices continue to scale to deep submicron nodes, the doping concentration in the substrate will increase. This affects how the device characteristics are modelled such as the relationship between carrier mobility and diffusivity. In addition, quantum effects should be included when modeling the noise in the channel current [31]. It is expected that more sophisticated equivalent circuit models will be required to model the physical effects of nanoscale devices. The effect of the substrate as a source of noise and the back-gate transconductance in the small signal model should be considered. The thinning of the gate oxide at aggressively scaled technologies may make gate leakage effects an important consideration. Other sources of noise, such as shot noise, should also be taken into consideration below the 40 nm node. The existing noise optimization framework using GP can be modified to include these effects. In addition, the application of GP optimization for other topologies, such as the shunt-series feedback amplifier, will be considered in future work. Finally, with the trend towards biasing analog circuits in the weak to moderate inversion regions to reduce power dissipation, it would be interesting to explore GP methods as outlined in this paper to optimize these circuits.

Appendices

A. Expressions for MOSFET Output Conductance and Transconductance

In this appendix, analytical expressions for the output conductance and transconductance are discussed for both long-channel devices and short-channel devices.

A.1. Derivations of g_{d0} and g_m for Long-Channel Devices. For long-channel devices, the well-known expressions of the drain current in both the triode region and saturation region are given as

$$I_{d\text{triode}} = \mu_0 C_{\text{ox}} \frac{W}{L} \left(V_{\text{od}} \cdot V_{\text{ds}} - \frac{1}{2} V_{\text{ds}}^2 \right), \quad (\text{A.1})$$

$$I_{d\text{sat}} = \frac{1}{2} \mu_0 C_{\text{ox}} \frac{W}{L} V_{\text{od}}^2,$$

where $V_{od} = V_{gs} - V_{th}$. By definition, the output conductance g_d is

$$g_d = \left. \frac{\partial I_{dtriode}}{\partial V_{ds}} \right|_{V_{gs}} = \mu_0 C_{ox} \frac{W}{L} (V_{od} - V_{ds}). \quad (A.2)$$

Therefore, the output conductance at zero bias (i.e., $V_{ds} = 0$), can be expressed by

$$g_{d0} = g_d|_{V_{ds}=0} = \mu_0 C_{ox} \frac{W}{L} V_{od} = \sqrt{2 \frac{W}{L} \mu_0 C_{ox} I_{dsat}}. \quad (A.3)$$

The transconductance of a long-channel device in saturation is given as

$$g_m = \left. \frac{\partial I_{dsat}}{\partial V_{gs}} \right|_{V_{ds}} = \mu_0 C_{ox} \frac{W}{L} \cdot V_{od} = \sqrt{2 \frac{W}{L} \mu_0 C_{ox} I_{dsat}}. \quad (A.4)$$

For long-channel devices, it is obvious that the output conductance at zero bias g_{d0} has the same form as the transconductance in saturation in terms of V_{od} or I_{dsat} .

A.2. Derivations of g_{d0} and g_m for Short-Channel Devices. The drain current for short-channel devices is expressed differently than for the long-channel devices. By taking some important short-channel effects into account, such as velocity saturation and channel-length modulation, the expressions of

the analytical drain current model in both the triode region and saturation region are given by [38]

$$\begin{aligned} I_{dtriode} &= \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \cdot \frac{(V_{gs} - V_{th}) V_{ds} - (m/2) V_{ds}^2}{1 + (\mu_{eff} V_{ds}) / (2v_{sat} L)}, \\ I_{dsat} &= \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \frac{(V_{gs} - V_{th})^2 / (2m)}{1 + \mu_{eff} (V_{gs} - V_{th}) / (2mv_{sat} L)} \\ &\quad \cdot (1 + \lambda V_{ds}), \end{aligned} \quad (A.5)$$

where [38, 41]

$$\mu_{eff} = \frac{\mu_0}{1 + \theta (V_{gs} - V_{th})}, \quad (A.6)$$

$$\theta = \frac{\beta_\theta}{t_{ox}}, \quad (A.7)$$

$$m = 1 + \frac{\sqrt{\epsilon_{si} q N_{ch} / (4 \Psi_B)}}{C_{ox}}, \quad (A.8)$$

$$\Psi_B = \left(\frac{kT}{q} \right) \ln \left(\frac{N_{ch}}{n_i} \right). \quad (A.9)$$

After applying the quotient rule, the output conductance g_d can be expressed as

$$\begin{aligned} g_d &= \left. \frac{\partial I_{dtriode}}{\partial V_{ds}} \right|_{V_{gs}} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \frac{(V_{od} - mV_{ds}) \cdot (1 + \mu_{eff} V_{ds} / (2v_{sat} L)) - (V_{od} V_{ds} - (m/2) V_{ds}^2) \cdot (\mu_{eff} / (2v_{sat} L))}{(1 + \mu_{eff} V_{ds} / (2v_{sat} L))^2} \\ &= \frac{\mu_{eff} C_{ox} (W/L) [V_{od} - mV_{ds} - (m/2) (\mu_{eff} / (2v_{sat} L)) V_{ds}^2]}{(1 + \mu_{eff} V_{ds} / (2v_{sat} L))^2}. \end{aligned} \quad (A.10)$$

Therefore, the output conductance at zero bias ($V_{ds} = 0$) can be expressed by

$$g_{d0} = g_d|_{V_{ds}=0} = \frac{\mu_0}{1 + \theta V_{od}} C_{ox} \frac{W}{L} V_{od}. \quad (A.11)$$

By substituting the effective mobility equation into the saturation drain current formula, the equation of I_{dsat} for short-channel devices can be rewritten as

$$\begin{aligned} I_{dsat} &= \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \frac{(V_{gs} - V_{th})^2 / (2m)}{1 + \mu_{eff} (V_{gs} - V_{th}) / (2mv_{sat} L)} \\ &\quad \cdot (1 + \lambda V_{ds}). \end{aligned} \quad (A.12)$$

Using (A.6) and (A.12), the transconductance of a short-channel device in saturation is given as

$$\begin{aligned} g_m &= \left. \frac{\partial I_{dsat}}{\partial V_{gs}} \right|_{V_{ds}} \\ &= C_{ox} \mu_0 \left(\frac{W}{L} \right) \frac{1}{2m} (1 + \lambda V_{ds}) \\ &\quad \cdot \left[\frac{V_{od}^2}{(1 + \theta V_{od} + (\mu_0 / (2mv_{sat} L)) V_{od})} \right]' \\ &= C_{ox} \mu_0 W v_{sat} \cdot (1 + \lambda V_{ds}) \\ &\quad \cdot \frac{4mv_{sat} L V_{od} + (2mv_{sat} L \theta + \mu_0) V_{od}^2}{(2mv_{sat} L + (2mv_{sat} L \theta + \mu_0) V_{od})^2}. \end{aligned} \quad (A.13)$$

B. Monomial Expressions for g_m and g_{d0}

This appendix describes how a curve-fitting approach is used to determine monomial expressions for the transconductance (g_m) and output conductance (g_{d0}) from the analytical expressions derived in Appendix A. Monomial expressions of transconductance (g_m) and output conductance (g_{d0}) are given by

$$\begin{aligned} g_m &= A_0 L^{A_1} W^{A_2} I_{ds}^{A_3}; \\ g_{d0} &= B_0 L^{B_1} W^{B_2} I_{ds}^{B_3}. \end{aligned} \quad (B.1)$$

The geometry ranges specified for the devices for the monomial curve-fitting are given in Table 6(a). Additionally, the bias conditions are chosen to ensure the transistors operate in the saturation regions; for example, $V_{ds} \geq V_{od}$ as shown in Table 6(a). The fitting parameters that were determined from the above process are listed in Table 6(b) for both the 90 nm and 180 nm CMOS processes used in this study.

The accuracy of the curve fitting has been examined by comparing the estimated transconductance (g_m) and output conductance (g_{d0}) from the monomial expressions with calculated values from the analytical solutions.

The curve fitting results for the 90 nm process are shown in Figures 13 and 14. The coefficient of determination (R^2 value) for the transconductance curve fitting is 0.9999, indicating that the regression fits extremely well with the data compared with the analytical solutions in (23). The maximum relative error from curving fitting is about 2.56% (Figure 13(a)). Furthermore, 98.2% of the curve fitting data has a relative error less than 1.0% (Figure 13(b)).

The coefficient of determination for the output conductance is 1.0, suggesting that the curve fitting is close to perfect. The accuracy of curve fitting is shown in Figure 14(a) with a maximum relative error of 0.97%. Moreover, among this curve fitting data, 99.99% of the points have a relative error of less than 0.96% (Figure 14(b)).

The curve fitting results are shown in Figures 15 and 16 for the 180 nm process. The coefficients of determination (R^2 value) for these two curve fittings are very close to 1 and more than 97% of curve fitting data have a relative error less than 1.0% for both cases.

C. Expression for the Correlation Coefficient

This appendix describes the calculation of correlation coefficient c following [8]. Since the induced gate noise is correlated with the drain thermal noise, the correlation coefficient is defined as

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}}, \quad (C.1)$$

where $\overline{i_{ng} \cdot i_{nd}^*}$ is the spectrum of the cross-correlation of the drain thermal noise and the induced gate noise, $\overline{i_{nd}^2}$ is the spectrum of the drain thermal noise and $\overline{i_{ng}^2}$ is the spectrum

TABLE 6: (a) Ranges of devices geometry and bias conditions for calculation of g_m and g_{d0} for 90 nm and 180 nm CMOS processes. (b) Fitting parameters of monomial expressions of g_m and g_{d0} for 90 nm and 180 nm CMOS processes.

(a)		
Parameters	90 nm	180 nm
Gate length L	$0.09 \mu\text{m} \leq L \leq 0.45 \mu\text{m}$	$0.18 \mu\text{m} \leq L \leq 0.9 \mu\text{m}$
Gate width W	$1 \mu\text{m} \leq W \leq 100 \mu\text{m}$	$1 \mu\text{m} \leq W \leq 100 \mu\text{m}$
Overdrive voltage V_{od}	$0.1 \text{ V} \leq V_{od} \leq 0.4 \text{ V}$	$0.1 \text{ V} \leq V_{od} \leq 0.5 \text{ V}$
Drain to source voltage V_{ds}	$0.5 \text{ V} \leq V_{ds} \leq 1.0 \text{ V}$	$0.6 \text{ V} \leq V_{ds} \leq 1.2 \text{ V}$
(b)		
Parameters	90 nm	180 nm
A_0	0.0423	0.0463
A_1	-0.4578	-0.4489
A_2	0.5275	0.5311
A_3	0.4725	0.4689
B_0	0.0091	0.0096
B_1	-0.5637	-0.5595
B_2	0.5305	0.5194
B_3	0.4695	0.4806

of the induced gate noise. In a long-channel device, they are given as [8]

$$\begin{aligned} \overline{i_{ng} \cdot i_{nd}^*} &= 4kT \cdot \frac{1}{9} j\omega (C_{ox}WL) \cdot \Delta f, \\ \overline{i_{n,d}^2} &= 4kT \gamma_{long} g_{d0} \Delta f, \\ \overline{i_{n,g}^2} &= 4kT \beta_{long} g_g \Delta f, \end{aligned} \quad (C.2)$$

where g_g is given by (8) and $C_{gs} = (2/3)C_{ox}WL$. By substitution of (C.2) into (C.1), the correlation coefficient c for long-channel can be calculated as

$$c = \frac{1}{6\sqrt{(1/5)\beta_{long} \cdot \gamma_{long}}} j. \quad (C.3)$$

Substituting β_{long} and γ_{long} with their corresponding long-channel values of 4/3 and 2/3 yields $c = \sqrt{5/32}j = 0.395j$.

D. Sensitivity of the γ and β Parameters

This appendix shows the sensitivity of the γ and β parameters on the calculation of the minimum noise figure. The effect of varying the γ parameter is shown in Figure 17. When a $\pm 10\%$ variation is applied to γ , a small percentage of variation (around 4%) occurs to the minimum noise figure. Similarly, less than 4% variation occurs on the minimum noise figure when a $\pm 10\%$ change is applied to β , as illustrated in Figure 18.

FIGURE 13: (a) Histogram of relative error for curve fitting of g_m for 90 nm. (b) Cumulative density function of relative error for curve fitting of g_m for 90 nm.

FIGURE 14: (a) Histogram of relative error for curve fitting of g_{d0} for 90 nm. (b) Cumulative density function of relative error for curve fitting of g_{d0} for 90 nm.

FIGURE 15: (a) Histogram of relative error for curve fitting of g_m for 180 nm. (b) Cumulative density function of relative error for curve fitting of g_m for 180 nm.

FIGURE 16: (a) Histogram of relative error for curve fitting of g_{d0} for 180 nm. (b) Cumulative density function of relative error for curve fitting of g_{d0} for 180 nm.

FIGURE 17: Variation of γ factor on the minimum noise figure for a nominal value of $\gamma = 1.2$.

FIGURE 18: Variation of β factor on the minimum noise figure for a nominal value of $\beta = 7.5$.

This gives confidence to the assumption that the parameters γ and β can be modeled as constants for the purposes of optimization.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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