Research Article

A Modularized Noise Analysis Method with Its Application in Readout Circuit Design

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A readout integrated circuit (ROIC) is a crucial part that determines the quality of imaging. In order to analyze the noise of a ROIC with distinct illustration of each noise source transferring, a modularized noise analysis method is proposed whose application is applied for a ROIC cell, where all the MOSFETs are optimized in subthreshold region, leading to the power dissipation $2.8 \mu\text{W}$. The modularized noise analysis begins with the noise model built using transfer functions and afterwards presents the transfer process of noise in the form of matrix, through which we can describe the contribution of each noise source to the whole output noise clearly, besides optimizing the values of key components. The optimal noise performance is obtained under the limitation of layout area less than $30 \mu\text{m} \times 30 \mu\text{m}$, resulting in that the integration capacitor should be selected as 0.74 pF to achieve an optimal noise performance, the whole output noise reaching the minimum value at $74.1 \mu\text{V}$. In the end transient simulations utilizing Verilog-A are carried out for comparisons. The results showing good agreement verify the feasibility of the method presented through matrix.

1. Introduction

An infrared detector has a wide range of applications in areas of military, research, and manufacture, whose core part is an infrared focal plane assembly [1, 2]. The assembly mainly consists of two parts, a focal plane array (FPA) that functions to convert radiation to current signal and a readout integrated circuit (ROIC) that is responsible for realization of serial processing of signals sampled from the FPA [3].

As an essential part of the signal chain, the research on integrators and correlated double sampler (CDS) has been highlighted since they were invented, alongside with the character of noise transferring from end to end, which is affected by various factors like amplifying, sampling, filtering, and so on. An integrator conducts current signals through an integration capacitor to be transformed into voltages, which inevitably induces strong reset noise. So a CDS has to be used to suppress it, which also subtracts the reference voltage from the output to present a net integration voltage.

Applications of FPAs with large format and high resolution put forward more harsh demands on the small layout area. In order to give an optimization for noise performance of a ROIC, a modularized noise analysis method is proposed for a readout cell, consisting of an integrator and a new type of correlated double sampler (CDS), both of which are switched capacitor circuits, where all the MOSFETs are optimized in subthreshold region to be acceptable to the power limitation of large format FPAs [4, 5]. The modularized noise analysis begins with the architecture of the readout cell that is for pixel level ROICs, operating in snapshot mode. Afterwards the noise model is built using transfer functions and the method of presenting the transfer process of noise in the form of matrix is given, through which we can describe the contribution of each noise source to the whole output noise distinctly. In the end, calculations of noise for the proposed readout cell are carried out by the transfer function method and transient simulations utilizing Verilog-A, respectively. The results due to the two methods show good agreement.

FIGURE 1: Architecture of snapshot ROIC.

2. Architecture of the ROIC

Figure 1 depicts the architecture of the ROIC, whose readout timing operates on pixel level. Snapshot mode is employed. Each pixel corresponds to each readout unit cell, which are connected electrically through indium bump [6]. All the pixels are exposed to radiation simultaneously and transfer the generated photocurrent to the corresponding readout unit cells. Utilizing the architecture provides the capability of expanding integration time, which can adapt to the situation of low intensity radiation [7]. After an integration period ends, with the control of digital logical signals, the integration voltage maintained in each readout unit cell is transmitted serially through a multiplexer and then delivered outside the ROIC through a buffer.

3. Design of the Readout Unit Cell

The structure of the proposed readout unit cell is shown in Figure 2, constituted by two parts, an integrator and a CDS. The integrator adopts the CTIA structure, which provides

nearly 100% injection efficiency and linearity. Meanwhile the CDS is composed of three OPs, A_2 , A_3 , and A_4 , connected as buffers, two sampling capacitors, and four complementary switches, S_1 , S_2 , S_3 , and S_4 . From those A_2 and A_3 act to isolate switching operations between the former and latter circuit part.

Herein the structure we proposed is compared with four different ROIC unit cells in [8–11]. The added CDS part provides the capability of suppressing low frequency noise from reset operation and photocurrent for the proposed ROIC one which in aspect of noise performance surpasses those referred to in [8–10] without CDS circuits. The linearity of the BDI structure in [11] can reach 99% which is high enough for the type of structure while for the CTIA type like the one we proposed and these in [8–10] it is easy to achieve more than 99.5% linearity; besides, the power dissipation of the two types makes no difference if the static power of the OP involved is the same. Thus how to choose the most suitable OP and optimize the power dissipation of the OPs involved is another crucial problem.

FIGURE 2: Structure of the proposed readout unit cell.

TABLE 1: Performance comparison.

	Gain	Output range	Speed	Power	Noise
Cascade OP	Medium	Medium	High	Low	Low
Folded cascade OP	Medium	Medium	High	Medium	Medium
Two-stage OP	High	High	Low	Medium	Low
Gain boost OP	High	Medium	Medium	High	Medium

Several types of structure of OP are able to be used for the proposed unit cell, such as cascade OP, folded cascade OP, two-stage OP, and gain boost OP. Table 1 gives the comparison among them [12]. From Table 1 we see that, except for the speed disadvantage, the two-stage OP is the best choice, as shown in Figure 3, which just maintains medium power obtaining high gain which can guarantee low static error. On account of the application of the proposed ROIC unit for infrared image acquisition, the clock operations are not in a high frequency, so the speed of the OPs is easy to achieve in either of the OP types.

Introduction of operational amplifiers (OPs) which consumes more power will sacrifice the performance of power dissipation of circuits inevitably. Especially for the structure of the ROIC unit cell we proposed, four OPs are needed for an individual unit cell. To overcome the shortcoming, subthreshold technology is applied [4, 5, 13]. Subthreshold technology is operating transistors in subthreshold region by providing gate-to-source voltage lower than threshold voltage ($V_{gs} < V_{th}$). Ideally, when V_{gs} is lower than V_{th} , the channel between source and drain is shut down. Nevertheless, some electrons still flow across the two ports, known as subthreshold current. Research demonstrates that the subthreshold current is increasing exponentially with the V_{gs} increase, like the current in BJT. The relationship can be expressed as

$$I_{sub} = I_0 e^{(V_{gs} - V_{th})/nV_T} (1 - e^{-V_{ds}/V_T}), \quad (1)$$

where I_0 is the drain current when $V_{gs} = V_{th}$, V_T is the thermal voltage, and V_{ds} represents the drain-to-source voltage. MOSFETs operating in subthreshold region have

FIGURE 3: Structure of the OPs used in the proposed ROIC.

larger gm-to-channel current ratio than those in saturation region, which implies that subthreshold technology can be applied to optimization power dissipation of analog ICs with the guarantee for sufficient gain.

It is worth noting that the behavioural model of MOSFETs in subthreshold region is not accurate enough when the process of ICs goes into deep submicron, like $0.18 \mu\text{m}$. To do the calculation precisely, all the parameters adopted should be those obtained through simulations. Figure 4 shows the qualitative illustration of the real gm-to-channel current ratio compared with the theoretical one, (a) for NMOS and (b) for PMOS, from which it can be seen that although the ratio does not increase as fast as the theoretical curve expects when the $V_{gs} - V_{th}$ goes down, it is much larger in the subthreshold region than that in the saturation region. That is what we desire to improve efficiency of utilizing current.

Figure 5 shows the timing diagram of the readout unit cell. The switches turn on and off when the controlling signals are high and low, respectively. At " t_1 " S_r and S_4 turn on, the integrator resets, and the voltage of " V_{in} " node is set to the reference voltage V_{ref} , which is sampled at the positive input

FIGURE 4: gm-to-channel current ratio.

FIGURE 5: Timing diagram of the proposed readout unit cell.

port of A_4 by C_2 immediately. After the integration ends, the voltage of “ V_{in} ” node is given by

$$V_{in} = V_{ref} - \frac{I_L T_{int}}{C_{int}}, \quad (2)$$

where I_L is the photocurrent and C_{int} and T_{int} are integration capacitor and integration time, respectively. At “ t_2 ” S_1 and S_2 turn on and the voltages of the two nodes “ V_1 ” and “ V_2 ” across C_1 become the V_{in} and V_{ref} , respectively. At “ t_3 ” S_3 turns on and “ V_1 ” node connects to ground. Based on the law of conservation of charge, the voltage of “ V_2 ” node turns into

$$V_2 = V_{ref} - V_{in} = \frac{I_L T_{int}}{C_{int}}. \quad (3)$$

The output node “ V_{cfs} ” should be equal to “ V_2 ” under ideal condition, thus giving the net integration voltage and subtracting the charge injection error brought by the reset process of integrator. However the transmission of signal will

be influenced by noise, which is analyzed in the next section in detail.

The transient response of the readout unit cell is depicted in Figure 6. We can see that the reset voltage equal to the reference voltage is 2.5 V and the “ V_{in} ” node becomes 1.5 V from 2.5 V through integration. At “ t_3 ” S_3 turns on, the “ V_1 ” node connects to ground, and “ V_2 ” sets to 1 V, which drives the output voltage to 1 V, the net integration voltage. Besides, the static power dissipation of the proposed readout unit cell reaches 2.8 μ W with 700 nW per OP.

4. Noise Model Based on Transfer Function

4.1. The Integrator Part. The noise model of the integrator part is shown in Figure 7. There are three noise sources: photocurrent noise caused by photoelectric effect which cannot be avoided [14], the noise caused by the reset process of switch S_r , and the noise of the OP presenting as the input reference noise source.

FIGURE 6: Signal transfer process.

FIGURE 7: Noise model of integrator part.

For CTIA ROIC, photocurrent and its noise integrate on C_{int} directly, which can be expressed as

$$V_{out}(n(T + T_{int})) = \frac{1}{C_{int}} \int_{nT}^{n(T+T_{int})} i(t) dt, \quad (4)$$

where T represents the time length of a frame and (3) can be comprehended as $i(t)$ convolving a window function with T_{int} window length [15]. So in frequency domain the process can be expressed as

$$\begin{aligned} V_{out}(f) &= \frac{1}{C_{int}} i(f) H_{square}(f) \\ &= \frac{1}{C_{int}} i(f) (T_{int} \text{sinc}(\pi f T_{int})) = i(f) H_i(f), \end{aligned} \quad (5)$$

FIGURE 8: Noise model of OP.

where $H_i(f)$ is the transfer function of photocurrent noise source to the “ V_{in} ” node and the contribution to the output noise of the integrator part is given in the form of power spectrum density (PSD) by

$$e_{no1,inp}^2 = H_i^2(f) i_{np}^2, \quad (6)$$

where $e_{no1,inp}^2$ represents the PSD of noise voltage on “ V_{in} ” node induced by i_{np}^2 , that is, the PSD of photocurrent noise from the corresponding pixel. The transfer function of the OP noise source e_nA , denoted by $H_A(f)$, can be derived by the model depicted in Figure 8:

$$H_A(f) = \frac{C_{int} + C_{det}}{C_{int} + (C_{int} + C_{det})/A(f)}, \quad (7)$$

where C_{det} is the shunt capacitor of the pixel and $A(f)$ is the open loop transfer function of the OP, which can be expressed as [11]

$$A(f) = \frac{A_0}{1 + jfA_0/GBW}, \quad (8)$$

where A_0 and GBW are the low frequency gain and gain bandwidth product of the OP.

We can get the transfer function of e_nSr by the same approach, which is given by

$$H_R(f) = \frac{1}{1 + jfR_{off}C_{int}}, \quad (9)$$

where R_{off} is the off-resistance of the switch S_r . The output noise of integrator part can be expressed in matrix, which is given by

$$\begin{aligned} O_1 &= \begin{bmatrix} e_{no1,inp}^2 \\ e_{no1,A}^2 \\ e_{no1,S_r}^2 \end{bmatrix} \\ &= \begin{bmatrix} H_i^2(f), & 0, & 0 \\ 0, & H_A^2(f), & 0 \\ 0, & 0, & H_R^2(f) \end{bmatrix} \begin{bmatrix} i_{np}^2 \\ e_{nA}^2 \\ e_{nS_r}^2 \end{bmatrix}. \end{aligned} \quad (10)$$

4.2. CDS Part. The noise model of the CDS is shown in Figure 9, where all the OPs are connected as unity-gain buffers. Because of the noninverting structure, their output resistance is reduced by A_0 times which can be ignored based on the Thevenin equivalent.

When the integrator resets, the voltage on “ V_{in} ” node is sampled on C_2 ; after the integration, the voltage on “ V_{in} ” node is transferred to the “ V_1 ” node at the moment S_1 and S_2 turn on. The voltage across C_1 is

$$V_{C_1}(nT) = V_2(nT) - V_1(nT). \quad (11)$$

For Δ time after S_1 and S_2 turn off and S_3 turns on, the voltage on “ V_2 ” is

$$V_2(n(T + \Delta)) = V_{C_1}(n(T + \Delta)) - V_1(n(T + \Delta)). \quad (12)$$

The expression in frequency domain is given by

$$v_{n2}^2 = \int e_{n2}^2 df = \int (e_{nC_1}^2 + e_{n1,\Delta}^2) df, \quad (13)$$

where $e_{nC_1}^2$, $e_{nC_1}^2$, and $e_{n1,\Delta}^2$ stand for the PSD of noise voltage on “ V_2 ,” across C_1 at “ nT ” and on “ V_1 ” at “ $n(T + \Delta)$.” So the latter two can be expressed as follows:

$$e_{nC_1} = [H_{int}(f), H_{S_r}(f), H_{A_2}(f), H_{S_1}(f), H_{A_4}(f),$$

$$H_{S_2}(f)] \begin{bmatrix} e_{mint} \\ e_{on1,S_r} H_D(f) \\ e_{nA_2} \\ e_{nS_1} \\ e_{nA_4} \\ e_{nS_2} \end{bmatrix} \quad (14)$$

$$e_{n1,\Delta}^2 = e_{nS_3}^2, \quad (15)$$

where $H_X(f)$ is the transfer function of the noise source X to the nodes across C_1 , respectively. e_{mint} is the noise of “ V_{in} ” node at the moment an integration ends which is equal to $e_{on1,A} + e_{on1,inp} + e_{on1,S_r}$. $H_D(f) = \exp(-j\omega T_{int})$ represents the reset process that is before the integration starts [15]. Consider

$$e_{nC_1}^2 = [H_{int}^2(f), H_{int}^2(f),$$

$$|H_{int}(f) + H_{S_r}(f) H_D(f)|^2, H_{A_2}^2(f), H_{S_1}^2(f),$$

$$H_{A_4}^2(f), H_{S_2}^2(f)] \begin{bmatrix} e_{on1,inp}^2 \\ e_{on1,A}^2 \\ e_{on1,S_r}^2 \\ e_{nA_2}^2 \\ e_{nS_1}^2 \\ e_{nA_4}^2 \\ e_{nS_2}^2 \end{bmatrix}. \quad (16)$$

$n(T + \Delta)$ marks the end of one period of correlated double sampling; at that time the noise on “ V_2 ” and the noise of A_3 are transferred through A_3 with a transfer function denoted by $A_{UG}(f)$ to the “ V_{cds} ” node:

$$v_{on}^2 = \int e_{on}^2 df = \int (e_{n2}^2 + e_{nA_3}^2) |A_{UG}(f)|^2 df, \quad (17)$$

$$A_{UG}(f) = \frac{1}{1 + jf/GBW}. \quad (18)$$

The PSD of the noise of the output node “ V_{cds} ” of CDS can be written as the following equation:

$$O_2 = \begin{bmatrix} e_{on2,inp}^2 \\ e_{on2,A}^2 \\ e_{on2,S_r}^2 \\ e_{on2,A_2}^2 \\ e_{on2,S_1}^2 \\ e_{on2,A_4}^2 \\ e_{on2,S_2}^2 \\ e_{on2,S_3}^2 \\ e_{on2,A_3}^2 \end{bmatrix} = H_2 E_{cds} = H_2 \begin{bmatrix} e_{on1,inp}^2 \\ e_{on1,A}^2 \\ e_{on1,S_r}^2 \\ e_{nA_2}^2 \\ e_{nS_1}^2 \\ e_{nA_4}^2 \\ e_{nS_2}^2 \\ e_{nS_3}^2 \\ e_{nA_3}^2 \end{bmatrix}, \quad (19)$$

where H_2 is a diagonal matrix whose diagonal line corresponds to the transfer functions of each noise element in E_{cds} . It can be seen that the first three elements in E_{cds} are noise sources from the integrator. To show the noise sources in CDS, we define

$$E_2 = [0, 0, 0, e_{nA_2}^2, e_{nS_1}^2, e_{nA_4}^2, e_{nS_2}^2, e_{nS_3}^2, e_{nA_3}^2]^T. \quad (20)$$

So the following expression can be acquired:

$$E_{cds} = E_2 + T_1 \{O_1\}, \quad (21)$$

where T converts O_1 to an enhanced length with 0, which means O_1 changes from $[e_{on1,inp}^2, e_{on1,A}^2, e_{on1,S_r}^2]^T$ to $[e_{on1,inp}^2, e_{on1,A}^2, e_{on1,S_r}^2, 0, 0, 0, 0, 0, 0]^T$. Written briefly, the transmission of noise through the two parts of the readout unit cell is

$$O_1 = H_1 E_1,$$

$$O_2 = H_2 (E_2 + T_1 \{O_1\}). \quad (22)$$

Every noise source in each part of the readout unit cell transmitting to the output node is expressed precisely and compactly by using (22). The design contains only two parts, so the numbers marking the parts are 1 and 2. Under the situation of much more constituent parts, the transmission of noise source can be written as

$$O_{n+1} = H_{n+1} (E_{n+1} + T_n \{O_n\}). \quad (23)$$

FIGURE 9: Noise model of CDS part.

5. Noise Computing

5.1. Noise Computing Based on Transfer Function. The photocurrent noise is related to the value of the generating photocurrent, which varies with the radiation intensity. Strictly speaking, it is pixel noise, which does not belong to the noise of readout circuits [15]. Thus the photocurrent noise will not be calculated in the paper. All the noise sources in the readout unit cell are induced by the MOSFETs. For the switches, MOSFETs operating in linear region produce thermal noise modeled by [12, 16]

$$e_{nS_i}^2 = 4kTR_{oni}, \quad (24)$$

where k is the Boltzman constant, T is the absolute temperature, and R_{oni} represents the on-resistance of the switches. MOSFETs in the OP operate in the subthreshold region, producing thermal noise and $1/f$ noise; the whole noise of an OP can be represented as the reference input noise:

$$e_{nA_i}^2 = K_{1e} + \frac{K_{2e}}{f}, \quad (25)$$

where K_{1e} and K_{2e} represent thermal noise factor and $1/f$ noise factor for the OPs, respectively. The detail of computing expression can be referred to in the chapter introducing OP of [12, 16], through which the specific values of the two parameter are obtained. The process on which the project is based is Globalfoundries 0.18 μm Industry Compatible Dual Voltage 1.8 V/3.3 V Process. The frequency character of the OP is simulated, which is shown in Figure 10. From it we can see that the OP achieve a 61-degree phase margin that leads to stability when countering an input of a step signal.

The switches in the proposed ROIC are implemented as CMOS switches, individual of which consists of a P type MOSFET, Mp, and an N type MOSFET, Mn, as shown in Figure 11. The W/L of both of the two MOSFETs are set to be $0.3 \mu\text{m}/2.35 \mu\text{m}$. The simulation curve of resistance of the CMOS switch is shown in Figure 12, where the input signal spans from 0.5 V to 2.5 V. Figures 12(a) and 12(b) present the value of maximum on-resistance 2.2 k Ω and the value of minimum off-resistance 1 G Ω .

FIGURE 10: Frequency character of OP used in the proposed ROIC.

The parameters used for the calculation of noise are summarized in Table 2, where we assume that all the OPs have the same parameters and so do the switches.

For the application of high resolution, the area of a single pixel is restricted, leading to the limited layout area for the readout unit cell. With respect to the fact that capacitors consume the largest area resource, therefore, with the guarantee of sufficient layout area for the MOSFETs, more layout areas should be distributed to the three capacitors in the unit cell. Through calculations, effect on the output noise due to C_2 can be neglected, which should be designed small to save up layout area to allow larger C_{int} and C_1 . With the limitation of $30 \mu\text{m} \times 30 \mu\text{m}$ layout area, the maximum of the sum of the two capacitors is 2 pF.

The contribution of each noise source to the output noise is calculated using the transfer functions in Section 3, which is shown in Figure 13, where T_{int} is set as 100 μs . Figure 13(a) depicts the dependence of the output noise, integrator noise, and CDS noise on the C_{int} . The diagram reveals an opposite variation trend. The integrator noise is an increasing function

FIGURE 11: CMOS switch used in the proposed ROIC.

and the CDS noise is a decreasing function, which results from the limitation of the sum of capacitors. C_{int} increase leads to C_1 decrease inevitably, causing enlargement of the bandwidth of transfer functions of noise sources in CDS, which weakens the ability of low pass filtering. Figure 13(b) gives the curves of thermal noise, $1/f$ noise, and reset noise with the change of C_{int} . We can see that $1/f$ noise and reset noise increase with C_{int} increase while an optimal point appears for the thermal noise which is the majority, at 0.66 pF. When the C_{int} is smaller than 0.26 pF, the reset noise is smaller than $1/f$ noise. The output noise reaches the minimum at 74.1 μ V when the C_{int} is 0.74 pF and C_1 is 1.26 pF.

Figure 14 shows the output noise as a function of T_{int} with three different C_{int} . It can be seen that the output noise increases when T_{int} increases, despite different C_{int} . This is mainly because the increasing of T_{int} results in increasing of interval of correlated double sampling, which weakens the capability of suppressing $1/f$ noise and reset noise. From the figure we also get that, with smaller C_{int} , the increase speed of output noise is faster.

5.2. Noise Calculation Based on Verilog-A. The transient analysis of the proposed readout unit cell is carried out in the section. HSPICE provides the possibility to simulate circuit noise in AC response by computing the PSD but cannot give the waveform of noise in transient response directly, whereas we carried out an approach to model time domain noise source using Verilog-A, which is described in detail in [13, 17] with both thermal and $1/f$ noise source modelling.

FIGURE 12: Simulation curve of resistance of the CMOS switch.

TABLE 2: Parameters of noise calculation.

R_{on} (on-resistance of switch)	2.2 kΩ
R_{off} (off-resistance of switch)	1 GΩ
K_{1e} (thermal noise parameter of OP)	4×10^{-17} V ² /Hz
K_{2e} ($1/f$ noise parameter of OP)	4×10^{-12} V ² /Hz
GBW (gain bandwidth product of OP)	1.58 MHz
A_0 (low frequency gain of OP)	75 dB

The averaged RMS of the output noise obtained by Verilog-A are presented in Tables 3 and 4 to compare with those that were calculated through transfer functions specified in Section 3, where the unit of noise is μ V. In Table 3, T_{int} is assumed to be 100 μ s and C_{int} is 0.74 pF in Table 4. With different C_{int} and T_{int} , the two sets of results are in good agreement, the difference between which is lower than 6%, therefore proving the feasibility of the method of transfer function noise analysis.

FIGURE 13: Noise voltage versus integration capacitor.

FIGURE 14: Noise voltage versus integration time.

TABLE 3: Comparison between transfer function based and Verilog-A based.

C_{int}	100 fF	460 fF	820 fF	1.18 pF	1.54 pF	1.9 fF
Theoretical results	224.7	79.5	74.4	81.5	101.9	129.2
Verilog-A results	212.1	81.9	77.0	79.8	108.2	123.8

6. Conclusion

To adapt the application of imaging for large format and high resolution, a new readout cell with low power and small layout area is proposed, consisting of an integrator and

TABLE 4: Comparison with different integration time.

T_{int}	200 ns	800 ns	3.2 μs	12.8 μs	51.2 μs	204.8 μs
Theoretical results	71.5	72.0	72.5	72.9	73.5	75.9
Verilog-A results	74.6	74.4	69.9	75.6	72.8	74.4

a new type of CDS, both of which are switched capacitor circuits where all the MOSFETs are optimized in subthreshold region. The integrator adopts CTIA structure and the CDS is comprised of four switches, three Ops, and two capacitors. The noise model is built using transfer function in Section 3 and a method of presenting the transfer process of noise in the form of matrix is given, through which we can describe the contribution of each noise source to the whole output noise distinctly. In Section 4, noise analysis of the proposed readout cell is carried out by the transfer function method and transient analysis utilizing Verilog-A, respectively. The results showing good agreement verify the feasibility of the method presented through matrix. Under the limitation of layout area less than $30 \mu m \times 30 \mu m$, the integrator noise is an increasing function of C_{int} and the CDS noise is a decreasing function. With respect to the types of noise, $1/f$ noise and reset noise increase with C_{int} increase while an optimal point appears for the thermal noise which is the majority. The integration capacitor should be selected as 0.74 pF to achieve an optimal noise performance, the whole output noise reaching the minimum value at $74.1 \mu V$.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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