Research Article

A New CDS Structure for High Density FPA with Low Power

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Being an essential part of infrared readout integrated circuit, correlated double sampling (CDS) circuits play important roles in both depressing reset noise and conditioning integration signals. To adapt applications for focal planes of large format and high density, a new structure of CDS circuit occupying small layout area is proposed, whose power dissipation has been optimized by using MOSFETs in operation of subthreshold region, which leads to 720 nW. Then the noise calculation model is established, based on which the noise analysis has been carried out by the approaches of transfer function and numerical simulations using SIMULINK and Verilog-A. The results are in good agreement, demonstrating the validity of the present noise calculation model. Thermal noise plays a dominant role in the long wave situation while $1/f$ noise is the majority in the medium wave situation. The total noise of long wave is smaller than medium wave, both of which increase with the integration capacitor and integration time increasing.

1. Introduction

Infrared detectors have a wide range of applications in areas of military, research, and manufacture, whose core part is an infrared focal plane assembly. The assembly mainly consists of two parts: focal plane arrays (FPAs) that function to convert radiation to current signal and readout integrated circuits (ROIC) that are responsible for realization of serial read and processing of signals sampled by the FPA.

Being an essential part of infrared readout integrated circuit, correlated double sampling (CDS) circuits play important roles in both depressing reset noise and conditioning integration signals [1–3]. Applications of focal planes of large format and high density put forward more harsh demand on low power dissipation and small layout area of a ROIC unit cell. Based on the theory that MOSFETs operating in the subthreshold region consume much less dissipation than those in the depletion region, this paper proposed a low power CDS structure that contains only one sampling capacitor, two switches, and two operation amplifiers (OPs), which saves the layout area [4, 5]. Then the noise calculation model is established, based on which noise analysis has been carried out by the approaches of transfer function and numerical

simulation using SIMULINK and Verilog-A, whose results are in good agreement.

2. Circuit Design

2.1. Operating Principle. The proposed CDS circuit is shown in Figure 1. It comprises two OPs A_1 and A_2 that are connected as buffers, a sampling capacitor C_{sh} and two complementary switches S_1 and S_2 . A_1 and A_2 are standard two stage OPs, which are shown in Figure 2. They can provide high gain in order to reduce the error caused by the transmission process of the signals, in the meanwhile guarantee low noise.

The clock timing waveforms of the CDS circuit are also illustrated in Figure 1. After the integrator resets, S_1 and S_2 are both switched on at t_0 and the reset voltage of the integrator is coupled on the “ V_1 ” node, which is the first sample; then the two switches are off at t_1 , so the charge of C_{sh} remains unchanged until t_2 ; after the integration duration, S_1 is turned on while S_2 remains off at t_2 , and the second sampled signal is stored on “ V_1 ” node. Because of the law of conservation of charge, the voltage of “ V_2 ” node jumps by the difference value between the two sampling processes, which cuts off the error that resulted by the reset process

FIGURE 1: Operating principle: (a) structure and (b) operating timing.

FIGURE 2: Structure of the OPs used in the proposed CDS circuit.

of the integrator and suppresses low frequency noise. The proposed circuit structure is easy to implement, where using OP provides the conditions that no extra bias voltage is needed. As is known, capacitors occupy the most layout area; thus the design of only one capacitor saves much area. Besides subthreshold technology applied makes the proposed CDS circuit suitable for ROIC unit cells of the large format FPAs.

2.2. Power Optimization. Subthreshold technology is operating transistors in subthreshold region by providing gate-to-source voltage lower than threshold voltage ($V_{gs} < V_{th}$).

TABLE 1: Performance comparison.

Working region	Gain (dB)	GBW (Hz)	SR (V/us)	Power (W)
Saturation	78	50.5 M	10.2	622 u
Saturation	72.5	1.7 M	0.62	5.5 u
Subthreshold	75.6	1.58 M	0.57	720 n

Ideally, when V_{gs} is lower than V_{th} , the channel between source and drain is shut down. Nevertheless, some electrons still flow across the two ports, known as subthreshold current. Research demonstrates that the subthreshold current is increasing exponentially with the V_{gs} increasing, like the current in BJT. The relationship can be expressed as

$$I_{sub} = I_0 e^{(V_{gs} - V_{th})/nV_T} (1 - e^{-V_{ds}/V_T}), \quad (1)$$

where I_0 is the drain current when $V_{gs} = V_{th}$, V_T is the thermal voltage, and V_{ds} represents the drain-to-source voltage [6]. It is worth noting that the behavioural model of MOSFETs in subthreshold region is not accurate enough when the process of ICs goes into deep submicron, like 0.18 um. To do the calculation precisely, all the parameters adopted should be those obtained through simulations.

MOSFETs operating in subthreshold region have larger gm-to-channel current ratio than those in saturation region, which implies that subthreshold technology can be applied to optimization power dissipation of analog ICs with the guarantee for sufficient gain [7]. Table 1 is the comparison of the performance for the OPs consisting of MOSFETs working in different regions, where the supply voltages are 0 Volts to 3 Volts. It can be seen that the dissipation of the OP with the design of subthreshold technology succeeds in reducing at least one order of magnitude at the price of tradeoff with frequency character like small SR and GBW.

Figure 3 shows the transient response of the proposed CDS circuit with the two OPs A_1 and A_2 designed by the subthreshold technology, in which the reset voltage is 1 Volt, the output of the integrator is 3 Volts, and S_1 is switched on at " t_2 ". After slight oscillation the output of the CDS circuit reaches 2 Volts, which is the integration voltage.

FIGURE 3: The transient response of the CDS circuit.

FIGURE 4: Calculation model of noise.

3. Noise Analysis

3.1. Noise Calculation Model. The calculation model of noise for the proposed CDS circuit is illustrated in Figure 4, involving four noise sources, which are from the two OPs and the two switches, respectively. The noise sources of the switches are thermal noise and the noise of the OPs is composed of thermal noise and $1/f$ noise.

Referred to the noise, voltage difference appears on C_s at “ t_1 .” Based on the law of charge conservation, the voltage across C_s maintains the same, so the noise voltage of the “ V_2 ” node can be derived from

$$v_2(nT_S + T) = v_1(nT_S + T) - (v_1(nT_S) - v_2(nT_S)). \quad (2)$$

For the form of integration of frequency spectrum,

$$v_{n2}^2 = \int_0^\infty e_{n2}^2(f) df = \int_0^\infty e_{n,v_1}^2(f) H_{\text{CDS}}^2(f) + e_{n,v_2}^2(f) df. \quad (3)$$

The transfer function of $H_{\text{CDS}}(f)$ is given by

$$H_{\text{CDS}}(f) = 1 - \exp(-2\pi j f T), \quad (4)$$

where $e_{n,v_1}^2(f)$ and $e_{n,v_2}^2(f)$ are noise power spectrum density (PSD) of “ V_1 ” and “ V_2 ” nodes at “ nT_S ,” respectively [8, 9], which can be found by (5), due to the independence of each noise source. Here $H_{A_1,i}(f)$, $H_{1,i}(f)$, and $H_{2,i}(f)$ are transfer functions to the “ V_i ” node where i can be 1 or 2 for

TABLE 2: Parameters of noise calculation.

$R_{\text{on}1}, R_{\text{on}2}$	2.2 k Ω
K_{1ei}, K_{1e2}	4.0×10^{-17} V ² /Hz
K_{2ei}, K_{2e2}	4.2×10^{-11} V ² /Hz
GBW ₁ , GBW ₂	1.58 MHz
R_o	560 k Ω

the following three noise sources: $e_{nA_1}^2(f)$, $e_{nS_1}^2(f)$, and $e_{nS_2}^2(f)$, respectively, which are the reference noise of A_1 , the resistance-on noise of S_1 , and the resistance-on noise of S_2 , respectively. They are described in detail in the appendix:

$$\begin{bmatrix} e_{n,v_1}^2(f) \\ e_{n,v_2}^2(f) \end{bmatrix} = \begin{bmatrix} H_{A_1,1}^2(f), H_{1,1}^2(f), H_{2,1}^2(f) \\ H_{A_1,2}^2(f), H_{1,2}^2(f), H_{2,2}^2(f) \end{bmatrix} \begin{bmatrix} e_{nA_1}^2(f) \\ e_{nS_1}^2(f) \\ e_{nS_2}^2(f) \end{bmatrix}. \quad (5)$$

The noise of the end “ V_2 ” goes through A_2 with finite GBW, added by the noise source of A_2 . The output noise of the CDS circuit is given by

$$v_{no}^2 = \int_0^\infty (e_{n2}^2(f) + e_{nA_2}^2(f)) H_{\text{UG}}^2(f) df, \quad (6)$$

where $H_{\text{UG}}(f)$ is the transfer function of the buffers constituted by A_1 or A_2 , and GBW represents gain-bandwidth product as seen in a number of textbooks for CMOS design:

$$H_{\text{UG}}(f) = \frac{1}{1 + f/\text{GBW}}. \quad (7)$$

3.2. Noise Calculation. The noise of the OP and the switch is introduced by MOSFETs. With regard to S_1 and S_2 , MOSFETs in linear region produce thermal noise similar to resistance [6], which is given by

$$e_{nS_i}^2 = 4kTR_{\text{on}i}, \quad (8)$$

where k is the Boltzmann constant, T is the absolute temperature, and the MOSFETs of the OP are in the subthreshold region that generates not only thermal noise but also $1/f$ noise. The whole noise of the OP can be modeled as the reference input noise at the input port of the OP, which can be described by

$$e_{nA_i}^2 = K_{1ei} + \frac{K_{2ei}}{f}, \quad (9)$$

where $R_{\text{on}i}$ represents the on-resistance of the switches and K_{1ei} and K_{2ei} represent thermal noise factor and $1/f$ noise factor for the OPs, respectively [7]. Here i is equal to 1 or 2. The calculation of noise adopts the parameters in Table 2, where R_o is the output resistance of OP.

Detectors capable of different wavebands produce a variety of densities of photocurrent, which leads to different integration time needed at certain ability of charge processing.

FIGURE 5: Noise versus C_{int} : (a) long wave and (b) medium wave.

We define $K_{int} = T_{int}/C_{int}$ as the integration factor, determined by the value of photocurrent and output swing of the ROIC. T_{int} means integration time, that is, the time interval between the two sampling processes of CDS, and C_{int} is integration capacitor. Figure 5 gives the output noise and its component noise of the proposed CDS circuit as functions of C_{int} under the situations of applications of long wave and medium wave, respectively. K_{int} is 50 K for typical long wave and 1 MEG for medium wave. As can be seen, noise increases with C_{int} increasing for long wave detection, in which 1/f noise has greater growth than thermal noise; when $C_{int} < 2$ pF, thermal noise dominates. For medium wave situation, owing to the radiation weaker than that for long wave, larger T_{int} is needed at the same C_{int} . The fact mentioned above results in longer interval between the two sampling processes of CDS, thus causing inferiority of suppressing 1/f noise. We can see that under medium wave situation 1/f noise is larger than thermal noise and rises with C_{int} increasing. By comparison of the two situations, we conclude that the noise that CDS circuit brings into the signal chain is larger for medium wave application than that for long wave.

Figure 6 shows the noise varying as functions of T_{int} at fixed C_{int} , in which we can see 1/f noise is increasing with T_{int} increasing; while thermal noise nearly remains the same, the reason can be concluded through analysis that the increasing of T_{int} results in the increasing of $H_{CDS}^2(f)$ in its low frequency area; thus more noise of low frequency is transmitted to the output node of the CDS circuit.

4. Simulation Experiment

The transient analysis model of the proposed CDS circuit is constructed in SIMULINK, which is shown in Figure 7.

FIGURE 6: Noise versus T_{int} .

Thermal noise can be presented directly using the module in the simulator and 1/f noise is modeled by the approach brought out in [10]. HSPICE provides the possibility to simulate circuit noise in AC response by computing the PSD but cannot give the waveform of noise in transient response directly, whereas we carried out an approach to model time domain noise source using Verilog-A in this paper [11], as is shown in Figure 8(a). The noise is filtered by an RC filter, which settles its bandwidth. The waveform can be seen in Figure 8(b).

FIGURE 7: Noise model in SIMULINK.

At last we averaged the RMS of the output noise from the scope in Figure 7 and output noise obtained by Verilog-A method to compare with those that were calculated by the equations in Section 2, and the unit of noise is μV . The three sets of results, which are given in Table 3, are in good agreement, therefore proving the feasibility of the method of transfer function noise analysis.

5. Conclusion

For the applications of FPAs of large format and high density, a new structure of CDS circuit is proposed, whose power dissipation has been optimized by subthreshold technology, which leads to 720 nW. Because of using only one sampling capacitor, the proposed CDS circuit occupies small layout area. Then the noise calculation model is established, based on which the noise analysis has been carried out by the approaches of transfer function and numerical simulation using SIMULINK and Verilog-A. The results are in good

agreement, demonstrating the validity of the present noise calculation model. Thermal noise plays a dominant role in the long wave situation while $1/f$ noise is the majority in the medium wave situation. The total noise of long wave is smaller than medium wave, both of which increase with the integration capacitor and integration time increasing.

Appendix

Explanation of (5)

The model of noise source of A_1 transmitting to the nodes across C_s is shown in Figure 9, whose transfer functions that appear in (5) are given by (A.1) and (A.2), respectively:

$$H_{A_1,1}(f) = \frac{1}{1 + f/\text{GBW}} \cdot \frac{1 + sC_{\text{SH}}R_{\text{on}2}}{1 + sC_{\text{SH}}(R_o + R_{\text{on}1} + R_{\text{on}2})}, \quad (\text{A.1})$$

```
//NOISE SOUREC Verilog-A
module Noise_Soure (out);
output out;
electrical out;
Parameter period = 1.0;
Parameter Fall_time = 100;
Parameter vmod = 1;
integer x;
analog begin
  @(timer (0, period))
  x = $random;
  V(out) <+ transition(x, 0, period/Fall_time)/vmod;
end
endmodule
```

(a)

(b)

FIGURE 8: Noise source modelling in Verilog-A: (a) noise source and (b) waveform.

TABLE 3: Comparison of the two methods of noise analysis.

T_{int}	100 ns	1 us	10 us	100 us	150 us	200 us
Theoretical results	28.03	29.39	29.41	31.20	34.02	46.62
SIMULINK results	27.44	28.57	28.82	30.71	34.05	47.52
Verilog-A results	27.19	29.11	28.23	30.26	32.80	49.57

$$H_{A_{1,2}}(f) = \frac{1}{1 + f/GBW} \cdot \frac{sC_{SH}R_{on2}}{1 + sC_{SH}(R_o + R_{on1} + R_{on2})}. \quad (A.2)$$

The model of noise source of S_1 transmitting to the nodes across C_s is shown in Figure 10, whose transfer functions that appear in (5) are given by (A.3) and (A.4), respectively:

$$H_{1,1}(f) = \frac{1 + sC_{SH}R_{on2}}{1 + sC_{SH}(R_o + R_{on1} + R_{on2})}, \quad (A.3)$$

$$H_{1,2}(f) = \frac{sC_{SH}R_{on2}}{1 + sC_{SH}(R_o + R_{on1} + R_{on2})}. \quad (A.4)$$

The model of noise source of S_1 transmitting to the nodes across C_s is shown in Figure 11, whose transfer functions that appear in (5) are given by (A.5) and (A.6), respectively:

$$H_{2,1}(f) = \frac{sC_{SH}(R_o + R_{on1})}{1 + sC_{SH}(R_o + R_{on1} + R_{on2})}, \quad (A.5)$$

$$H_{2,2}(f) = \frac{1 + sC_{SH}(R_o + R_{on1})}{1 + sC_{SH}(R_o + R_{on1} + R_{on2})}. \quad (A.6)$$

FIGURE 9: Transfer function of noise source of A_1 . FIGURE 10: Transfer function of noise source of S_1 .

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

FIGURE 11: Transfer function of noise source of S_2 .

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