VLSI Design

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Special Issue on

VLSI Processor Architectures for Machine Learning in Computer Vision

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Machine learning has accomplished a long list of successful solutions; however, most of them have not been implemented in dedicated hardware devices incurring in extra power consumption and latency/throughput bottlenecks. Today, one of the main goals in this area is to design and implement efficient coprocessors that allow real time implementations of any of the existing machine learning algorithms and support the increasing amount of data that nowadays needs to be processed. But there are some critical constraints that require the attention of the community: 1) The fact that the algorithms are highly complex and require several expensive graphic processor units and consume significant energy. This makes it difficult to realize the real-time implementations in a cost-effective way. 2) The increase of information exchanged between the processor and the memories which causes routing congestion increasing the critical path of the resulting architectures and thus lowering the operating frequency and throughput of these solutions. 3) The need of generalized architectures that can be reconfigured for different scenarios balancing generality and efficiency.

So the primary challenges in this field are the design of processors with lower computational complexity, less exchange of data applying for example compression techniques, and the requirement of architectures that allow a high level of generalization.

Potential topics include but are not limited to the following:

- Architectures and configurable platforms including both analog and digital solutions for modern scenarios that use machine learning, such as Vision and LiDAR processing
- Design or optimization of algorithms oriented to hardware-friendly implementations of statistical learning algorithms, graphical models, Gaussian processes, Bayesian methods, neural networks especially convolutional neural networks, deep learning, structured learning, and so on
- Procedures to optimize FPGA and/or ASIC designs of reconfigurable learning theory implementations
- Energy efficiency analysis of different architectures and algorithms to allow low-power/portable solutions which can be integrated in real systems
- Design or optimization of Computer Vision algorithms in general and SLAM (Simultaneous Localization and Mapping) algorithms along with Detection and Tracking of Moving Objects for cars with advanced driving assistance systems and self-driving cars, using dedicated hardware and/or hardware-friendly implementations.

Authors can submit their manuscripts through the Manuscript Tracking System at http://mts.hindawi.com/submit/journals/vlsi/vlsip/.

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