

Research Article

Wireless Interconnect in Multilayer Chip-Area-Networks for Future Multimaterial High-Speed Systems Design

Oluwole John Famoriji, Xu Yan, Mehdi Khan, Rao Kashif, Akinwale Fadamiro, Md Sadek Ali, and Fujiang Lin

Micro-/Nano-Electronic System Integration R&D Centre (MESIC), University of Science and Technology of China (USTC), Hefei, Anhui 230026, China

Correspondence should be addressed to Oluwole John Famoriji; famoriji@mail.ustc.edu.cn

Received 9 August 2017; Revised 2 October 2017; Accepted 16 October 2017; Published 5 December 2017

Academic Editor: Eva Antonino Daviu

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Wireless chip area network which enables wireless communication among chips fosters development in wireless communication and it is envisioned that future hardware system and developmental functionality will require multimaterial. However, the traditional system architecture is limited by channel bandwidth-limited interfaces, throughput, delay, and power consumption and as a result limits the efficiency and system performance. Wireless interconnect has been proposed to overcome scalability and performance limitations of multihop wired architectures. Characterization and modeling of channel become more important for specification of choice of modulation or demodulation techniques, channel bandwidths, and other mitigation techniques for channel distortion and interference such as equalization. This paper presents an analytical channel model for characterization, modeling, and analysis of wireless chip-to-chip or interchip interconnects in wireless chip area network with a particular focus on large-scale analysis. The proposed model accounts for both static and dynamic channel losses/attenuation in high-speed systems. Simulation and evaluation of the model with experimental data conducted in a computer desktop casing depict that proposed model matched measurement data very closely. The transmission of EM waves via a medium introduces molecular absorption due to various molecules within the material substance. This model is a representative of channel loss profile in wireless chip-area-network communication and good for future electronic circuits and high-speed systems design.

1. Introduction

Interchip wireless communication has attracted research attention in recent time as present-day exclusively wired communication and circuit dimensions get smaller. Specifically, the rapid emergence of integrated circuits (ICs) and systems on flexible and organic substrates for wearable and implantable electronics, Internet of Things (IoT) or Internet of Everything (IoE), data center, multicore computers, multilayer sensor networks, and so on require effective coupling for adequate and optimum performance of the systems [1, 2]. Since there is high system multifunctionality demand, it is envisioned that multimaterial high-speed system will surface in the nearest future. Wireless IC design has power reduction, latency reduction, and aggregate higher data rates than processing cores which intercommunicates with the ultimate goal to alternate wired interconnect. Furthermore,

logically deployed high-speed ultrashort range wireless links integrated platforms will provide improvements in efficiency, weighty reduction in size and complexity; fault tolerance; reconfigurability; and overall performance [3]. A major characteristic quality of the twenty-first century integrated electronics has been the emergence of wireless interconnect and explosive development of multifunctional and handy devices with sub-10 GHz communications as future requires higher bandwidths and data rates with ultra-low power systems connected in very short length scales [2]. Another integrity of wireless interconnect systems includes low complexity compared to wired connections; high energy efficiency for long, one-hop communication; and compatibility with CMOS wireless technology designs. Interconnects in multicore high performance computing architectures are the major drivers of such inconsistent requirements for design with mobile data cloud and intraroom multimedia [2, 4–9]; channel path loss

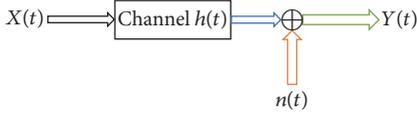


FIGURE 1: The system design.

quantification/model becomes necessary for specification of choice of channel bandwidths and any mitigation technique for channel distortion and interference such as equalization (e.g., filter) for adequate systems design.

Attempts have been made by different researchers such as [1, 10–16] to model the propagation pattern in on-chips but less attention on interchip communication [13, 17] and the general free space path loss model [18] remains unattended. Since interchip communication is key in system designs, then it becomes necessary to have an estimated path loss for adequate systems design. Recently, [2] designed an ultralow power wireless interconnects for network-on-chip and chip-to-chip communications by optimization of inductor-less two-stage cascode cascade LNA towards 90 GHz operation. It gains switching advantage against CMOS counterpart without additional switching transistors which consequently makes it highly power efficient and faster. Chen and Zhang [17] modeled path loss for interchip wireless communication channel from measurements. However, environment of propagation was assumed uniform (i.e., single material) which may not be valid for future multimaterial system hardware and development applications; for example, applying the model for circuits on PCB (printed circuit board) made of silicon and polyimide materials may be challenging, and frequency dependency is another key factor that should be considered because loss intensity changes with frequencies.

Adequate path loss characterization and modeling of interconnect in high-speed systems remain an open challenge and as a result requires more research attentions. Robust channel models are still required for the proper and appropriate characterization of interchip channels. In this paper, an analytical channel model which was validated by practical experimental data obtained from a computer desktop casing is proposed. The proposed model is frequency dependent and environmental material property dependent (dielectric property) which make it more robust and better for interchip large-scale path loss prediction. Introduction is presented in Section 1. Section 2 shows the proposed model while measurements and analysis are presented in Section 3. Section 4 presents model simulation and evaluation and Section 5 concludes the paper.

2. Proposed Analytical Model

A wireless channel can be characterized as an open-loop system with both static and dynamic changes of the channel parameterized. Figure 1 is a representation of a typical open-loop system; $x(t)$ is the input signal, $h(t)$ is the channel response, $n(t)$ is the noise, and $y(t)$ is the output signal which is given as [19]

$$y(t) = h(t) x(t) + n(t). \quad (1)$$

Signal propagating wirelessly is inversely proportional to a certain degree (say m) of its distance d . The ratio of output signal $y(t)$ to input signal $x(t)$ varies directly to wavelength λ while its constant of proportionality K defines the links parameters (electrical properties of the channel) such as effective permeability μ_e , and it is the effective dielectric constant, effective permittivity ϵ_e which implies the dielectric constant of a homogeneous medium that replaces air, depending on the nature of the material, signal source core/chip gain G_t , and receiving core/chip gain G_m . The combined noise effect of all the above parameters can act as noise source $n(t)$ that is mentioned in (1). Therefore, the constant of proportionality K can be expressed as

$$K(n) = \epsilon_e \mu_e G_t G_m; \quad (2)$$

for a uniform material propagation path (e.g., silicon), effective permittivity and permeability will be a constant value each. However for multilayer dielectric structures which are found in the present semiconductor industry, effective modeling of these structures enhances fast and accurate analysis and reduced computational cost. Teng [20] presents an extended Maxwell-garnet model ((3) and (4) are general expression for permittivity and permeability, resp.) which can be used to model effective permittivity and permeability. The extraction procedure for effective constitutive parameters is well detailed in [20]

$$\epsilon_e = \epsilon_{r,m} \frac{\epsilon_{r,i}(1+2p)F(\theta) - 2(p-1)\epsilon_{r,m}}{\epsilon_{r,i}(p-1)F(\theta) + \epsilon_{r,m}(2+p)}, \quad (3)$$

$$\mu_e = \mu_{r,m} \frac{\mu_{r,i}(1+2p)F(\theta) - 2(p-1)\mu_{r,m}}{\mu_{r,i}(p-1)F(\theta) + \mu_{r,m}(2+p)}, \quad (4)$$

where subscripts i and m represent the permeability and permittivity of matrix material and inclusion material, respectively, while p is the volume fraction of the inclusion and $F(\theta)$ is the frequency dependent term defined as

$$F(\theta) = \frac{2(\sin\theta - \theta \cos\theta)}{(\theta^2 - 1)\sin\theta + \theta \cos\theta}, \quad (5)$$

$$\theta = k_0 a \sqrt{\epsilon_{r,i} \mu_{r,i}},$$

where a is the radius of the sphere inclusion.

As signal propagates through the channel wirelessly on PCB, it varies with frequency variation, and hence a factor δf^n is introduced. f is frequency, and n accounts for other losses due to interference, dispersion, and so on of the channel. Therefore (3) by substitution can be expressed as

$$\frac{y}{x} = h = \frac{\epsilon_e \mu_e G_t G_r c}{4\pi (d/d_0)^m \delta (f/f_0)^n d_0^m f_0^n}. \quad (6)$$

Practically, there is no ideal environment, and then $n > 0$. At any point of signal observation, signal received is given as

$$y(t) = \frac{\epsilon_e \mu_e G_t G_r c}{4\pi (d/d_0)^m \delta (f/f_0)^n d_0^m f_0^n} x(t), \quad (7)$$

$$P_r = \frac{P_t G_t G_r}{\sigma}. \quad (8)$$

Equation (11) can therefore be used to predict signal intensity at any point of observation. Conversely, loss σ and received signal intensity are inversely related to each other (see (8) [2]); by substitution and logarithmic approach, loss gives

$$\sigma \text{ (dB)} = \sigma_0(d_0, f_0, \epsilon_e, \mu_e) + 10m \log\left(\frac{d}{d_0}\right) + 10n \log\left(\frac{f}{f_0}\right) + \delta, \quad (9)$$

$$\sigma_0(d_0, f_0, \epsilon_e, \mu_e) = 10 \log\left(\frac{4\pi d_0^m f_0^n}{\epsilon_e \mu_e c}\right).$$

For single layer dielectric structure,

$$\sigma_0(d_0, f_0, \epsilon, \mu) = 10 \log\left(\frac{4\pi d_0^m f_0^n}{\mu \epsilon c}\right). \quad (10)$$

For multilayer dielectric structures,

$$\sigma_0(d_0, f_0, \epsilon_e, \mu_e) = 10 \log\left(\frac{4\pi d_0^m f_0^n}{c \epsilon_e \mu_e}\right), \quad (11)$$

where f is in Hz, the space between cores/chips d can be in mm (millimeter), μm (micrometer), cm centimeter, and so on depending on application and technology, d_0 is the reference distance, f_0 is in Hz, σ_0 is the reference attenuation in dB, k is the zero mean Gaussian distributed random variable (dB), c is the speed of light, and m and n account for interference, dispersion, noise, and so on which are frequency dependent. Exponents m and n are the power loss factor which could be determined by fittings from measurement data.

3. Measurement and Analysis

An interchip channel measurement using a computer motherboard or computer casing was conducted. It was difficult to put antenna close to mounted chip surface because of large-area chips which are not readily available and presence of discrete components. Hence, two UWB antennas (structure appears in Figure 2) whose measured impedance bandwidths were placed vertically with a right angle connector. The employed UWB antenna has free space measured S_{11} shown in Figure 3 lower than -10 dB over 6.7 GHz from 3.75 to 10.45 GHz and the measured free space radiation patterns in E and H planes are shown in Figure 4 where the antenna display quasi omnidirectional patterns. Normalized transfer function and group delay are given in Figure 5. For proper channel sounding in the computer motherboard, pair of 20 cm semiflexible cable was positioned between antennas and network analyzer cables. The network analyzer employed is an Agilent PNA-L network analyzer of model N5230A up to 20 GHz and measurements were carried out on a typical commercial desktop LENOVO computer case, where different components such as hard drive, floppy drive, zip drive, memory, and graphic card are mounted.



FIGURE 2: UWB antenna structure.

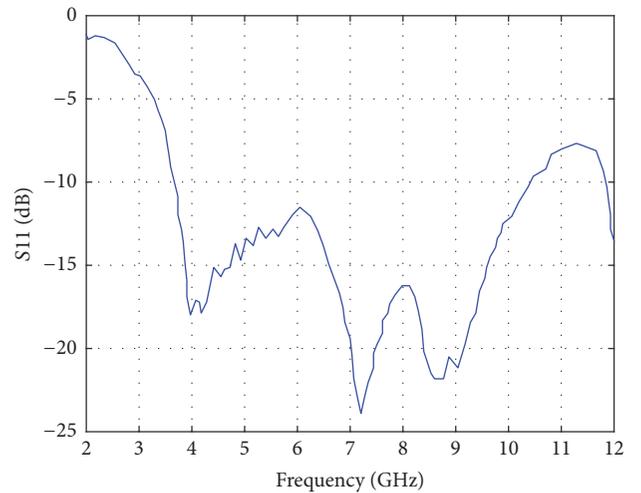


FIGURE 3: Free space measured S_{11} of UWB antenna.

The measurement setup appears in Figure 6 and a photograph is shown in Figure 7. For all measurements taken, the computer case was placed on laboratory electronic work bench and recording was taken for both closed and open of computer case. No object was moving around during measurement and for closed computer case, the closure was well shielded against any outside interferences. Hence, the multipath channel is frozen or quasistatic. CPU fan and heat-sink were removed for the convenient measurement and sampling frequency range chosen is 3.1–10.6 GHz in order to obtain the highest allowable emitting power under FCC regulations. Series of measurements were taken: (1) between CPU and chip Y: transmitting antenna positioned on top of chip Y and receiving antenna moves on the grids of CPU; (2) chip X and CPU: there was non-line-of-sight due to graphic card inside the case, transmitting antenna positioned on chip X and receiving antenna on the grids of central processing unit.

Figure 8 shows typical NLOS received power when computer case is closed curve fittings of path loss to the proposed

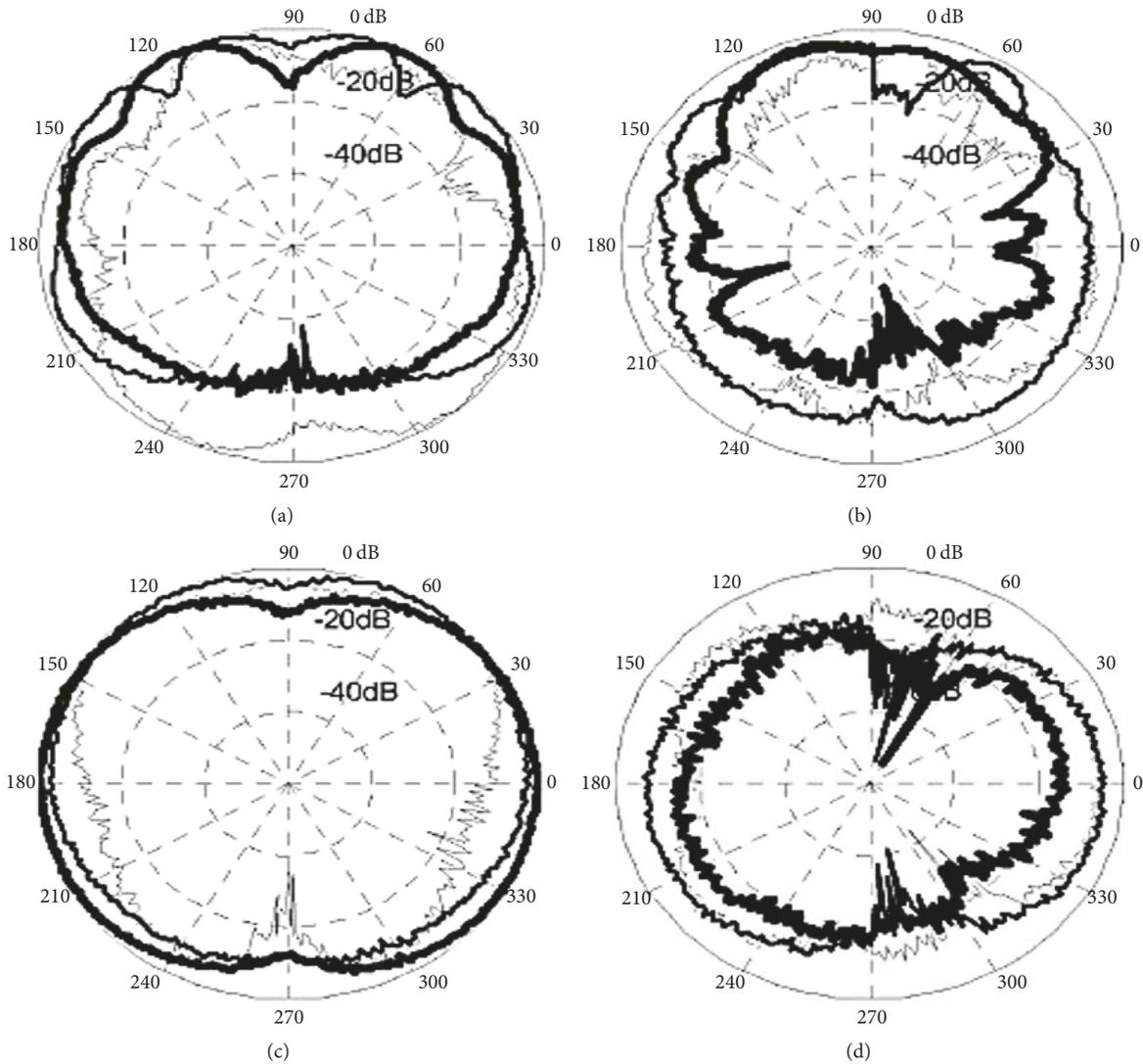


FIGURE 4: Radiation patterns of UWB antenna (free space measurements obtained): (a) and (b) are E-plane co- and cross-polarization, respectively; (c) and (d) are H plane co- and cross-polarization, respectively. Thick-line 3.5 GHz, normal line 6.85 GHz, and thin line 10.0 GHz in each plot.

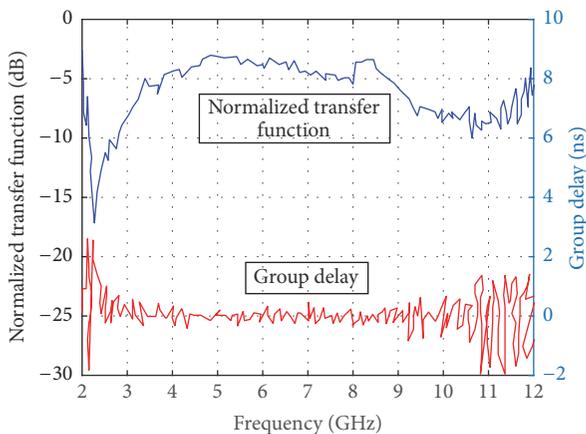


FIGURE 5: Normalized transfer function and group delay of UWB antenna.

model which was performed in Matlab with 95% confidence level and parameter extracted is as summarized in Table 1 while fittings of path loss scatter plot are as shown in Figure 9. Discrete components in close proximity of antennas during measurements altered antenna characteristics and the effect cannot be calibrated out from sampled chip-to-chip interconnect response. Path loss factors were affected by multipath in the computer case. In computer closed case, energy bounces inside the case which consequently leads to lower path loss factor and low power attenuation. During open case scenario, energy goes out of the case while the remaining portion got reflected and as a result leads to higher path loss factor and power loss. Path loss between casing closed and casing opened increases when interconnect distance increases. Reflected energy from metal cover is firstly collected before scattering out, the intensity which is

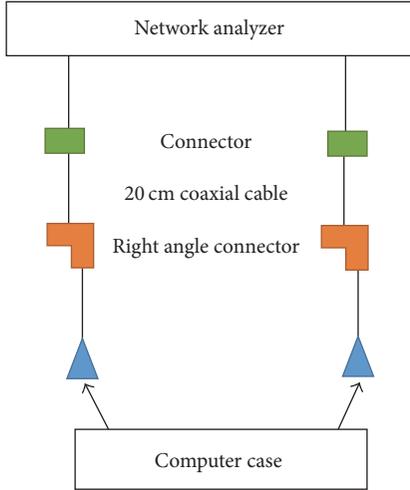


FIGURE 6: Computer case measurement campaign.

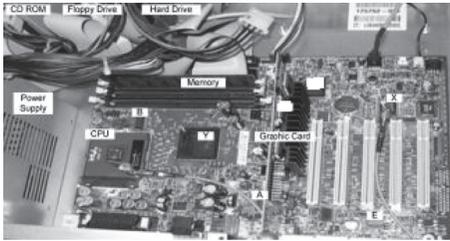


FIGURE 7: Computer casing (motherboard) photograph.

TABLE 1: Model parameters.

Parameter	Closed case	Open case
d_o (mm)	62.2	62.2
σ_0 (dB)	24.87	27.02
f_o (GHz)	1	1
m	1.75	3.41
n	0.87	0.73
δ	0.482	2.15

a function of metallic material properties (formulated in the reference path of the proposed model). It was observed that the closed casing has more uniform environment because of lower shadowing effect δ .

4. Model Simulation and Evaluation

As shown in Figure 10, proposed model matches the experimental results closely, and this shows that fitted parameters appearing in Table 1 are appropriate and therefore suitable for chip-to-chip interconnecting. It can be used to abstract the actual propagation characteristics of electromagnetic waves utilized for conveying certain information in a compact or open form. Generally, the model developed is appropriate for the characterization and modeling of interconnects in chip-to-chip wireless communication. In the past, various models

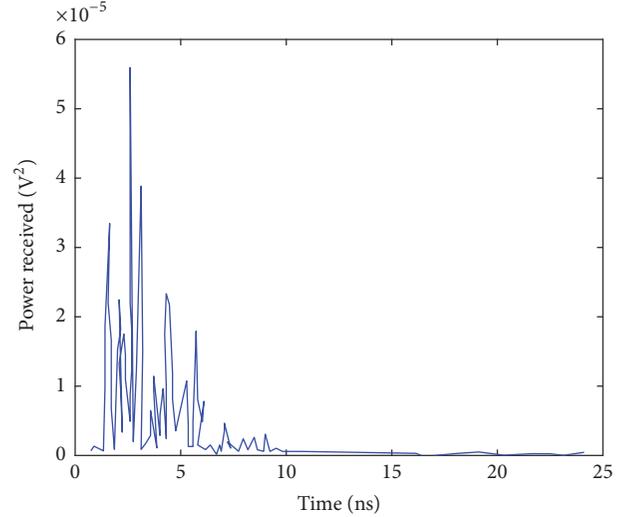


FIGURE 8: Received power in NLOS for computer case closed.

have been developed to adequately predict channel path loss but none considered dielectric material effect and because characteristic impedance of transmission line varies with the material property, this yields the reflection loss due to mismatched impedance at the source and load of transmission line. Also loss tangential factor of each material has significant effect on the loss profile. Electromagnetic permeability in free space is approximately $4\pi \times 10^{-7}$ H/m while permittivity varies with material property. Four dielectric materials were tested; that is, silicon, Teflon, beryllia, and gallium arsenide were examined to show electromagnetic propagation in a nonuniform material at 10 GHz and the results are shown in Figure 11. Dielectric material loss intensity varies from material to material; this must therefore be considered for efficient wireless chip network designs. A quantitative comparison between previous path loss models for chip-to-chip communication and the proposed model becomes important, thereby given in Table 2. Power decay rate change over distance in Figure 12 is explained by

$$Z = md + z_0, \quad (12)$$

where m , d , and z_0 are the slope, T-R distance in mm, and decay rate at zero interception distance, respectively. The decay rate parameters over distance are summarized in Table 3. It can be observed that decay rate is higher with opened case than that of the closed case; this is because closed case allows signal to bounce more time before it decays completely. Negative values m imply that when T-R distance increases, signal has more paths to arrive at the receiving antenna consequently resulting in a lower time decay rate. Open case steeper slope indicates that increase in the number of paths in proportion to T-R distance is more important for open case scenario. For closed case, there present many paths even for short distance due to the closed environment; hence, increase in number of paths due to increase in T-R distance is not as critical as that in open case. The variation of energy among grids of chips has been investigated in

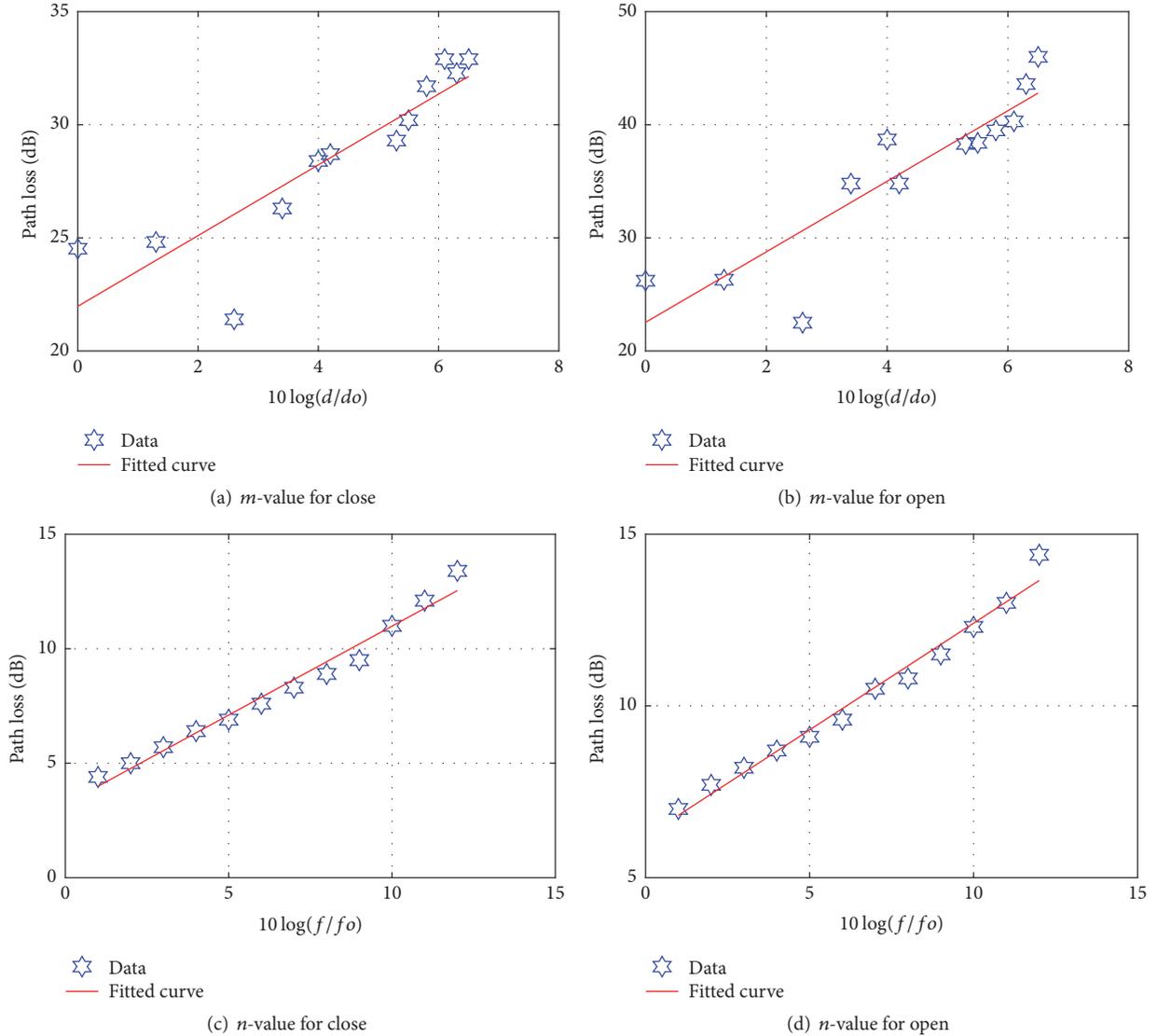


FIGURE 9: Interchip channel loss intensity curve fitting.

TABLE 2: Comparison between previous models and the developed model.

Work	Nature	Antenna parameters	Frequency dependency	Shadowing effect	Single dielectric	Multidielectric
[13]	Empirical	Yes	No	Yes	Yes	No
[17]	Empirical	Yes	No	Yes	Yes	No
[18]	Analytical	No	Yes	No	Yes	No
This paper	Analytical	Yes	Yes	Yes	Yes	Yes

TABLE 3: Decay rate parameters.

Parameter	m (dB/ns/mm)	z_0 (dB/ns)
Case closed	-0.005293	2.658
Case open	-0.00732	4.387

small scale analysis presented in Chen and Zhang [17] while this work focuses mainly on large-scale analysis. As signal propagates through the medium with multimaterial causes

different level of absorption as a result of different molecules presents in the material substances. The proposed model is therefore adequate for interchip interconnects path loss characterization and modeling for effective electronic circuits and systems designs.

5. Conclusion

In this paper, an analytical channel model has been proposed for the interconnect characterization and modeling

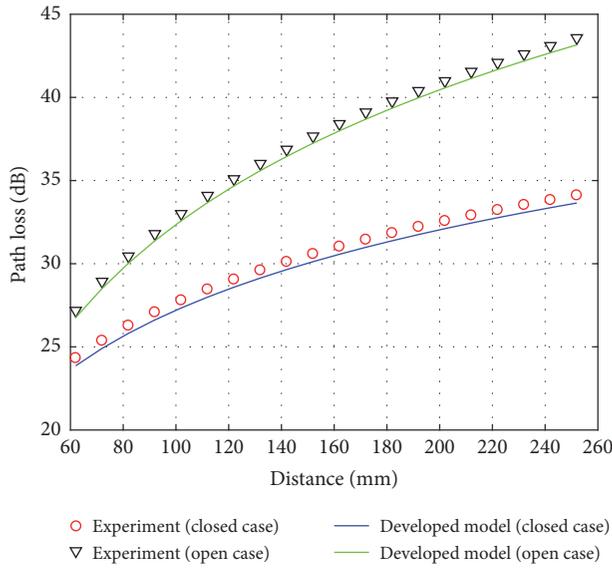


FIGURE 10: Developed model versus experiment.

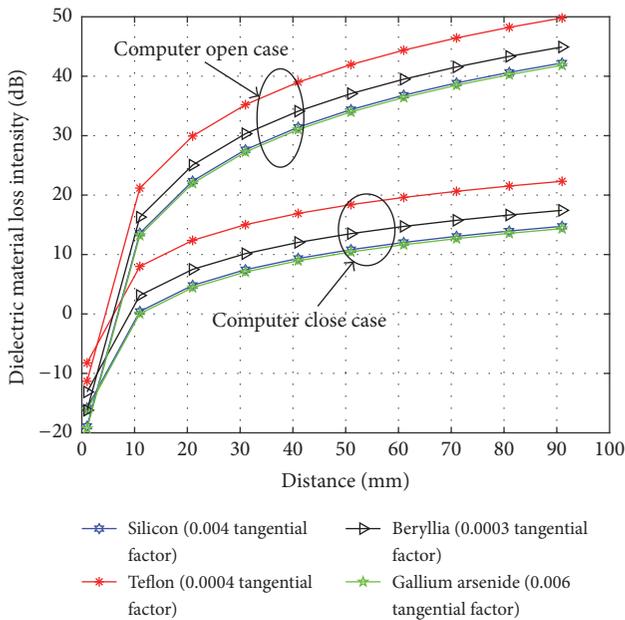


FIGURE 11: Proposed dielectric material dependency loss intensity prediction profile for open and closed case.

of wireless chip-to-chip network in single and multimaterial high-speed system design. The transmission of EM waves via a medium causes molecular absorption due to various molecules within the material substance. The statistical analysis of interchip wireless interconnect evaluated with measurement data in a desktop computer cases which represents practical interchip wireless platform and a close matching was observed. It equally incorporates dielectric material property of the environment of propagation which turned out to be an important factor in system design. The proposed model is recommended for interchip wireless interconnect

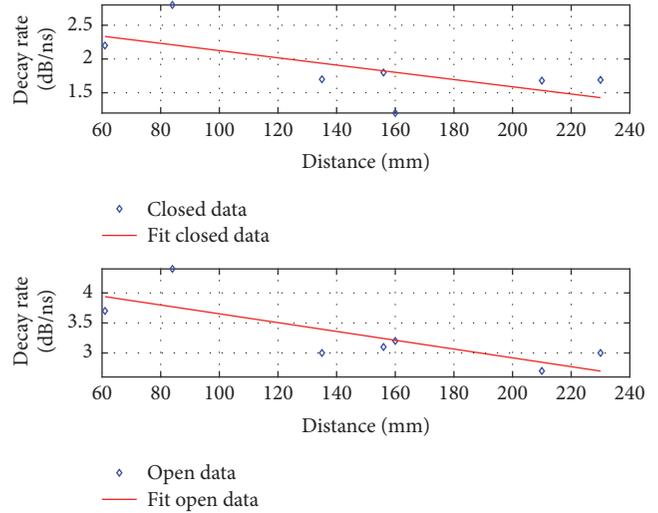


FIGURE 12: Decay rate profile over distance.

characterization and modeling towards efficient and adequate electronic circuits and systems design.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

Experiment was conducted in Micro-/Nano-Electronic System Integration Center of USTC. This work is financially supported by CAS-TWAS president fellowship.

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