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Resolution Enhancement in I_{DDQ} Testing for Large ICs*†

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Current drawn by a static CMOS VLSI integrated circuit during quiescent periods is extremely small and is normally of the order of nanoamperes. However, it is remarkably susceptible to a number of failure modes. Many faults present in such ICs cause the quiescent power-supply current (IDDQ) to increase by several orders of magnitude. Some of these faults may not manifest themselves as logical faults, and would not be detected by traditional IC test techniques.

In large ICs, it may be hard to distinguish between larger IDDQ due to defects and elevated IDDQ due to normal parameter variations. A statistical characterization of the problem is presented. This can be used to determine the optimal size of partitions. A new information compression scheme is presented which can significantly enhance resolution.

Key Words: I_{DDQ} *Testing; Built-in Current Sensing; Current Monitoring;* I_{DDQ} *Signatures; VLSI Testing*

The use of leakage current measurement to detect faults in CMOS ICs has been under consideration for a number of years [1]. Recent studies on leakage current based testing techniques [2], [3] have concluded that it is necessary to include IDDQ monitoring to obtain highly reliable CMOS ICs. The data presented for four sample CMOS ICs showed that the defect detection increased between 60% to 180% when IDDQ monitoring is added to a functional test set [2].

In the next section we review the research on current testing. We then discuss the statistical characterization of the currents of the circuits, and analyze the partitioning of a circuit for the purpose of improving the resolution of the current testing. We propose a new signature scheme for IDDQ testing and summarize our findings in the conclusion.

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BACKGROUND

There are several reasons for using IDDQ monitoring for testing of ICs [4], [5]. Traditional IC testing techniques are not effective in detecting a number of failure modes in CMOS ICs. In general, faults such as gate oxide shorts [4], [6]–[10], certain bridging faults [11]–[14], certain open faults, stuck-on faults [7], punch-through faults, operation induced faults [15], parasitic devices, pn junction leakage, and abnormally high contact resistance, may not manifest as logic faults and therefore will not be detected by traditional tests which monitor the output logic levels. These localized defects degrade the electrical performance of the circuit without affecting the logical operation performed by the circuit. Parametric faults such as incorrect threshold voltage, excessive parasitics, etc., are also difficult to detect by traditional test techniques, and often affect circuit signal delays as well as the power consumption. Implementing IDDQ testing prior to burn-in has resulted in a significant decrease in the fall-out [5].

A major fraction of failures caused by circuit fatigue will first appear as parametric drifts. Progressive gate oxide leaks, for example, may not initially affect the functionality of a device, but could become shorts during a short time leading to the failure of a device [7]. Eventually some of them will advance enough to alter the logical behavior or circuit failure. Leakage current based testing will detect these parametric drifts before they actually change the circuit behavior. Data exists that show that a device that fully passes the logic functional tests but fail the IDDQ test, fall in a significant category that functionally fail more frequently in early life than normal [4].

Current testing also is an invaluable tool for detecting faults in devices that contain both analog and digital functions on a single substrate [16]. In near future, a large fraction of devices are expected to combine digital and analog functions on a single substrate [17].

The off-chip current testing has several other advantages over the traditional functional testing techniques [1]. In functional testing, the site of a fault has to be excited and the effect of the fault has to be propagated to the output. In IDDQ testing, the propagation of the effect is automatic. Further, it can provide transistor level resolution as opposed to gate level resolution. Off chip current testing has proved to be very efficient for circuits like static RAMs [18].

Most of the gate oxide shorts cannot be modeled as stuck-at faults, especially for transistors with $W/L \gg 1$ [19]. The use of current measurement techniques to find the gate oxide leaks is investigated in [20], and techniques are presented to test quiescent IDDQ to a 1 μa limit on every clock phase of a functional test. It also identifies several problems associated with the measurement of IDDQ. The current drawn by I/O circuits, for example, could mask the current drawn by a fault. Other problems identified include wideband noise across the load capacitance, dielectric absorption in output pads, input capacitance offered by the VDD pin, and the presence of mixed logic and redundant cells. To overcome these problems, use of several techniques during the design of ICs has been proposed, including the use of separate VDD pins for output buffers and internal logic.

Stuck-on faults in CMOS circuits cannot be detected using traditional functional fault testing techniques. Test generation for detection of such faults, when IDDQ testing is used, is considered in [21]. Different decision processes involved in detecting such faults have been examined. The voltage level under stuck-on or bridging faults in CMOS circuits depend on the relative impedances of the transistors involved and the bridge [22]. This makes detection of such faults difficult using voltage measurement techniques. However, IDDQ testing detects such faults. It has been shown that IDDQ testing also detects multiple stuck-at faults as well as logically redundant faults [22], [23].

Most of the research in this area considers the use of IDDQ measurement techniques for detection of faults in CMOS circuits. This can be attributed to the fact that the static quiescent current drawn by a CMOS circuit is very small and therefore the detection of a fault which increases the IDDQ is relatively easy to detect. With technologies such as NMOS and TTL, the quiescent current can be fairly large, and the increase in current drawn due to a fault may not be significant enough to be detected by measuring equipment. Even so, current testing techniques have been successfully used to detect faults in TTL circuits [24]. The faults that have been detected include open circuits, stuck at faults and multiple faults.

The supply current measurement has been supplemented in [25] with the measurement of low frequency noise in supply current, the circuit delay as a function of the supply voltage, transient current as the circuit switches between states, and the noise in transient current to provide indication of incipient failure of CMOS integrated circuits.

Several factors could complicate the testing of an IC by current measurements. One such example is the strong non-linear characteristics of certain defects. It has been suggested that IDDQ be measured at the highest possible VDD to overcome this problem. It has, however, been observed that a measurement of IDDQ vs VDD could often identify the nature of the defect causing IDDQ elevation [2]. High IDDQ logic states are inherent in some designs and may occur unintentionally in others. Examples of such conditions include internal bus contention states in microprocessors, and IC's with analog circuitry [26].

One obstacle for commercial acceptance of current testing of ICs has been the relatively slow measurement rate compared to normal logic testing. Typically, current testing is done at a rate less than 100K test patterns per second [20], whereas the functional testing can be carried out at the normal operating frequency of the device under test. The speed of IDDQ testing is limited by several factors. The width of transient current pulse, loading of VDD pin due to output buffers and the impedance of the probing circuitry are some of them. It has been demonstrated that the rate of testing can be increased by several

orders of magnitude by isolating the output buffers of an IC from the VDD pin [2]. IDDQ testing was demonstrated to reduce line fallout after 99.6% stuck-at fault testing failed to achieve desired quality goals [27]. The high resolution required for current testing has been cited as another problem that makes acceptance of current testing difficult at present [3].

The key to performing an effective IDDQ test is the probe circuit used to measure the current. Such a circuit should be capable of measuring small currents, without affecting the supply voltage especially during transients, and must be capable of fast measurements [28]. The different types of current probes in use are examined in [28], and a probe circuit has been proposed which allows a system to perform dynamic IDDQ tests as an integral part of the functional testing of a CMOS device.

Built-in current sensing techniques have been proposed to overcome the disadvantages of existing off-chip current testing techniques. Current sensors have been proposed and implemented using CMOS technology, some capable of detecting currents as small as 2 μa at 1 MHz clock frequency [3], [4]. In BIC testing, an IC is implemented using a number of modules and each module is connected to the power supply through a current sensor. Another circuit design for built-in current testing has recently been proposed [29]. The output of the current sensor of a module is observed with the proper input vectors to detect faults in that particular module. Limitations of BIC sensors due to virtual ground is given in [30].

STATISTICAL CHARACTERIZATION

Some approaches suggested for current testing involve recording the entire waveform or recording the value of IDDQ once each cycle. These approaches involve recording and processing a large amount of information. They may not be suitable for testing a large volume of devices or for a built-in-test application. The best approach is to make a binary decision each time. The IDDQ value is compared with a previously decided threshold value. If the measured value exceeds the threshold, a fault is considered to have been detected. We assume this approach in the discussions below.

IDDQ based testing requires measurement of an analog quantity rather than a digital signal in case of voltage testing. Both the normal and faulty values can vary significantly. To arrive at an upper limit of normal IDDQ and to examine limitations of IDDQ based testing, a statistical characterization of the problem is needed.

Resolution for Current Testing

In a normal CMOS device, one may view the overall conductance of the device (IDDQ/VDD) as the sum of conductances of individual cells, all connected in parallel (Figure 1). If the supply voltage is assumed to be fixed, we can write

$$\text{IDDQ} = \sum_{j=1}^{n} i_{j\text{DDQ}} \tag{1}$$

where $i_{j\text{DDQ}}$ is the quiescent supply current through cell j, and n is the total number of cells.

For each normal cell, $i_{j\text{DDQ}}$ will vary depending on the parameter values as well as the input logic signals. It can therefore be regarded as a random variable. At this time not enough data exists that will enable us to find the applicable distribution. However for a first approximation using the central limit theorem [31], we can assume that IDDQ, being a summation, has a distribution which is approximately Gaussian. If the current through an average cell, i_A is characterized by $\mu_{i\text{ADDQ}}$ and $\sigma_{i\text{ADDQ}}$ then we can assume,

$$\mu_{\text{IDDQ}} = n.\mu_{i\text{ADDQ}}$$

$$\sigma_{\text{IDDQ}} = \sqrt{n}.\sigma_{i\text{ADDQ}} \tag{2}$$

Let us now assume that at most one leakage defect exists. This is not a limiting assumption as a multiple leakage defect is likely to be tested more easily. Let us assume that the additional quiescent supply current, i_f, is characterized by the parameters $\mu_{if}(\mu_{if} = \mu_{\text{IDDQf}} - \mu_{\text{IDDQ}})$ and $\sigma_{if}(\sigma_{if} = \sigma_{\text{IDDQf}} - \sigma_{\text{IDDQ}})$. Then

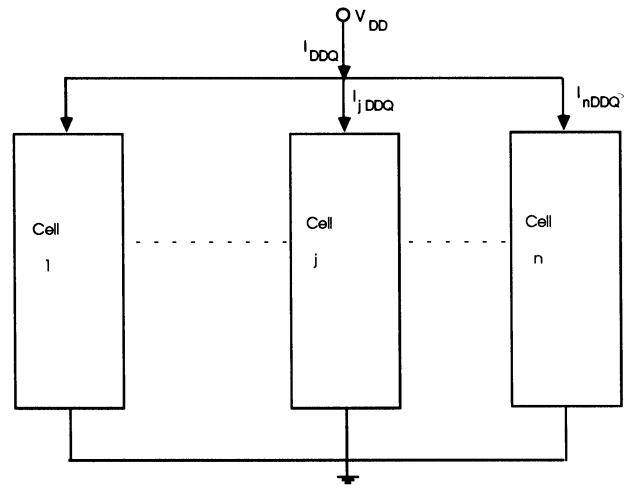


FIGURE 1 The parallel current paths in a CMOS device.

the overall supply current in the presence of a defect is given by IDDQ + i_f with the distribution given by

$$\mu_{IDDQf} = n\mu_{iADDQ} + \mu_{if} \quad (3)$$

$$\sigma_{IDDQf} = \sqrt{n\sigma^2_{iADDQ} + \sigma^2_{if}} \quad (4)$$

The distinction between the normal IDDQ and the faulty $IDDQ_f$ is easy if the two distributions are well separated. As most of the distribution is centered with $(\mu \pm 3\sigma)$, we can define the separation between the two distributions as (Figure 2):

$$\text{gap} = (\mu_{IDDQf} - 3\sigma_{IDDQf}) - (\mu_{IDDQ} + 3\sigma_{IDDQ})$$

$$= \mu_{if} - 3(\sqrt{n\sigma^2_{iADDQ}} + \sigma^2_{if} + \sqrt{n}.\sigma_{iADDQ}) \quad (5)$$

This expression (Eqn. 5) illustrates the basic problem in testing large devices. As n increases, the spread of the distributions also increase. For devices that are sufficiently large, the gap will become negative, i.e. the two distributions will overlap.

Deciding the Threshold Value

As we have discussed above, the most convenient setup for current monitoring compares the measured IDDQ with a preselected I_{DDQth}. If the measured value is higher, the device is regarded to be faulty.

As discussed above, for larger devices, the distinction between the normal and faulty values may be hard to make. A more strict screening will use a lower value of I_{DDQth}. However, this will result in a larger number of good devices being rejected.

Below we obtain an expression for the probability of incorrectly rejecting a good device.

Let I_{DDQm} be a measured value. Consider the following (Eqn. 6).

$$\text{Prob}\{\text{device is good} | I_{DDQm} > I_{DDQth}\} = \frac{\text{Prob}\{I_{DDQm} > I_{DDQth} | \text{device is good}\}.\text{Prob}\{\text{device is good}\}}{\left[\begin{array}{l}\text{Prob}\{I_{DDQm} > I_{DDQth} | \text{device is good}\}.\text{Prob}\{\text{device is good}\} \\ \quad + \text{Prob}\{I_{DDQm} > I_{DDQth} | \text{device is bad}\}.\text{Prob}\{\text{device is bad}\}\end{array}\right]} \quad (6)$$

where the right hand side is obtained by using the Bayes' rule.

An optimal value of I_{DDQth} would be arrived at by considering the cost of rejecting a good device versus the cost of passing a bad device. Many devices are

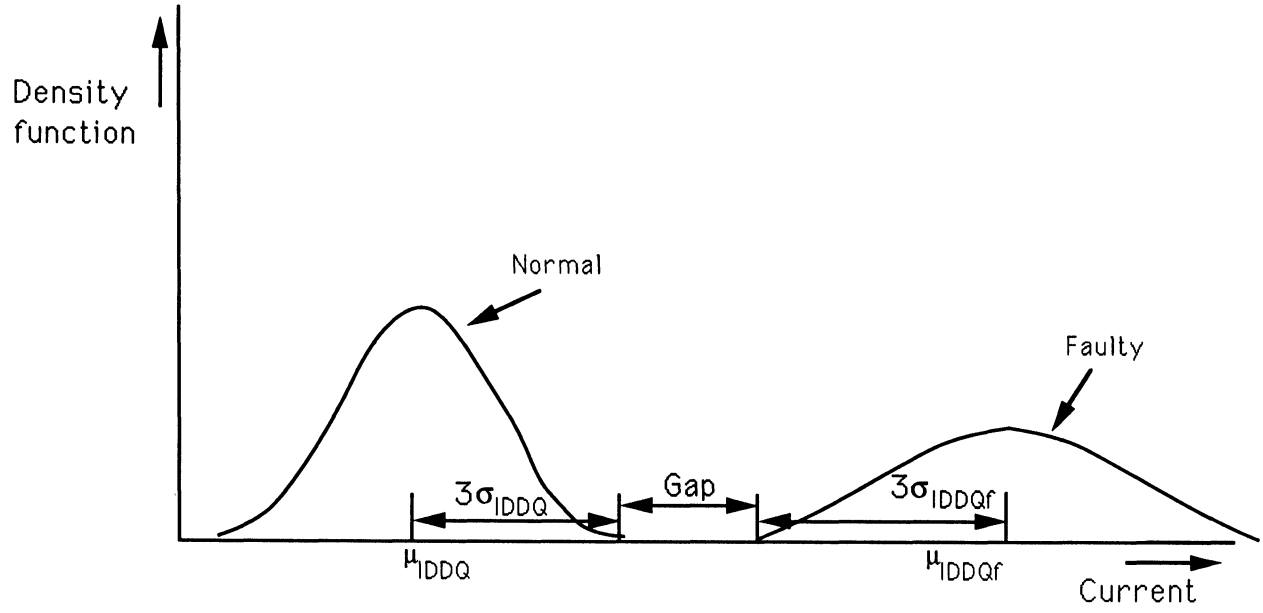


FIGURE 2 The 'gap' between normal and faulty value.

marginal, allowing a larger supply current, but the logical operation is correct. The cost of using these devices is the higher drain on the power source as well as significantly reduced reliability because of the heat generated.

PARTITIONING

From the discussion in the previous section, we have seen that the gap between the normal and faulty distributions will decrease when the number of cells n increases. If the number of the cells of a device exceeds a certain value, the gap becomes negative, i.e., the two distributions overlap. Under this situation, it would be difficult to distinguish the faulty current from the normal one. The solution to this problem will be to partition the device under test into modules. Each module will have its own current sensor. Thus these modules can be tested independently. Similar equations about the parameters of the distributions can be established for each module. And the size of each module can be controlled such that the faulty and normal distributions within each module can be distinguished.

Below we obtain the criteria for a valid partitioning for this device.

The same equation for the gap applies for each module:

$$\text{gap} = \mu_{if} - 3(\sqrt{n\sigma^2_{i\text{ADDQ}} + \sigma^2_{if}} + \sqrt{n}\sigma_{i\text{ADDQ}}) \tag{7}$$

where n is the number of cells in one module.

Let us assume that maximum size of each module is determined by letting gap by 0. Although we have to use numerical methods to obtain the exact value of n, we can derive the upper bound of n as follows:

$$\mu_{if} = 3(\sqrt{n\sigma^2_{i\text{ADDQ}} + \sigma^2_{if}} + \sqrt{n}\sigma_{i\text{ADDQ}}) \tag{8}$$

Since the term $(\sqrt{n\sigma^2_{i\text{ADDQ}} + \sigma^2_{if}})$ in the above equation is greater than $(\sqrt{n}\sigma_{i\text{ADDQ}})$, μ_{if} can be written as:

$$\mu_{if} \geq 6\sqrt{n}\sigma_{i\text{ADDQ}} \tag{9}$$

So the upper bound of maximum n, denoted by n_b, is

$$n_b = \left(\frac{\mu_{if}}{6\sigma_{i\text{ADDQ}}}\right)^2 \tag{10}$$

Hence the device can be partitioned into modules whose sizes will not exceed n_b, and all the modules will have approximately the same number of cells.

CMOS circuits of different levels (1, 3, 5 and 10 levels) were chosen for simulation with BICS (Built-in Current Sensor) to determine the time for current to settle. The number of levels indicate the number of gates connected in series with one another. For example, simulation for 5 levels totaling 500 gates has 5 gates connected in series with 100 such series of gates in parallel. Figure 3 shows plots for I_{DDQ} settling time vs. total number of gates for different levels of CMOS circuits. The current is sampled by the BICS only after all the transients due to switching have completed and the current has settled to a steady low current value [3]. The settling time shown in Figure 3 shows the time when the current has settled to about 5% of the steady low current value for sampling by the BICS. The settling time for a 10-level circuit for example, is greater than that of a 5-level circuit with the same number of gates due to the larger propagation delay in the former. For a circuit with a given level, the settling time increases with the number of gates. The settling time thus has two components, one due to the propagation delay, and the other due to the capacitance at the node to which the current sensor is connected. Thus the larger the circuit that is covered by a current monitor, the longer the second component of the transient time will be. Another advantage of partitioning is the reduction of this component of settling time due to the total capacitance.

A NEW SIGNATURE SCHEME

Here a new scheme is presented, which reduces the probability of making an incorrect decision. It also

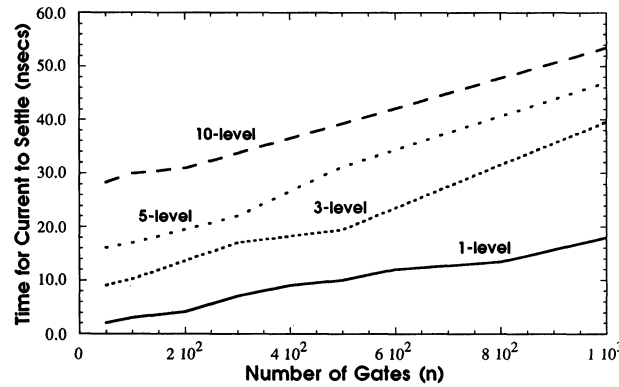


FIGURE 3 I_{DDQ} settling time vs. number of gates for different levels.

allows for high IDDQ states, which may occur in some normal devices for some test vectors [20].

Consider application of a set of test vectors for which current monitoring is done. The output of the sensing circuit is a binary sequence where a '1' represents the fact that I_{DDQm} is greater than I_{DDQth} for that vector. Rather than basing a decision on a single '1', the string can be compressed into a signature, which can be used for evaluation. Since the faults cause a unidirectional error (i.e. 0 to 1) adding the number of '1's can be an appropriate signature. If this signature S is greater than a preselected value S_{th}, the device is rejected.

The effectiveness of this scheme is due to the fact that by multiple samplings, more information is used for decision making.

Consider a situation when m randomly chosen vectors are applied, where $m > S_{th}$. The probability of rejecting a good device then is given by the following:

$$\text{Prob}\{S > S_{th} | \text{device is good}\} = \sum_{S=S_{th}-1}^{m} \binom{m}{s} (1-p)^S p^{m-S} \quad (11)$$

where

$$p = \text{Prob}\{I_{DDQm} < I_{DDQth} | \text{device is good}\} \quad (12)$$

It is easy to see that this probability declines with increasing S_{th}. Let us also consider the probability of incorrectly accepting a bad device,

$$\text{Prob}\{S < S_{th} | \text{device is bad}\} = \sum_{S=0}^{S_{th}} \binom{m}{s} (1-q)^S q^{m-S} \quad (13)$$

where

$$q = \text{Prob}\{I_{DDQm} < I_{DDQth} | \text{device is bad}\} \quad (14)$$

Again it is easy to see that this probability increases with increasing S_{th}.

Thus the optimal value of S_{th} can be obtained only by obtaining a suitable cost function involving these two probabilities.

The simplest current sensor can be built with either a resistive or a capacitive element (labeled by 'X' in Figure 4) along with a voltage comparator, as shown in Figure 4. The current flow will cause a voltage drop on the element X and the voltage on X is fed to the comparator [28], [32]. The other input of the comparator is the standard voltage which would result from I_{DDQth} on the same capacitor. Therefore, if the measured current I_{DDQ} is greater than I_{DDQth}, the output of the current sensor is 1. If I_{DDQ} is equal to or smaller than I_{DDQth}, the output of the current sensor is 0.

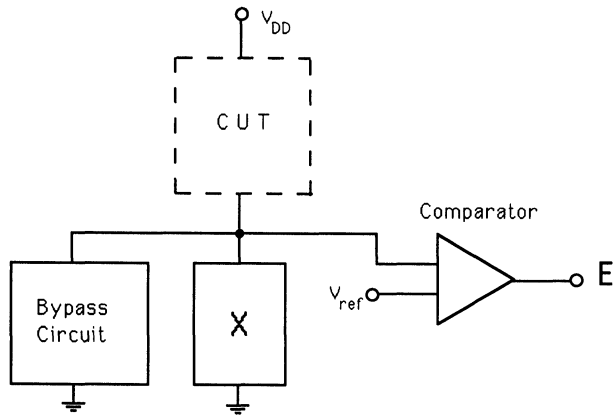
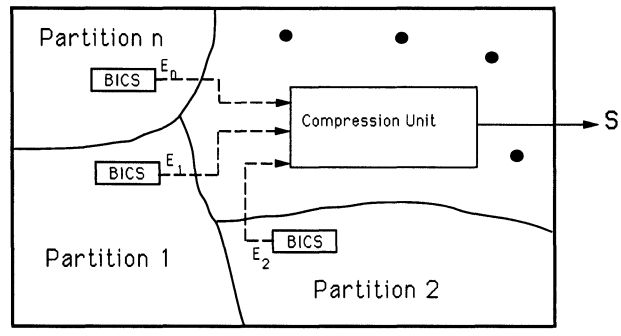


FIGURE 4 A general current sensor.

The signature is obtained by counting the number of times when the detected current flow exceeds I_{DDQth}, which is denoted by S. If $S \geq S_{th}$, as discussed in the previous paragraph, then the device is regarded to be faulty. The logic circuit that is used to extract the information about the signature is called signature extractor.

Since each module or subcircuit has its own current sensor, it is impractical to observe the output of every current sensor. One solution to this problem is to propagate the outputs of all the sensors to one observable output pin which is designed solely for the signature extractor. This signature extractor may be implemented simply by an OR gate. The outputs from all the current sensors are fed to the OR gate. A counter is connected to the output of the OR gate, as shown in Figure 5, to calculate the total number of times that the detected current I_{DDQ} exceeds I_{DDQth}, which is nothing but the signature S.



BICS - - Built-in Current Sensor

FIGURE 5 Partitioning and information compression.

This signature extractor also works correctly if there are more than one faulty module since in that case S will be even greater than that when there is only one faulty module.

CONCLUSIONS

Testing of large ICs using IDDQ monitoring require larger test times and exhibits lower resolution between faulty and fault-free devices. A statistical characterization of the quiescent current of a circuit module under normal and faulty conditions was presented. The characterization was used to obtain a criterion for optimally partitioning a large circuit into smaller modules for higher resolution in current monitoring. The partitioned circuits need lower test time and result in enhanced resolution for IDDQ monitoring. A new signature scheme is proposed which allows the BICS outputs from several partitions to be compressed. It is shown that this scheme will further enhance resolution.

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