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Fault Characterization and Testability Analysis of Emitter Coupled Logic and Comparison with CMOS & BiCMOS Circuits

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The logic behavior and performance of ECL gates under a set of defect models are examined. These are compared with equivalent set of BiCMOS and CMOS gates. It is found that logical fault testing is inadequate for obtaining a sufficiently high fault coverage, e.g., 79% for ECL versus 54% for BiCMOS and 69% for CMOS equivalent gates. Performance degradation faults such as delay, current and Voltage Transfer Characteristics (VTC) or Noise Margin (NM) faults are analyzed as applied to these gates. It is shown that logical fault testing with delay fault testing yields the highest fault coverage for BiCMOS and CMOS gates (around 95%). However, for equivalent ECL gates to attain a fault coverage of around 98%, both logical and NM fault testing have to be used.

Key Words: *Testability analysis; Defects; Faults; Fault simulation; Synthesis for testability; Digital VLSI circuits*

Emitter Coupled Logic (ECL) devices operate out of saturation which eliminates transistor storage time as a speed limiting characteristics, thus permitting very high speeds of operation [1]. Conventional ECL technology provides system propagation delays of the order of 300 to 500 ps. However, the price paid for such speeds is very high power dissipation (more than 2 mW per gate) [2–4]. With recent advances in technology such as BIT1 [2], it becomes possible to fabricate ECL devices that take about 1/20th the area of conventional ones, with speeds comparable to the fastest ECL transistors and consuming only 1/10th of the power.

As a result of the low power, high speed and relatively high density, ECL technology is used in the design of Application Specific Integrated Circuits (ASICs) which are frequently utilized in applications demanding the highest circuit performance. It is also important to mention that ECL technology is currently used in BiCMOS processes, whereby ECL circuit islands embedded in BiCMOS circuits are required for critical path regions and for high speed operations.

With the increase in performance and complexity of ECL circuits, the testability issue becomes very important in the design process. The issue of fault modeling of ECL gates has been addressed in [3–6]. The fault models presented in [3–5] only consider logical faults; however, performance degradation faults, which could not be characterized by a failure in the device logic, are not discussed. For example, ECL high and low level noise margins are small (around 0.3V), and these make the circuits susceptible to noise or fluctuations that inevitably appear on the power supply line. In the presence of defects, the noise margins could be further reduced, which would increase the susceptibility of ECL circuits to noise. This, in effect, leads to performance degradation faults which can be detected through performance analysis of the ECL circuits. In order to detect many of the possible faults, it is necessary to consider the two categories of the defect generated faults.

The objective of this paper is to perform a comprehensive testability analysis on ECL digital circuits and to compare it with equivalent CMOS and totempole BiCMOS circuits [7]. This comparison is useful for contrasting the categorization of faults in the ECL technology with like faults in BiCMOS and CMOS processes. The analysis also helps to provide the fault categories which might lead to the testing method

with the highest fault coverage. It is shown that testing techniques for at least two fault models are necessary for obtaining a high fault coverage in ECL as well as BiCMOS and CMOS gates.

ECL BASIC CIRCUITS

In a BiCMOS environment, ECL circuits are mainly used for critical paths to minimize signal skew, for high speed processing, and to provide the interface to other ECL and TTL logic families. The ECL basic circuits include the OR/NOR gate, AND/NAND gate, the reference voltage network, and ECL-CMOS and CMOS-ECL level translators. This paper emphasizes on the OR/NOR gate, AND/NAND gate and the reference voltage network.

OR/NOR Gate

The structure of a typical ECL OR/NOR gate is shown in Figure 1. It consists of two parts: the differential input amplifier pair, and the emitter follower output stage. The former provides the current switching mechanism of ECL circuits, while the latter consists of level shifters which provide the appropriate logic levels. Transistor Q4 acts as a current source for the switching of devices Q1, Q2 and Q3. The circuit responds only to difference in voltage levels at the inputs of the devices Q1 or Q2 and Q3. A relatively small difference in voltage will cause the current to flow almost entirely through Q1, Q2 or Q3.

If the voltage levels at input of Q1 and Q2 are lower than V_{ref}, Q1 and Q2 will be turned off. The constant current of Q4 is directed through R2 and transistor Q3. This will cause a voltage drop across R2 and a reduction in the collector voltage of device Q3. Since no current is flowing through R1, the collector voltage of Q1 and Q2 reaches the power supply level. Transistors Q6 and Q7 act as level shifters and buffers for inputs to the next stage, and are biased by devices Q8 and Q9. The emitter of device Q7 (which is in the logic 0 state) implements the OR operation. The NOR operation is obtained at the emitter of device Q6. On the other hand, if the input levels to either Q1 or Q2 is higher than V_{ref}, device Q3 will be turned off. Then, the constant current is directed through R1 and transistor Q1 or Q2. This reduces the voltage level at the collectors of Q1 and Q2, and raises the collector voltage at Q3 to the power supply level. Therefore, the OR output will be in the logic 1 state while the NOR output will be in the logic 0 state.

EFL Cell

Another approach to the implementation of ECL circuits is the use of Emitter Function Logic (EFL) circuit structures [8]. A typical configuration of a two-level EFL cell is depicted in Figure 2. Like in the OR/NOR gate, the EFL cell consists of a differential input amplifier and an emitter follower output stage. The reference voltage inputs are supplied by separate networks. The cell contains multiple emitter devices in both the input and output parts. Also, an input can be connected to the emitter or the base of a device in the cell. The multiple emitter

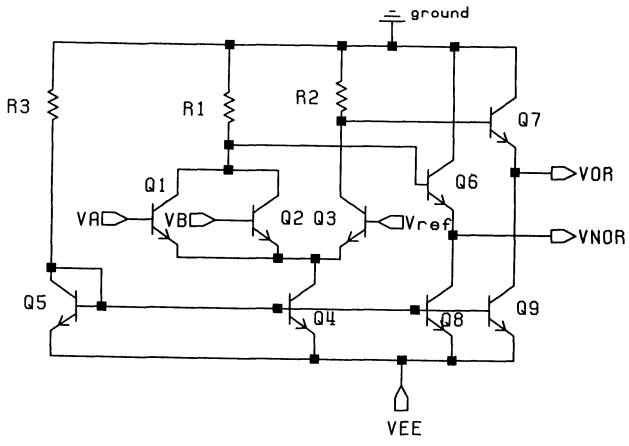

FIGURE 1 Basic ECL OR/NOR gate.

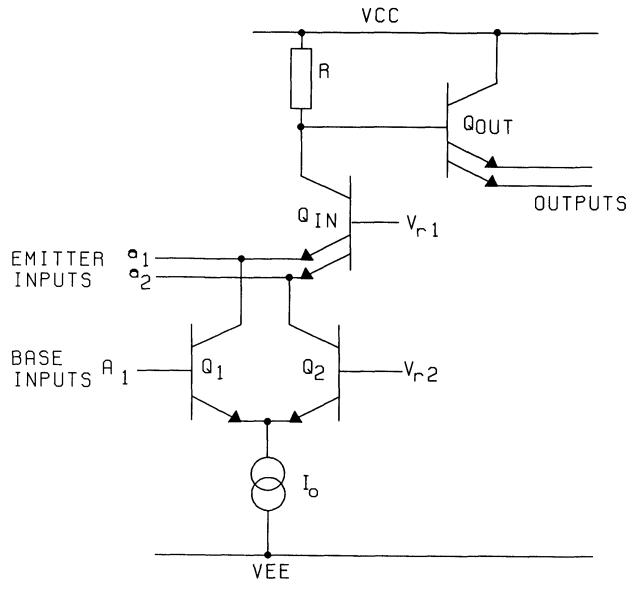

FIGURE 2 Basic Two Level EFL Cell.

devices provide multiple inputs to, or outputs from, the EFL cell. The difference in voltage levels between V_{r1} and V_{r2} is approximately V_{BE}.

If the input voltage level of device Q1 (A_1) is lower than V_{r2} (i.e. in the logic 0 state), device Q1 is off and Q2 is turned on. Now, if the voltage level of input a_1 is in the logic 1 state, there is no conduction of current through the corresponding emitter in Q_{IN}. However, assuming that the voltage level of input a_2 is in the logic 0 state, a conduction path is established in device Q_{IN}. Then, the current I_0 is directed through R via transistors Q2 and Q_{IN}. This leads to a reduction in the voltage level at the collector of Q_{IN} and causes the outputs to be in the logic 0 state. Conversely, if a_1 is in the logic 0 state and a_2 in the logic 1 state, no current flows through Q_{IN} since device Q1 is off. The current I_0 flows through input a_2 via device Q2. There is virtually no current through resistor R, thus, the collector of Q_{IN} is raised to the power supply voltage level. This will cause the outputs of the cell to be in the logic 1 state. Similar analysis can be performed for the other input voltage level combinations of A_1, a_1 and a_2.

The advantage of EFL circuits is that complex logic functions can be implemented in a modular fashion using fewer transistors and requiring less silicon area than when a combination of logic gates are used. Several combinatorial logic functions have been realized using EFL circuits and these include, OR/AND, two input AND, full-adder, multiplexer, demultiplexer, Flip-flops, etc [8].

Reference Voltage Network

The typical configuration of the temperature and voltage compensated bias network is shown in Figure 3. It consists of one BJT device, two diodes and three resistors R1, R2 and R3. By selecting appropriate values for the resistors, the desired reference voltage V_{ref}, can be obtained. In our analysis, we assume that all the reference voltage inputs to the ECL circuit are supplied by a block having this type of circuit configuration.

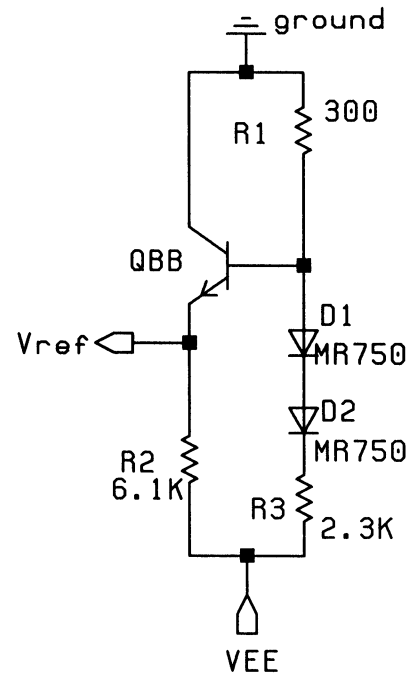

FIGURE 3 Basic reference voltage circuit.

TEST CIRCUITS

The general structure of the test circuit used in the fault analysis is shown in Figure 4. The circuit is simulated under defect free and many possible defect conditions, with the defects injected one at a time. During simulation, the supply current IDD and the primary input and output voltages are monitored to determine the behavior of the circuit. The detailed test circuit used for the ECL OR/NOR gate is shown in Figure 5. The circuit under test (CUT) is a 2-input ECL OR/NOR gate. The inputs of the CUT gate are driven by two level shifters which may be the outputs of another ECL gates. The CUT gate itself drives two loads of OR/NOR gates (load1 and load2). The load circuits are used to monitor separately the behavior of the OR and NOR outputs of the test circuit.

Figure 6 shows the details of the test circuit used for the AND gate. The CUT is a two-input EFL AND gate. As illustrated in Figure 6, the multiple emitter devices shown in Figure 2 are represented using multiple transistors with common base and collector, but separate emitters. For instance, device Q_{IN} in Figure 2 is represented with devices Q5 and Q6, while device Q_{OUT} is represented with transistors

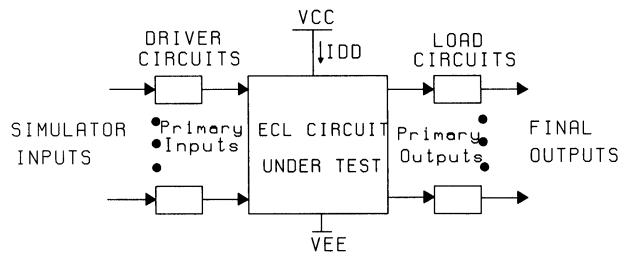

FIGURE 4 Generic test circuit.

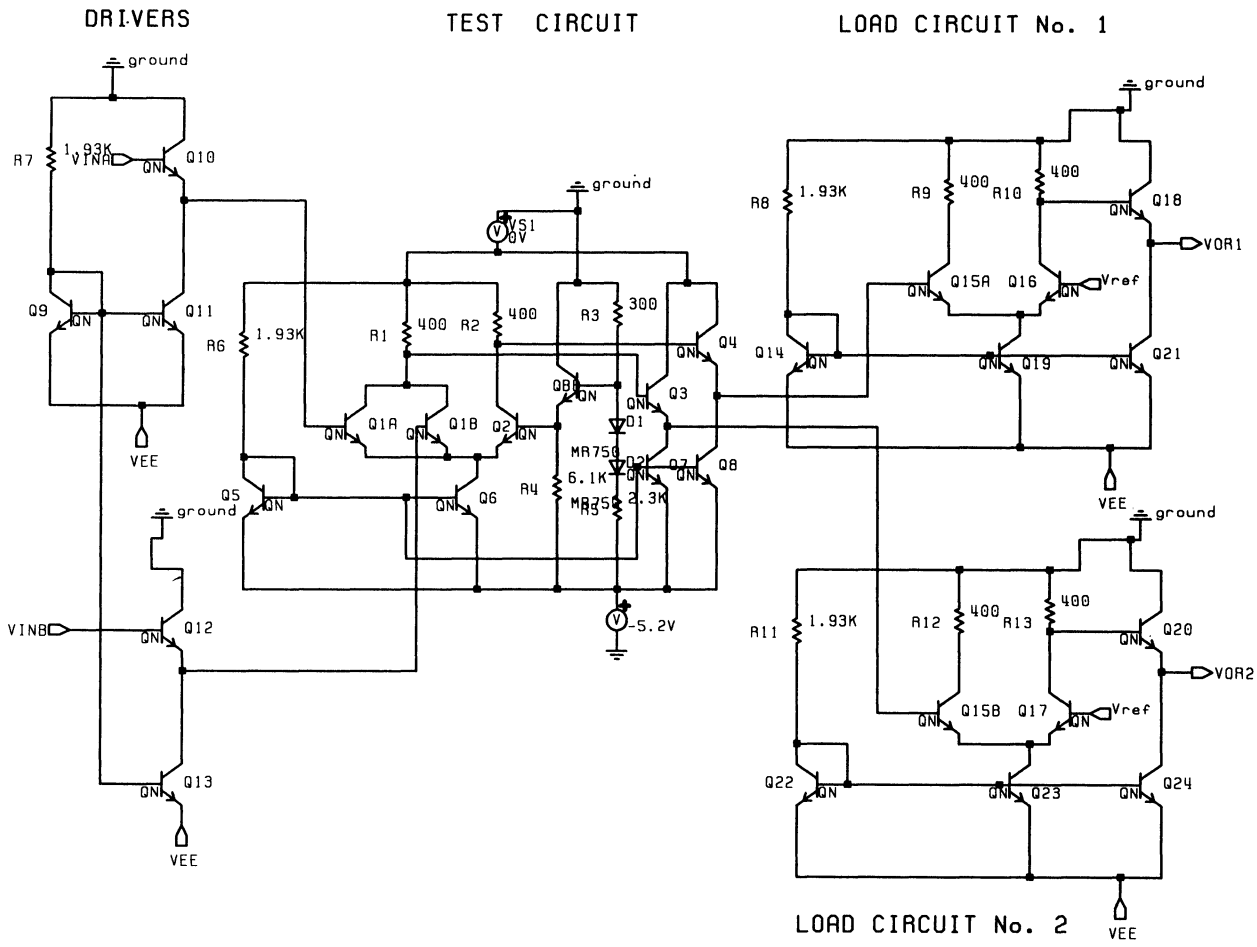

FIGURE 5 Test Circuit: ECL OR/NOR gate.

Q9 and Q10 in Figure 6. The CUT is driven by two driver circuits. The outputs of the AND gate are monitored by two types of load circuits, load type I and load type II. The difference between the two load circuits is that the AND gate output is connected to an emitter input in load type I and to a base input in load type II.

Note also that the driver for an emitter input is different from the one used to drive the base input of the AND gate, the reason being that, if the driver for the base input is used for the emitter input, for certain input voltage level combinations, more current than required will be directed through R2. For example, assume that the signals VINA and VINB are in the logic 0 state and logic 1 state respectively. Devices Q5 and Q2 will be turned on while device Q12 will be off. Then, both the current of transistor Q3 and the bias current of transistor Q12 will be directed through R2 via device Q5. This will result in a higher voltage drop across R2 and hence, more reduction than expected in the collector voltage of transistors Q5 and Q6. This phenomenon produces improper signal levels at the outputs of the AND gate.

The inclusion of the drivers in the test circuits is necessary to isolate the primary inputs from being forced to a particular voltage level by the simulator due to a fault in the test circuits.

PHYSICAL DEFECTS AND MODELS

The subsets of defects appropriate to the MOS and Bipolar fabrication processes are shown in Table I. ECL circuit defects consist of shorts and open-circuit failures in the resistors and diodes, plus failures due to the bipolar devices. The most prevalent defects in bipolar technology [7] are open connections, shorts between terminals and emitter-collector pipes with excessive leakage currents. Open-Circuit defects are modeled as a very high resistor (10 GΩ) in parallel

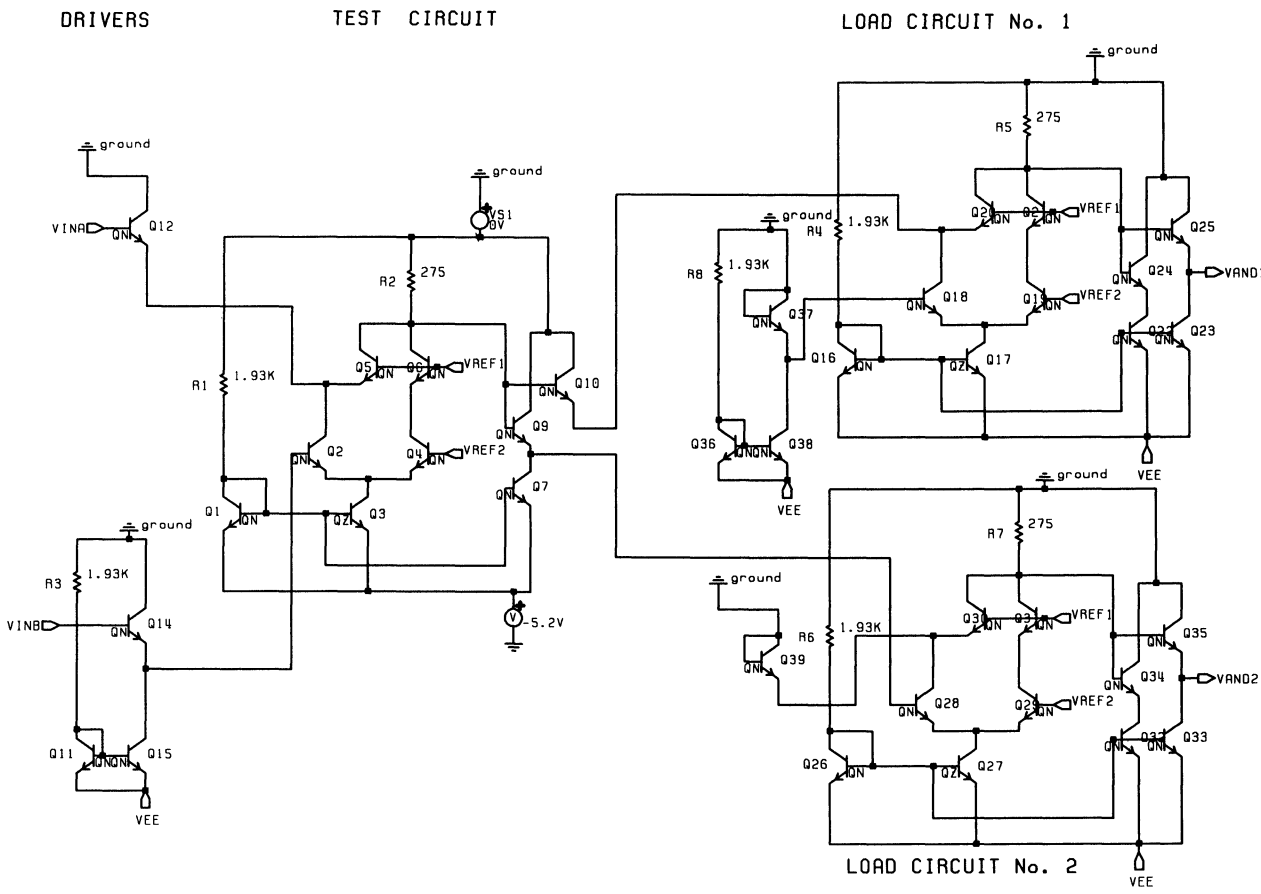

FIGURE 6 Test Circuit: ECL AND gate.

with a small capacitor (0.001 pF), inserted between the device's terminal and the node to which the terminal would normally have been connected. Short-Circuit defects are modeled as a simple connection between two nodes of the bipolar device. Emitter-collector pipes are modeled with 1 KΩ resistor inserted between the collector and the emitter of the faulty transistor [7]. It is assumed that the likelihood of occurrence of defects in the ECL circuits is evenly distributed.

TABLE I
List of MOS and Bipolar Defects

MOS	BIPOLAR
Gate-Source Pinhole	Emitter-Collector Pipe
Gate-Drain Pinhole	Base-Collector Short-Circuit
Gate-Channel Pinhole	Base-Emitter Short-Circuit
Gate-Source Short-Circuit	Collector-Emitter Short-Circuit
Gate-Drain Short-Circuit	Base Open-Circuit
Source-Drain Short-Circuit	Collector Open-Circuit
Gate Open-Circuit	Emitter Open-Circuit
Source Open-Circuit	
Drain Open-Circuit	

ANALYSIS OF PHYSICAL DEFECTS

The test circuits in Figures 5 and 6 are first simulated under fault-free condition. Figures 7 and 8, respectively, show typical operations of ECL OR/NOR and AND gates with no defect. The responses in Figure 7 for the OR/NOR gate are obtained using R1 = R2 = 400 Ω, V_{ref} (V_{BQ2}) = −1.3V, while in Figure 8 for AND gate, R2 = 400 Ω, V_{ref1} = −0.4V and V_{ref2} = −1.3V. In both test circuits, the constant current = 2.75 mA, and the supply voltages are V_{CC} = 0V and V_{EE} = −5.2V. The simulation is performed using bipolar device model parameters obtained from an existing 2 μm BiCMOS process [9]. The diode model parameters are obtained from [10]. These parameters are listed in the Appendix. From the simulation results, critical parameters are extracted to form a set of specifications to be used as a fault-free reference. The values of these parameters are shown in Table II. The delay values include those of the driver and CUT circuits, while the current values include the current supplied to the differential

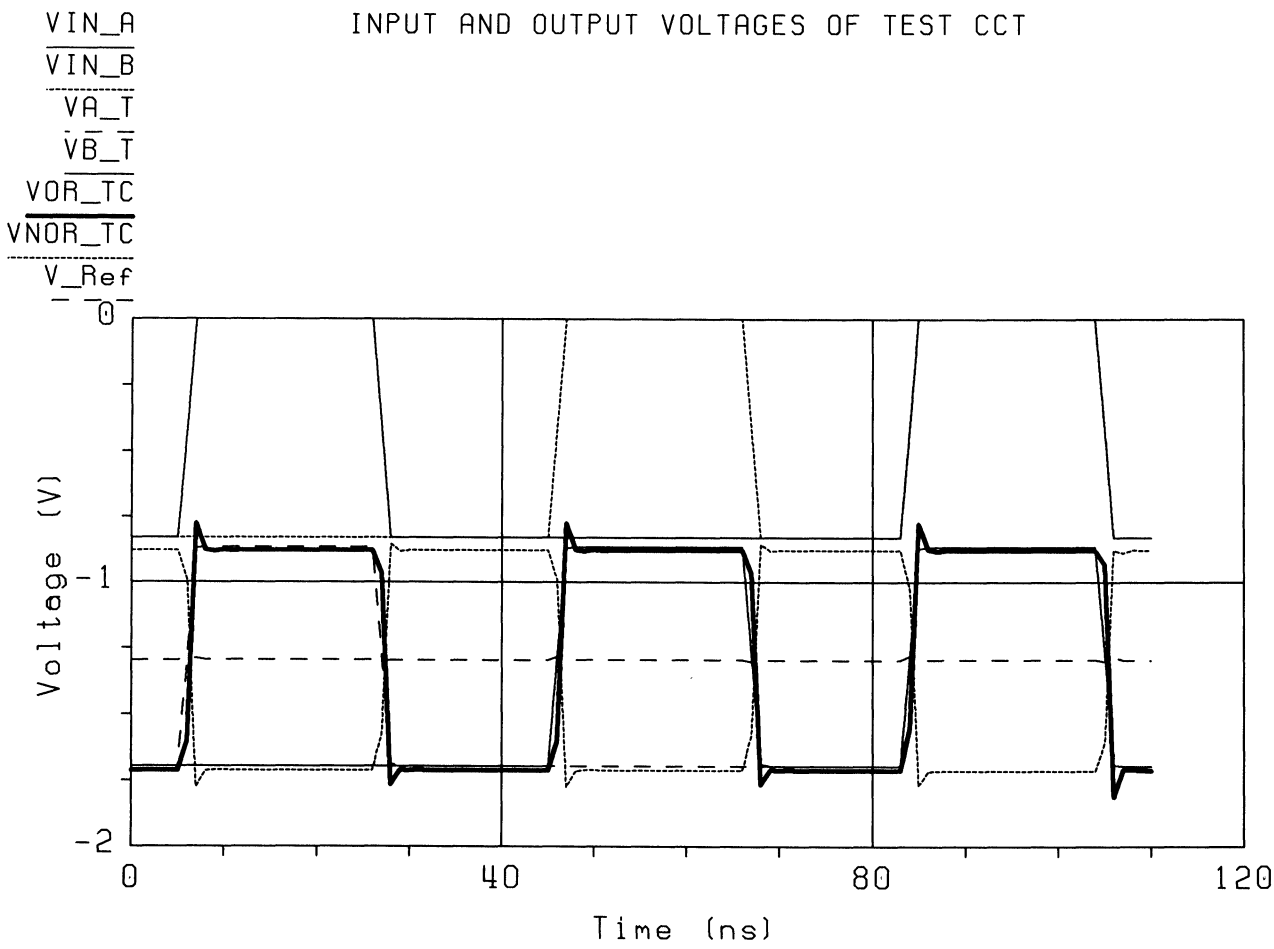

FIGURE 7 Operation of ECL OR/NOR gate with no defect.

input amplifier pair and the emitter follower output of the ECL gates.

Then, defects are injected into the test circuits one at a time. Any deviation from the fault-free logic behavior, or more than ±20% of the fault-free performance behavior, constitutes a fault. The total number of defects injected into the ECL OR/NOR gate is 61, as compared to 77 and 36 defects for equivalent BiCMOS and CMOS gates, respectively. For the ECL AND gate, the total number of defects is 70, compared to 77 for BiCMOS and 36 for CMOS NAND gates. The distribution of the defects for these gates is shown in Table III.

Effects of Defects in ECL AND and OR/NOR Gates

Shorts and/or opens in the devices of the CUTs in Figures 5 and 6 will result in improper current levels flowing through R1 and/or R2 (Figure 5) and R2 (Figure 6), hence producing improper signal levels at the outputs of the test circuits. Consider a defect of base-emitter short in device Q2 of Figure 6 (AND gate). This defect causes transistor Q2 not to conduct since input B is connected to both the base and emitter of the device. Also, transistors Q4, Q5 and Q6 are off regardless of the signal level at input A. There is no current flowing through R2 and thus, the output of the test circuit will be stuck-at-1. If the base or emitter of Q2 is open, the output of the CUT will be stuck-at-0 since current will always be directed through R2, Q6, Q4 and Q3. It is observed that the output of the CUT will be stuck-at-1 for faults of base-emitter short in devices Q1, Q2, Q3, Q4, Q7, Q10, opens in the base, collector and emitter of Q3, opens in the base of devices Q5, Q6, open in R1 and short in R2.

An open in the base of the transistor Q4 for instance, will cause the output of the CUT to follow the signal level of input A, thus producing an incorrect logic function. A base-collector short in devices

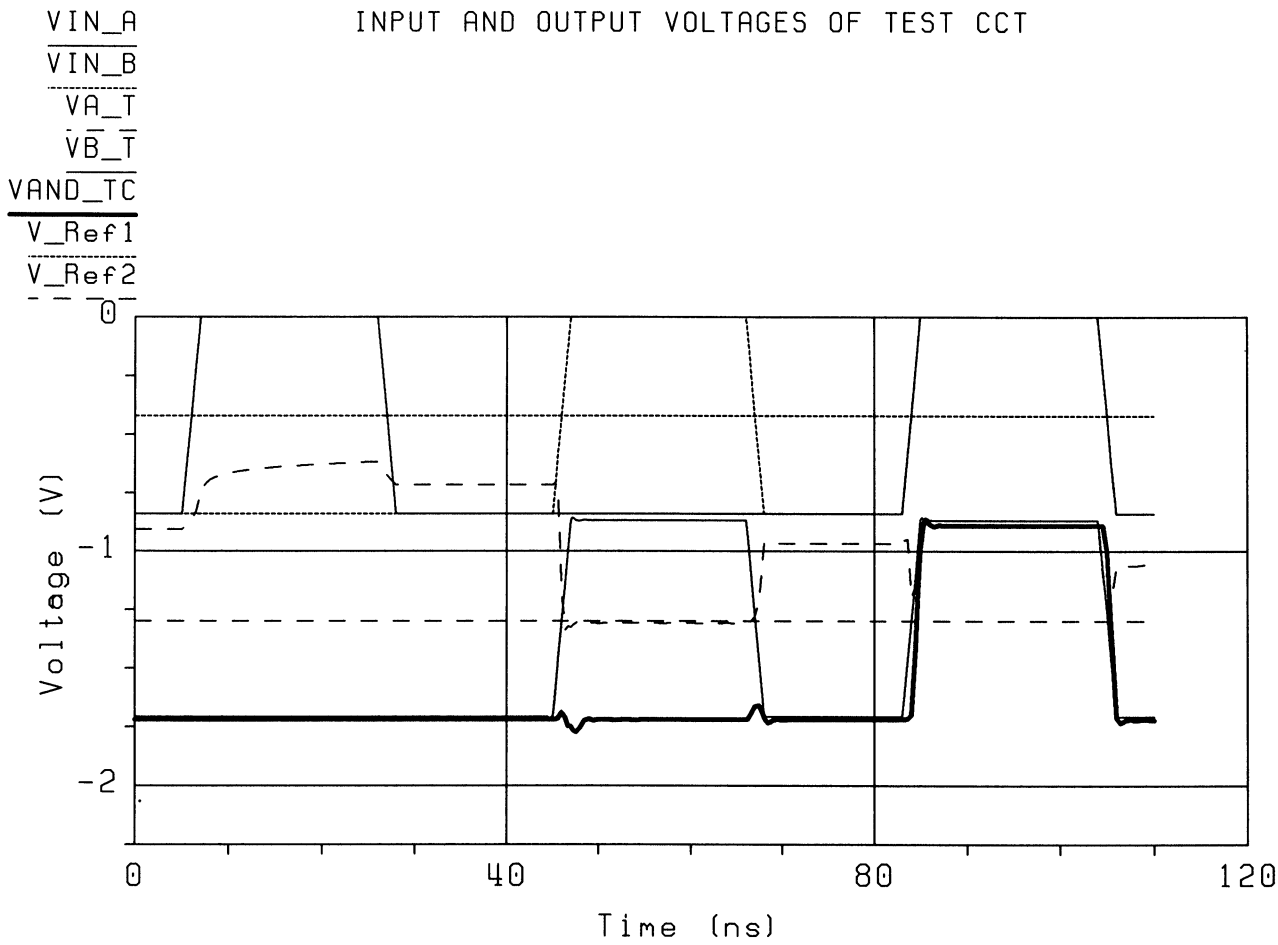

FIGURE 8 Operation of ECL AND gate with no defect.

Q5, Q6 (i.e. multiple emitter defect) causes the output to be stuck-at undefined (invalid) voltage level (neither a 0 or 1 logic level). All the above faults can be easily detected using regular logic tests. However, some of the faults cause errors which cannot be detected with the logic tests. For example, in the circuit of Figure 6, a base-collector short in transistor Q7 causes a very high increase in the current supplied to the CUT. Most of the collector-emitter pipe defects and opens/shorts in some of the devices cause the high output voltage level to be much lower or the low level to be much higher than expected. This would result in smaller signal swings, shift in delay and a lower noise immunity.

TABLE II
Set of specifications for ECL gates

Critical parameters	ECL OR/NOR	ECL AND
t_{PLH}	0.377 ns	0.538 ns
t_{PHL}	0.406 ns	0.442 ns
V_{IH}	−1.18 V	−1.18 V
V_{IL}	−1.41 V	−1.42 V
V_{OH}	−0.88 V	−0.88 V
V_{OL}	−1.77 V	−1.72 V
V_M	−1.295 V	−1.30 V
IDDmax	8.94 mA	8.44 mA
IDDQ	8.60 mA	7.53 mA
NMH	0.3 V	0.3 V
NML	0.3 V	0.3 V

TABLE III
Gate distribution of defects

Gate	Defects	
	Total	Shorts & opens
ECL OR/NOR	61	52
ECL AND	70	61
REF. VOLT. NETWORK	14	13
BiCMOS NOR	77	54
BiCMOS NAND	77	54
CMOS NOR	36	24
CMOS NAND	36	24

The amount of shift in delay could adversely affect the performance of the system. For example, if a gate output with this problem is used to clock several circuits, it could be devastating to the normal operation of the system. It is important to mention, however, that the reduced signal swing is being restored to the full swing as the signal passes through the following gates. As a result, the noise immunity level is restored to that of the fault-free case, and the effect of the defect is recovered. Thus, if only the final output of a system is monitored, there is a high possibility of not detecting these faults. The output of a system may be functionally error-free, but the actual sub-systems may have failed woefully. The defects which exist in the ECL OR/NOR gate (Figure 5) cause similar faults or output signal degradation as in the ECL AND gate.

Classes of Faults in ECL Circuits

The defect-generated faults have been classified into two groups as *logical* and *performance degradation faults*. The logical faults comprise of single stuck-at (SSA) 1, SSA-0, incorrect output logic functions and invalid signal levels. The logical faults are only combinational; sequential faults are not produced by the defects. This is in contrast to CMOS and BiCMOS circuits where the logical faults are both combinational and sequential in nature. Performance degradation faults are comprised of the following types: delay faults, VTC faults, IDD current faults or any combination of these faults. From the analysis of the results, the percentage distribution of the defects among the several fault sub-groups for the ECL AND gate is as follows: SSA-1 (31.4%), SSA-0 (32.9%), incorrect output logic function (15.7%), invalid signal level (1.4%), delay faults (24.3%), current faults (50%) and noise margin or VTC faults (15.7%). Similarly, for the ECL OR/NOR gate, the fault sub-groups are, SSA-1 (37.7%), SSA-0 (34.4%), incorrect output logic function (1.6%), invalid signal level (3.2%), delay faults (23%), current faults (66%) and VTC faults (30%). It is important to note that a single defect may cause multiple faults. For example, a defect may cause logical and current faults or VTC and delay faults, and so on.

Effects of Defects in the Voltage Reference Network

All the defects in the reference voltage network (14 defects) have three major effects on the reference voltage. They cause the reference voltage (V_{ref}) to increase or decrease above or below the nominal value and to produce invalid signal levels. For instance, a collector-emitter pipe in device QBB (Figure 5) causes V_{ref} to increase above -1.3 V. On the other hand, a short in D1 causes a decrease in V_{ref}. Open on R4 results to invalid reference signal level. The reference voltage network faults produce errors in the test circuits which fall within the two fault classes of ECL circuits discussed above. Also, the occurrence of some of the defects in the ECL gates can cause errors on the V_{ref}. For instance, an open between the Ground and R2 (Figure 5) transforms V_{ref} into series of pulses instead of a constant voltage level. These pulses occur mainly at the low to high level transition points of the input signals. In these cases, the faults produced by or induced on the reference voltage network can be detected by monitoring either the network's output or the final output of the ECL gates.

TESTABILITY ANALYSIS

In this section, we present the impacts of defects on ECL gates, using tables and bar charts. The testability analysis of the equivalent BiCMOS and CMOS gates has been reported by the authors in [7]. Where necessary, the results are presented for comparison with those of the ECL gates. The statistical information presented represents faults expressed as a percentage of the total number of defects simulated. Table IV depicts the distribution of the effects of the defects in the ECL OR/NOR, AND and reference voltage circuits. Also shown in the Table is how 30% and 16% of the total defects in the OR/NOR and AND gates respectively, cause a reduction in the signal swings at the output of the CUT. However,

TABLE IV
Distribution of effects of defects in ECL gates

Fault categ.	No. of faults		% of total faults	
	OR/NOR	AND	OR/NOR (61)	AND (70)
LOGICAL FAULTS	47	57	77	81
CURRENT FAULTS	40	35	65.6	50
DELAY FAULTS	14	17	22.9	24.3
VTC FAULTS	18	11	29.5	15.7
FAULTS RECOV. IN NEXT STAGE	18	11	29.5	15.7

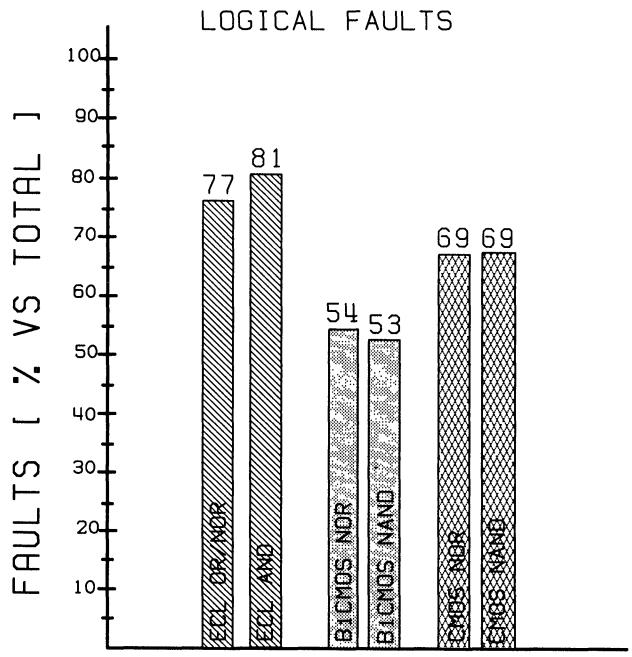

FIGURE 9 Spread of logical faults.

the full swings of the signals are restored in the stages following the CUT outputs. Thus, the effects of these faults are masked as the primary output signals of the CUT circuit propagate to subsequent load circuits.

Logical Faults

The logical faults analysis is shown in the bar chart of Figure 9. 77% of the total defects in the ECL OR/NOR gate cause logical faults while 81% for the AND gate cause logical faults. Also, as observed from the Figure, in the case of BiCMOS gates, the values are 54% for NOR and 53% for NAND. However, for CMOS gates, these numbers are 69% (NOR) and 69% (NAND). In the remainder of this section, the statistical numbers of the equivalent BiCMOS and CMOS gates will not be mentioned, but are shown on the corresponding tables and bar charts.

Current Faults

Current faults in the ECL circuits can be a decrease or increase in the fault-free steady-state (IDDQ) or transient current (IDDmax) values. From Table II, these values are respectively 8.60 mA (IDDQ) and 8.94 mA (IDDmax) for the ECL OR/NOR gate, 7.53 mA and 8.44 mA for the AND gate. It is important to mention that current faults in BiCMOS and CMOS circuits are only due to increase in the steady-state and transient values. The majority of current faults in the ECL circuits are a result of the steady-state current anomaly.

Figure 10 shows a typical simulation result corresponding to a current fault of Base-Collector Short (Q6) in the OR/NOR test circuit. In this illustration, the defect causes an increase in the IDDmax and IDDQ. The spread of the 40 defects (66% of total defects, see Table III) in the OR/NOR gate and 35 defects in the AND gate that cause current faults is shown in Figure 11. It is observed that a majority (47%) of the *total current faults* in the OR/NOR gate and 37% in the AND gate cause a decrease in current value between 20%–50% of the respective fault-free values. In the presence of defects the IDDQ current value varies respectively, from a minimum of 0.08 mA (OR/NOR) and 2.26 mA (AND) to a maximum of 251.9 mA (OR/NOR) and 217 mA (AND). The bar chart in Figure 12 depicts the percentage of the current faults versus the total faults. For ECL gates, the values are 66% for the OR/NOR and 50% for the AND.

Delay Faults

A decrease or increase in the fault-free nominal delay value constitutes a delay fault. Figure 13 depicts the response of a delay fault resulting from a collector-emitter pipe defect (Q3) in the AND test circuit. The spread of the ECL gates *total delay faults* (14 and 17 defects, respectively) is shown in Figure 14. The chart indicates that 58% of the delay faults in the OR/NOR gate leads to increase in delay of more than 100% of the nominal value. For the AND gate, 41% of the delay faults causes an increase in delay of more than 100%. However, none of the delay causing defects produces a decrease in delay below 100% of the nominal value. Figure 15 depicts the percentage of delay faults out of the total defects. In the case of ECL OR/NOR gate, the value is 23% compared to 24% for the AND gate. The ECL circuits are less sensitive to defects causing delay faults.

VTC Faults

The VTC faults are those that affect the noise margins of the circuit. Figure 16 shows a typical VTC response of the ECL AND gate with no defects. On the other hand, Figure 17 illustrates a VTC fault resulting from a collector-emitter pipe defect (Q1)

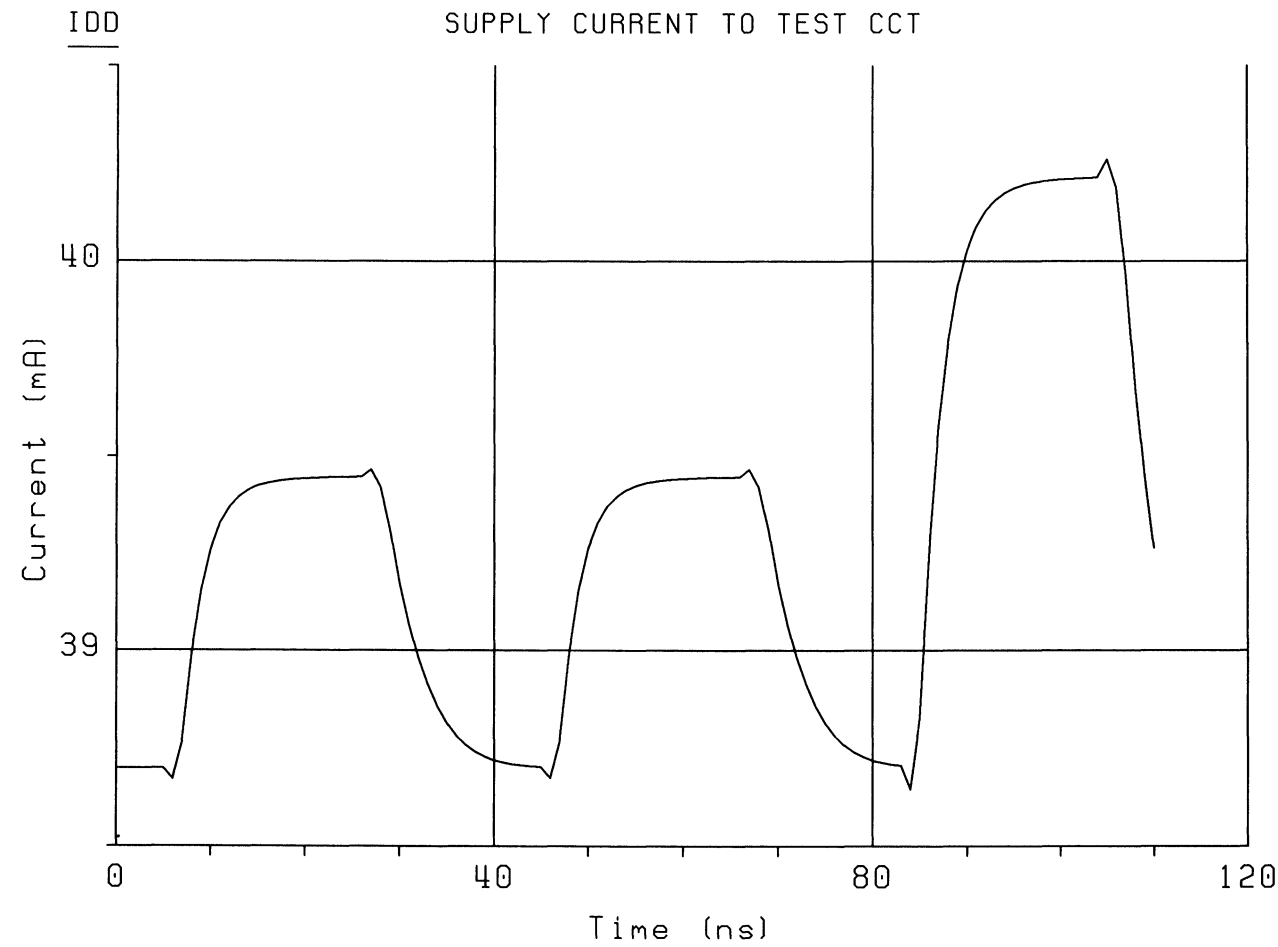

FIGURE 10 ECL OR/NOR gate with current fault.

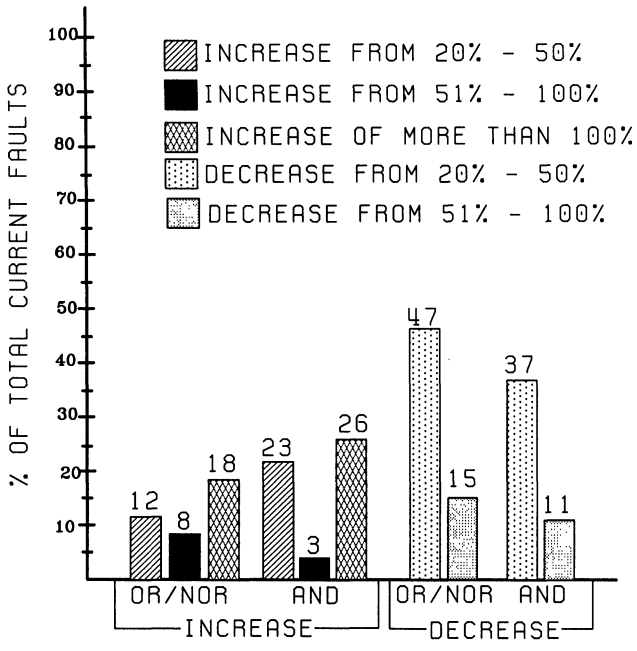

FIGURE 11 Spread of total current faults among different current ranges.

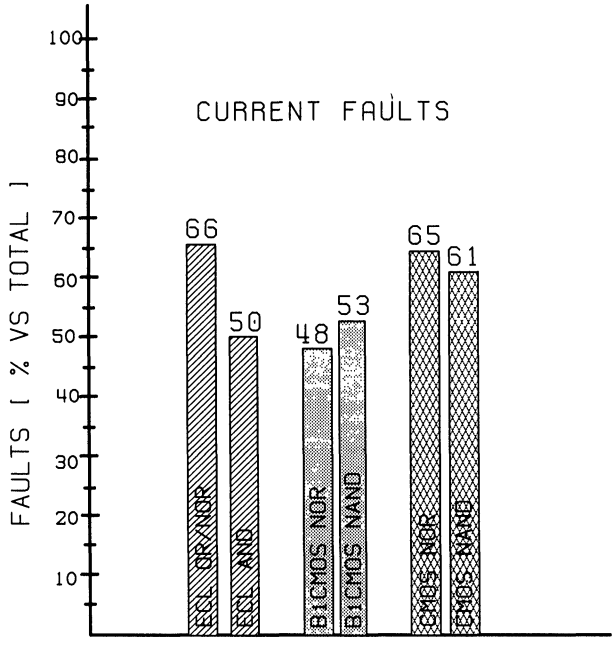

FIGURE 12 Spread of current faults.

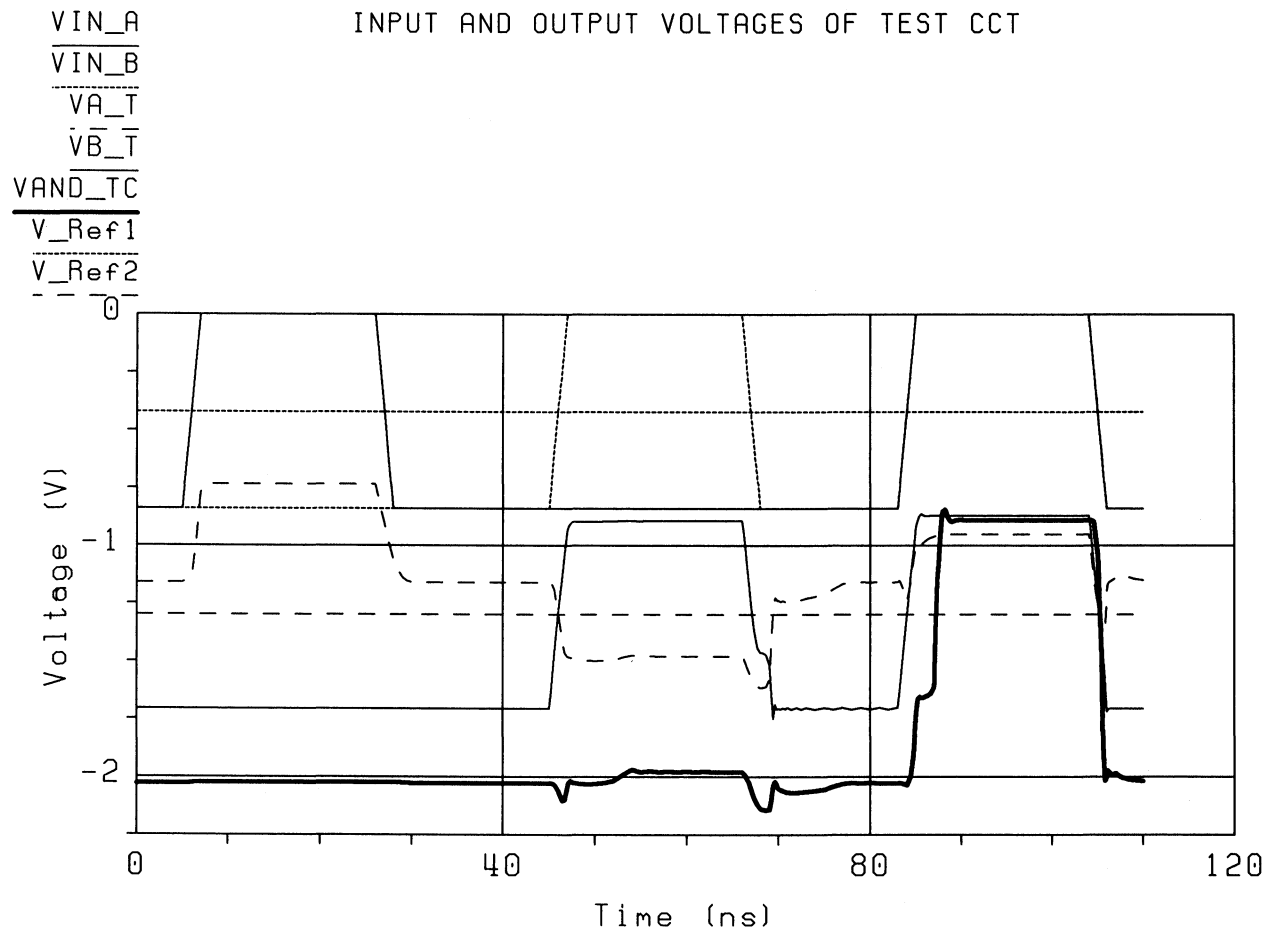

FIGURE 13 ECL AND gate with delay fault.

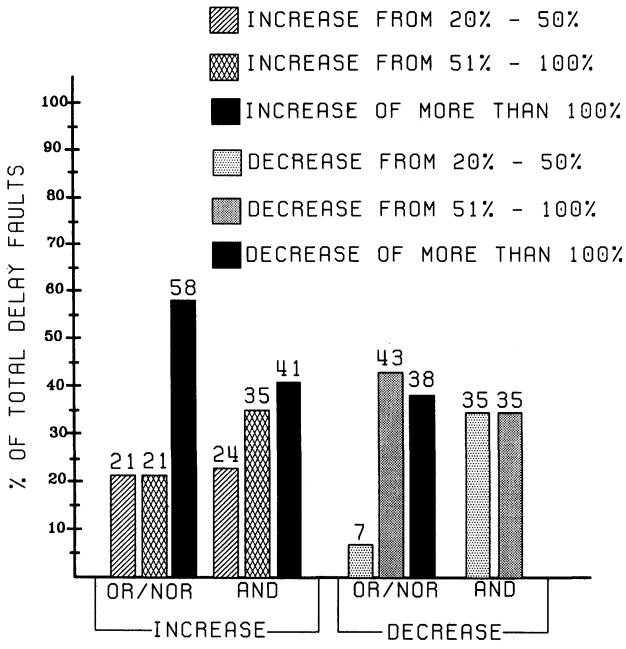

FIGURE 14 Spread of total delay faults among different delay ranges.

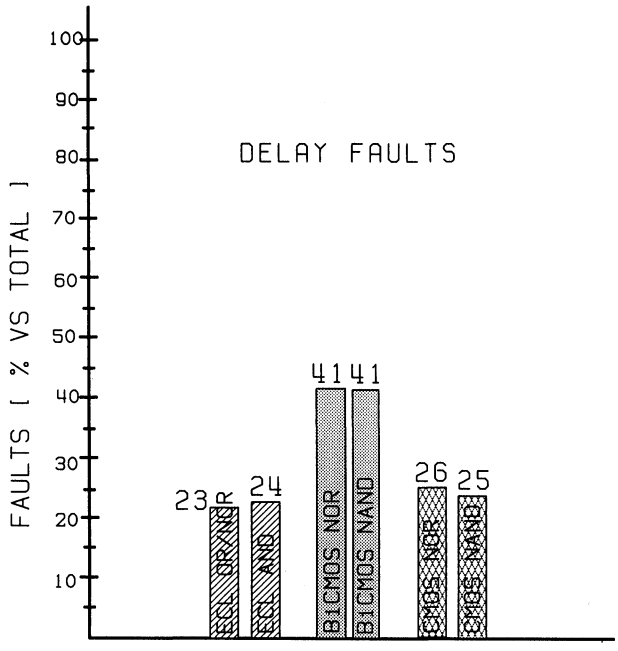

FIGURE 15 Spread of delay faults.

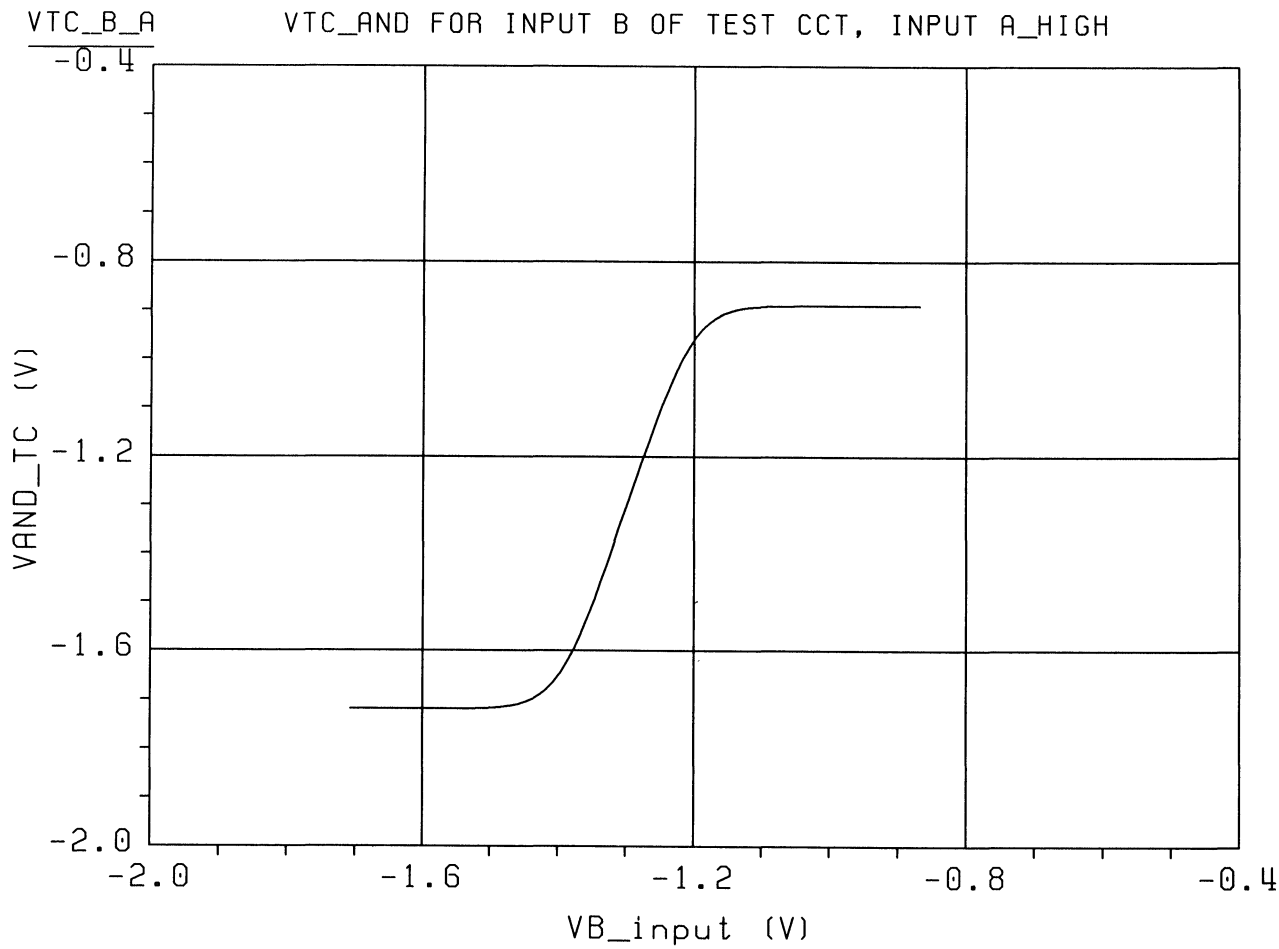

FIGURE 16 ECL AND gate with no VTC fault.

in the AND test circuit. The responses at the outputs of the CUT and the load circuit type II corresponding to this fault are shown in Figure 18. A smaller signal swing is produced at the output of the CUT due to the defect. This results in lower noise immunity. However, the full signal swing is restored as the signal propagates to the output of load circuit type II. This example illustrates the case where the effects of the defect are recovered in the stages following the CUT outputs.

VTC faults account for 30% and 16% of the total faults in ECL OR/NOR and AND gates respectively. The spread of the *total VTC faults* in the ECL gate, among the different ranges of noise margin is illustrated in Figure 19. It is observed that 61% and 36% of the total VTC faults in the OR/NOR and AND gates respectively result to decrease the noise margin between 20% to 50% of the nominal values. However, 39% and 64% of the total VTC faults in the respective gates, lead to decrease in noise margin between 51% to 100%. The majority of the VTC faults in the ECL gates results in low-level noise margin (NML) anomaly. The effects of VTC faults on noise margins of the defective gates, are summarized in Table V.

FAULT COVERAGE ANALYSIS

The statistical results show that using the logic fault model leads to a fault coverage of 79% of the total faults in all the ECL gates, 54% for BiCMOS and 69% for CMOS equivalent circuits. In the case of current faults, the percentages of total faults that can be detected in ECL, BiCMOS and CMOS gates are 57%, 48% and 65% respectively. Using the delay fault model, coverages are 24% (ECL), 41% (BiCMOS) and 26% (CMOS). The adoption of the VTC fault model yields a coverage of 22% for ECL, 16% for BiCMOS and 17% for CMOS circuits. From the analysis, it is apparent that the detection of faults

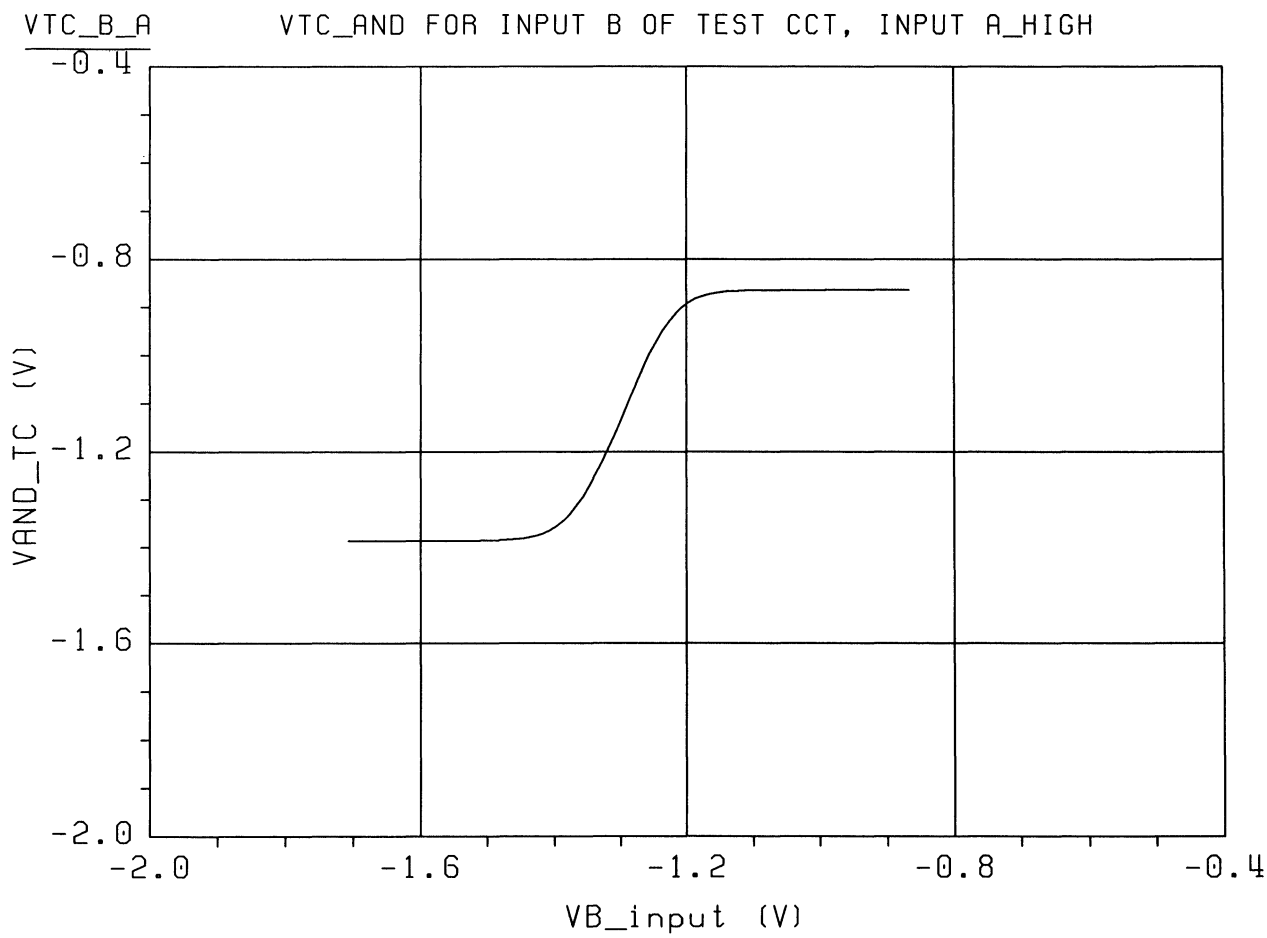

FIGURE 17 ECL AND gate with VTC fault.

by using only one fault model is inadequate to obtain high fault coverage in the ECL as well as BiCMOS and CMOS circuits.

In order to improve the testability of ECL gates, it is necessary to merge the different fault models. The bar chart of Figure 20 compares the percentage of detection for a combination of fault models of ECL, BiCMOS and CMOS equivalent gates. It is observed that, by combining the logical fault model with the delay model, the fault coverage can reach 95% for both ECL, BiCMOS and CMOS circuits. However, when the logical fault model is merged with the current fault model, the coverage goes to 92% for ECL, 70% for BiCMOS and 93% for CMOS. The merging of logical fault model with the VTC fault model leads to a coverage of 98% for ECL, 60% for BiCMOS and 72% for CMOS circuits.

It is important to note that merging the logical, current and delay fault models or the logical, current and VTC fault models or logical, delay and VTC fault models will lead to a fault coverage of 96%, 98% and 100% respectively, in ECL gates. The use of these approaches requires the detection of three fault categories with only slight increase in fault coverage, in contrast to when only two fault models are merged. It would be ideal to be able to monitor all the gates for current faults, but this is not possible with the high densities of today's VLSI circuits. Since ECL gates consume large DC currents, due to the normal parametric fluctuations and mismatch in transistors and resistors, it might be difficult to detect current faults in the VLSI circuit, unless every gate is monitored individually. As a result of this, approaches of detecting a combination of logical and delay or logical and VTC fault models are considered for ECL gates.

From the analysis of the results, it is found that the approach of combining the logical and VTC fault models would be more effective for ECL circuits. However, the combination of logical and delay fault

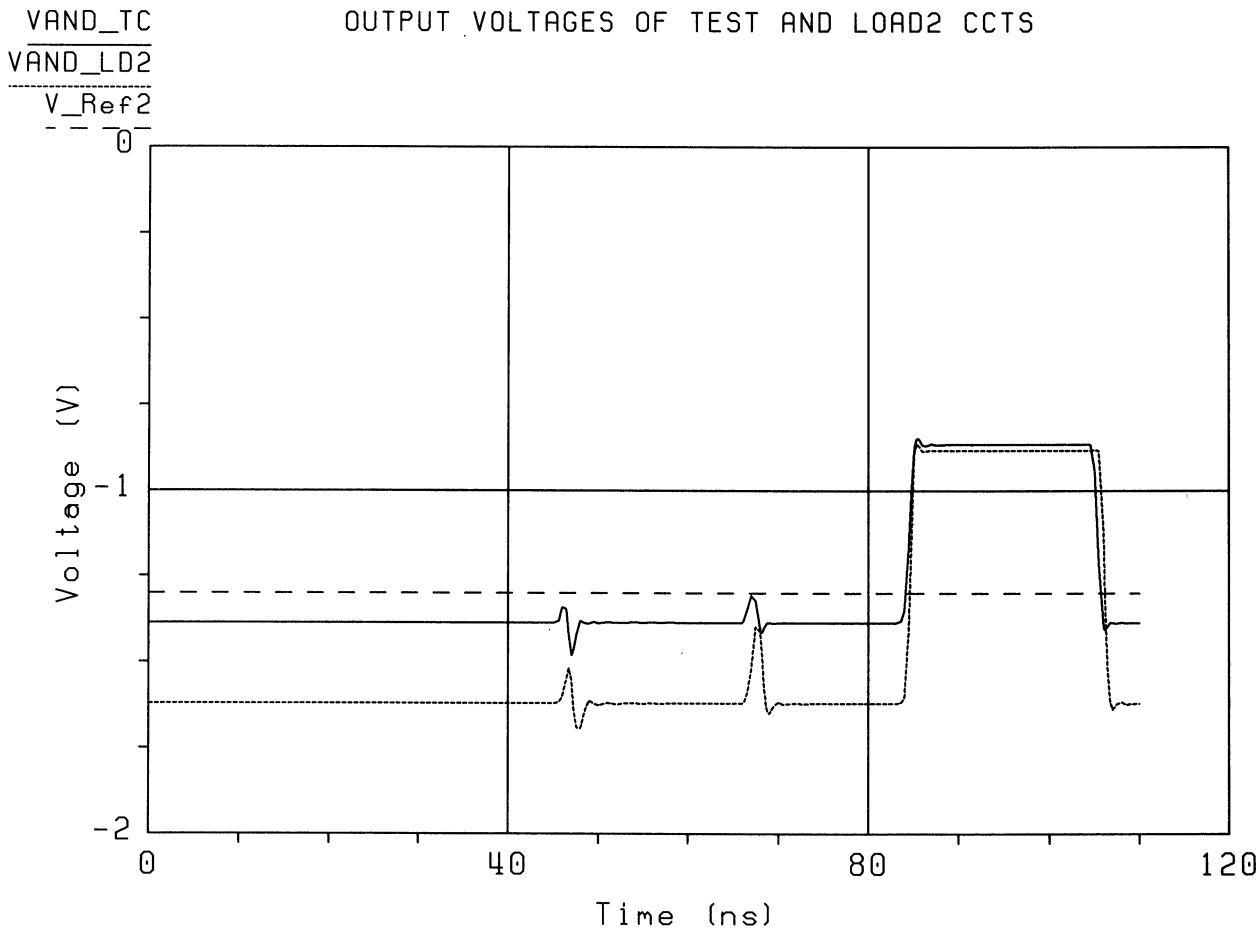

FIGURE 18 Output response of the CUT and Load type II circuits in the presence of the VTC fault.

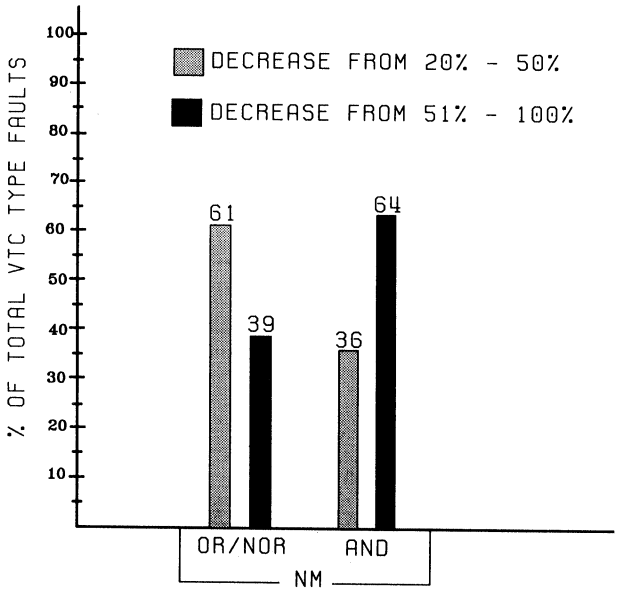

FIGURE 19 Spread of the VTC faults among noise margin ranges.

models approach is more effective for BiCMOS and CMOS equivalent gates. An approach to detect VTC type faults has been reported in [6]. The method attempts to stress the entire circuit just enough so that any marginal signals are sufficiently degraded to

TABLE V
Gate distribution of noise margins

	Noise margin parameters			
	No defect		Range with defects	
Gate	NML	NMH	NML	NMH
ECL OR/NOR	0.30	0.30	0.01–1.28	0.08–0.67
ECL AND	0.30	0.30	0.01–0.61	0.09–0.43
BiCMOS NOR	1.9	2.0	0.5–2.5	0.6–2.6
BiCMOS NAND	1.8	2.0	0.1–2.3	0.7–3.9
CMOS NOR	2.3	2.7	0.0–3.5	0.2–4.1
CMOS NAND	2.3	2.6	0.2–3.6	0.6–3.7

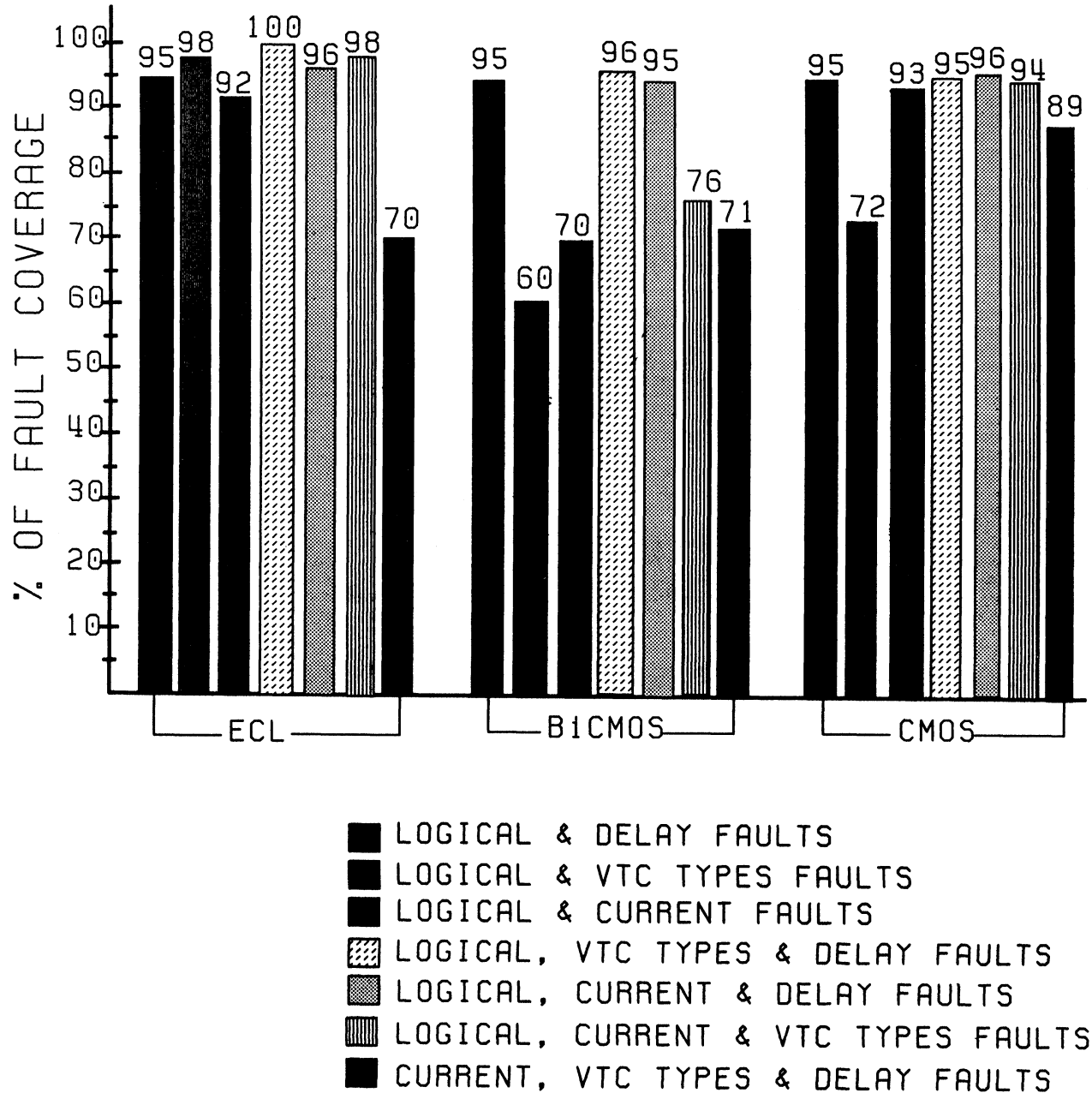

FIGURE 20 Comparison of all fault models coverage.

cause logic errors. The logic gates are respectively stressed by applying a DC offset which results in a shifted output signal. Stressing a faulty signal degrades it to the point of not being recoverable by the following gates. This is then detected on the final gate as a logic error. This technique, however, requires about 20% silicon area overhead since test control circuitry is augmented into every gate in the ECL circuit. Therefore, using any robust logic test and VTC test techniques, a high percentage (98%) of the faults in the ECL circuits can be detected.

CONCLUSION

The testability analysis of ECL gates has been investigated. Appropriate defect models have been selected and used to study the effects of defects on the ECL gates. Similar studies done on the equivalent BiCMOS and CMOS gates are used for the basis of comparison. The results show that logical fault model is inadequate for obtaining sufficiently high fault coverage in ECL, BiCMOS and CMOS gates. By combining the logical and VTC fault models, higher fault

coverage (98%) is achieved for ECL gates. In BiCMOS and CMOS equivalent gates, the merging of logical and delay fault models provides high coverage of about 95%. Therefore, these fault models together with adequate stimulation/detection methods, are required to improve the testability of ECL, BiCMOS and CMOS circuits.

APPENDIX

```
.MODEL QN NPN
+IS=4E-17A BF=100 NF=1 Tf=20E-12
IKF=8E-3 BR=8 TR=400E-12 IKR=80E-3
+RB=50ohms RE=3.75ohms RC=37.5ohms
ITF=40E-3 VTF=3 XTF=100 +CJC=80E-15
MJC=0.5 CJE = 60E-15 MJE=0.5
CJS=320E-15 MJS=0.5

.MODEL MP PMOS LEVEL=2 VTO= -0.8
+PB=1.04 CGSO=350P CGDO=350P RSH=50
CJ=330U CJSW=300P MJ=0.5 MJSW=0.5
+TOX=250E-10 NSUB=5E+16 NFS=0E+11
TPG=1 XJ=0.02U LD=0.15U +UO=250
VMAX=37.2K UEXP=0.0311 UCRIT=4.72K
DELTA=0.817 NEFF=2

.MODEL MN NMOS LEVEL=2 VTO=0.8
+PB=0.45 CGSO=350P CGDO=350P RSH=40
CJ=330U CJSW=300P MJ=0.5 MJSW=0.5
+TOX=250E-10 NSUB=1E+16 NFS=0E+11
TPG=1 XJ=0.04U LD=0.15U +UO=500
VMAX=37.9K UEXP=0.0129 UCRIT=1K
DELTA=1.64 NEFF=0.45

.MODEL MR750 D IS=3.29P RS=1.3M N=1.01
CJO=0.379N VJ=0.484 M=0.4 BV=60
IBV=0.2
```

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Biographies

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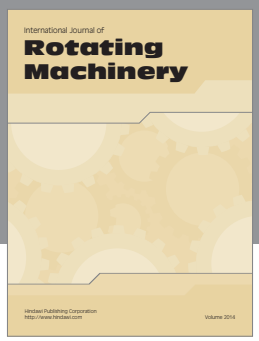

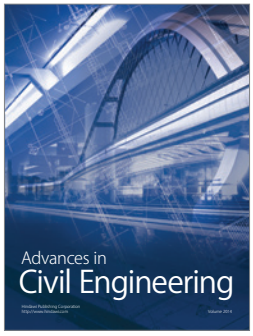

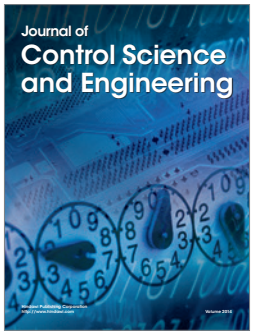

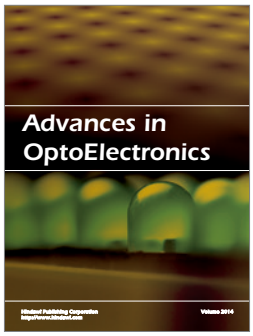

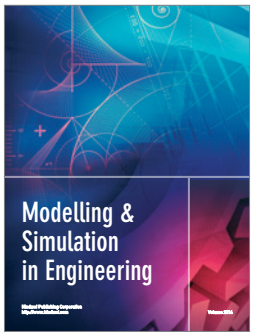

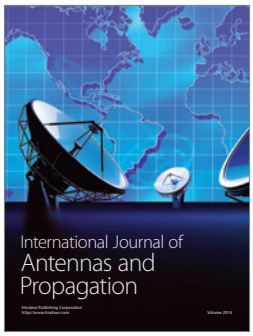

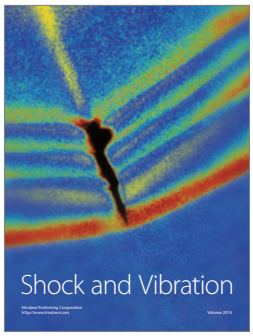

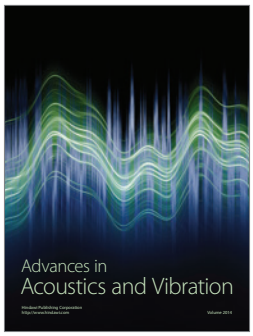

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