VLSI Design
1994, Vol. 2, No. 3, pp. 223–231
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A Quadratic Programming Approach to Estimating the Testability and Random or Deterministic Coverage of a VLSI Circuit

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(Received September 29, 1992, Revised March 9, 1993)

The testability distribution of a VLSI circuit is modeled as a series of step functions over the interval [0, 1]. The model generalizes previous related work on testability. Unlike previous work, however, we include estimates of testability by random vectors. Quadratic programming methods are used to estimate the parameters of the testability distribution from fault coverage data (random and deterministic) on a sample of faults. The estimated testability is then used to predict the random and deterministic fault coverage distributions *without* the need to employ test generation or fault simulations. The prediction of fault coverage distribution can answer important questions about the "goodness" of a design from a testing point of view. Experimental results are given on the large ISCAS-85 and ISCAS-89 circuits.

Key Words: *Detection probability, Fault coverage, Fault simulation, Quadratic programming, Testability profile*

1 INTRODUCTION

The problem of test generation for a VLSI circuit is to find a set of inputs that detect the presence of a desired fraction of modeled faults. The process of finding such a set can be summarized as follows:

- Create a fault list from the circuit descriptions; initialize the test set to empty.
- While coverage of test set is less than desired coverage do
    1. Select a target fault, f, and generate a test, t, for f using random or deterministic test generation procedures [10]; add t to the test set if needed.
    2. Simulate the generated test on the remaining faults [2] and update the fault list by removing faults detected by the generated test

Steps (1) and (2) above dominate the overall costs of the test generation process. Here, the costs are measured in terms of the CPU time and memory space requirements. The simulation costs are nonlinear in the size of the fault list [11]. In a previous paper [1], the above test generation process was restricted to a sample of faults. By employing a relationship between testability and fault coverage, tests generated on a sample of faults were used to *estimate* the population coverage without the need to use full fault simulation. Thus, major savings in the overall costs of fault simulation were obtained. Figure 1 shows a flow chart of the process of test generation by fault sampling.

The model used in estimating the testability profile is of great importance since the estimated testability is used to predict the population fault coverage and the sample size for pass two (if needed). In previous work the testability profile was modeled as a beta distribution [7]. The advantage of such a distribution is in the flexibility of the *beta* model (from a statistics point of view the beta model represents the most flexible and tractable two parameter model). The testability distribution of *real* circuits, however, is a mixture of step functions over the interval [0, 1] (this is due to the finiteness of fault populations). In addition in previous work, deterministic input vectors were used to estimate the parameters of testability. The testability profile is a function of the detection probabilities of faults in the circuit. The detection

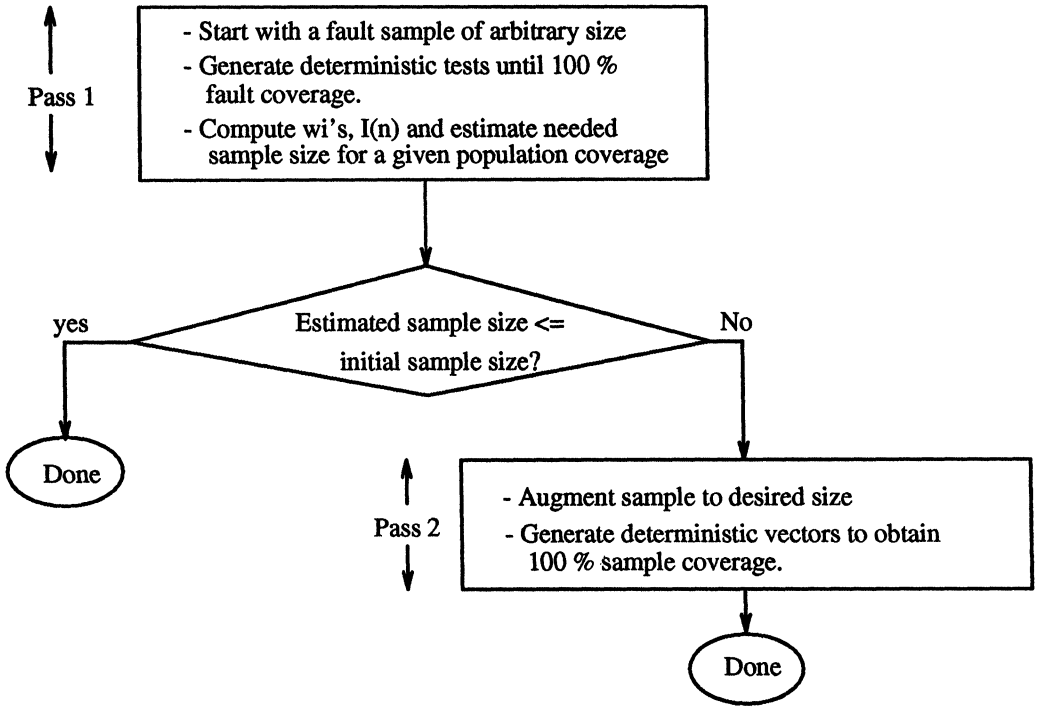

FIGURE 1 Test generation by fault sampling.

probability of a fault, however, is a function of the input distribution used. For example, when deterministic test generators are used to generate the input tests, the input vectors can be considered "random" from some unknown distribution. For this type of input distribution target faults have a detection probability equal to one (assuming no fault is redundant and no time limits are imposed on the deterministic test generator). As a result the testability profile distribution of deterministic vectors is usually more skewed to the right than that of random vectors taken from a uniform distribution.

The main contribution of this paper is: 1) adopting a general model and estimating its parameters (this results in a new procedure of estimating the testability profile of a circuit that is different from existing procedures [3, 13, 14]), and 2) estimating the random and deterministic coverage distributions of a set of vectors *without* the need to employ expensive means of full fault simulation.

The testability profile is modeled as a series of step functions over the interval [0, 1]. In addition, in order to account for redundant faults, the model includes an impulse function located at zero.

In estimating the testability distribution we use deterministic and random vectors. For both cases, the test generation process is carried over a random sample of faults. Deterministic and random tests are generated and simulated on the sample of faults (without fault dropping). The testability parameters are estimated from the detection counts collected on the sampled faults. From the estimated parameters, the random and deterministic coverage distributions are estimated without the need to employ the random or deterministic test generation process.

The paper is organized as follows. In Section 2 the needed definitions and the testability model are given. Section 3 contains a quadratic programming approach to estimating the testability parameters. Section 4 includes experimental results on three of the large ISCAS-85 circuits for the random coverage case and three of the large ISCAS-89 circuits for the deterministic coverage case. The conclusions are given in section 5.

2 BACKGROUND AND THE TESTABILITY MODEL

Definitions and Background. The *detection probability* of a fault, α, is the probability of detecting α by a random vector. Note that the detection probability of a fault is affected by the distribution from which the random inputs are selected. For example, when deterministic test generators are used to generate the tests, the input vectors can be considered

"random" from some *unknown* distribution. For this type of input distribution, target faults have a detection probability equal to one (assuming no fault is redundant and no time limits are imposed on the deterministic test generator).

The *detection probability distribution* (*testability profile*), $p(t)$, is the probability density function of the detection probabilities of faults. The term $p(t)dt$ corresponds to the fraction of faults with detection probability in $[t, t + dt]$.

The *fault coverage* by n vectors, y_n, is the fraction of faults detected by the n vectors. The set of vectors can be generated *randomly* or *deterministically*.

For random test generation, the method of obtaining the test vectors is a function of the probability of choosing a zero or a one at each input. We choose a uniform distribution. That is, the probability of applying a zero at any input is the same as the probability of applying a one. From [15], the random coverage by n vectors is $y_n = 1 - \int_0^1 (1 - x)^n p(x)dx = 1 - I(n)$. We call the term $I(n)$ the undetectability profile.

Deterministic test generation is accomplished by employing deterministic test generation procedures. For a given (target) fault, the test procedure selects a test for the fault by searching the input space. Thus, deterministic test vectors are assumed to detect at least one new fault not detected by other previously generated tests. In addition, the deterministic test (generated) is assumed to act as a random vector on the non-target faults. The distribution of the input space is unknown, however. From [15], the deterministic coverage by n vectors can be found as $y_n = 1 - I(n) + n/Y\,[1 + I(n) - \int_0^1 1 - (1 - x)^n/nx\, p(x)dx]$, where Y is the fault population size. For large n with $n << Y$, this coverage can be estimated by $y_n \approx 1 - I(n) + n/Y$. The approximation has an intuitive interpretation. The n/Y term is the contribution of the n deterministic vectors to coverage. The remaining term $(1 - I(n))$ is the random coverage contribution of deterministic vectors on non-targeted faults.

The Testability Model. The testability profile distribution of actual VLSI circuits is a mixture of discrete step functions. Figure 2 shows the actual testability distribution of the ISCAS-85 C432 circuit.

In accordance with actual distributions of the testability profile, we choose the following general testability model.

$$p(t) = \begin{cases} a_1\delta(t), & \\ a_2, & t_1 = 0 < t \le t_2, \\ a_3, & t_2 < t \le t_3, \\ \vdots & \vdots \\ a_k, & t_{k-1} < t \le t_k = 1 \end{cases} \tag{1}$$

where $\delta(t)$ is the Dirac delta function, $a_1 + a_2(t_2 - t_1) + \cdots + a_k(t_k - t_{k-1}) = 1$, and $a_i \ge 0$, $i = 1, 2, \ldots, k$. The model includes an impulse function at zero to account for the contribution of redundant faults (redundant faults have detection probability equal to zero).

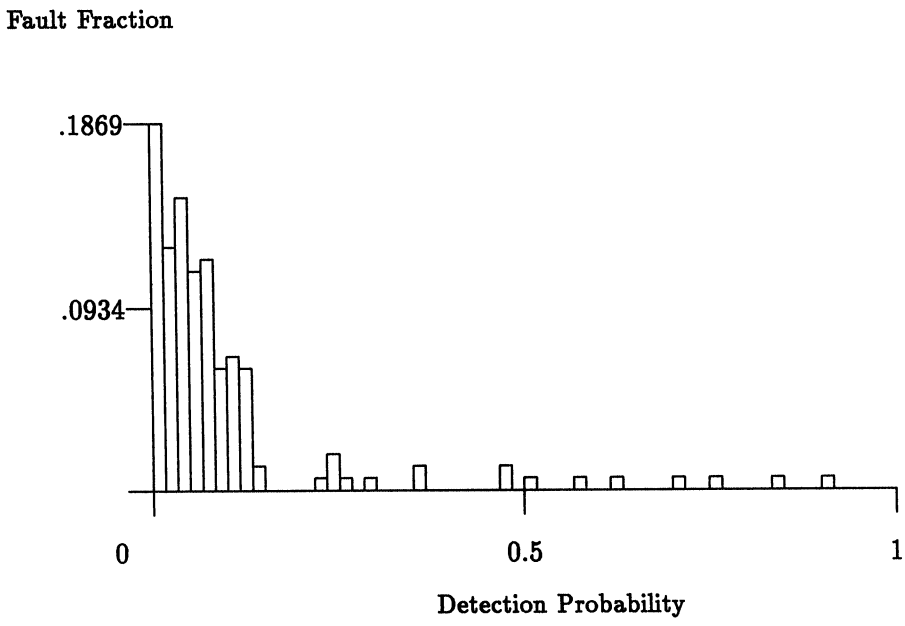

FIGURE 2 Actual testability distribution of ISCAS-85 C432 circuit.

A knowledge of the a_i parameters, $i = 1, 2, \ldots, k$, can be used to estimate the coverage distribution by n vectors. For deterministic coverage, the estimated coverage using the above model is evaluated to

$$y_n \approx 1 - \left[a_1 + \sum_{i=1}^{k-1} \int_{t_i}^{t_{i+1}} ((1-t)^n \cdot a_{i+1})dt\right] + \frac{n}{Y}$$

$$= 1 + \frac{n}{Y} - a_1 - \frac{1}{n+1}\left[\sum_{i=1}^{k-1} ((1-t_i)^{n+1} - (1-t_{i+1})^{n+1})\, a_{i+1}\right] \quad (2)$$

Similarly, for random vectors we obtain

$$y_n = 1 - a_1 - \frac{1}{n+1}\left[\sum_{i=1}^{k-1} ((1-t_i)^{n+1} - (1-t_{i+1})^{n+1})\, a_{i+1}\right] \quad (3)$$

In the next section we present a method of estimating these parameters by applying the test generation process to a random sample of faults.

3 PARAMETER ESTIMATION

The statistical frame work. Assume that a random sample of n_s faults is drawn from the fault population of a given circuit. Let Y denote the fault population size. Let t_i denote the actual detection probability of the ith sampled fault, $i = 1, \ldots, n_s$. Note that t_i equals the fraction of the input space that will detect the ith fault and that such a t_i is not known.

For $n_s << Y$, one may assume that $t_1, \ldots, t_{n_s}$ constitutes a random sample of faults from a population of faults with detection probability distribution $p(t)$, $0 \le t \le 1$. Assume N random input vectors are applied to each of the n_s faults. Let $X_1, \ldots, X_{n_s}$ denote the number of times (out of N) faults $1, \ldots, n_s$ are detected, respectively. The conditional distribution of X_i given t_i is binomial with N trials and success parameter t_i. That is

$$P(X_i = x|t_i) = \binom{N}{x} t_i^x (1-t_i)^{N-x}$$

The unconditional distribution of X_i is a mixture of binomials with probability distribution function given by

$$P[X_j = x] = \int_0^1 \binom{N}{x} t^x (1-t)^{N-x} p(t)dt, \quad (4)$$

where $x = 0, \ldots, N$, and $j = 1, \ldots, n_s$. From (4), the probability that fault f_j is detected $i-1$ times is given as

$$P[X_j = i-1] = \int_0^1 \binom{N}{i-1} t^{i-1}(1-t)^{N-i+1} p(t)dt$$

$$= a_1 + \sum_{l=2}^{k-1} a_l \int_{t_l}^{t_{l+1}} \binom{N}{i-1} t^{i-1}(1-t)^{N-i+1}dt, \quad (5)$$

where $i \ge 1$. Equation (5) was obtained from the testability model of $p(t)$ as given in (1) and can be written as

$$P[X_j = i-1] = a_1 + \sum_{l=2}^{k-1} e_{il}a_l, \quad i = 1$$

$$= \sum_{l=2}^{k} e_{il}a_l, \quad i = 2, \ldots, N,$$

where

$$e_{il} = \int_{t_{l-1}}^{t_l} \binom{N}{i-1} t^{i-1}(1-t)^{N-i+1}dt,$$

$$l = 2, \ldots, k. \quad (6)$$

This can be written as

$$P[X_j = i-1] = \sum_{l=1}^{k} e_{il}a_l, \quad i = 1, \ldots, N,$$

where

$$e_{11} = 1 \text{ and } e_{i1} = 0 \text{ for all } i \ge 2$$

Computing the parameters of testability. Let W_i equal the number of X_j's which are equal to i, $i = 0, 1, \ldots, N$. That is W_i is the number of faults in the sample that are detected i out of N times. Then $P[X_j = i-1]$ is approximated by W_{i-1}/n_s, $i = 1, \ldots, N$. Based on the unconditional distribution of each X_i ($i = 0, \ldots, n_s$), the testability parameters can be estimated using the method of least squares. To do this we need to minimize

$$D = \sum_{i=1}^{N} \left[\sum_{l=1}^{k} e_{il}a_l - p_i\right]^2$$

where

$$p_i = \frac{W_{i-1}}{n_s}, \quad i = 1, \ldots, N,$$

subject to the constraints $\int_0^1 p(t)dt = 1$ and $a_i \geq 0$ for $i = 1, 2, \ldots, k$. It is well-known that least squares problems can be solved by quadratic programming methods. Here, we show how this method apply to the problem of estimating the testability parameters. Let E, P and A be $N \times k$, $N \times 1$ and $k \times 1$ matrices with entries e_{ij}, p_i and a_i, respectively. Define the matrix, C, as

$$C = EA - P = [c_{ij}].$$

Note that the matrix, C, is an $N \times 1$ matrix where

$$c_{i1} = \sum_{l=1}^{k} e_{il}a_l - p_i.$$

Note also,

$$D = C^TC = (EA - P)^T(EA - P).$$

Multiplying the above matrix equation for D and simplifying we get,

$$D = A^THA + 2GA \tag{7}$$

where H is the $k \times k$ matrix E^TE and G is the $k \times 1$ matrix with $G = -E^TP$. From this and the previous constraints, we obtain

$$\begin{cases} \textit{minimize} & D = 2GA + A^THA \\ \textit{Subject to} & a_1 + a_2(t_2 - t_1) \\ & \quad + \cdots + a_k(t_k - t_{k-1}) = 1, \\ & a_i \geq 0, \quad i = 1, \ldots, k. \end{cases}$$

The above is a quadratic programming problem with H a positive definite symmetric matrix. A solution to this problem will yield the proper a_i values in A. These values can then be used to estimate the coverage distribution from the testability and coverage relationship. In order to solve this problem, however, we need to determine the values of the constant matrices G and H. In addition, the $t_i - t_{i+1}$ terms needed to be known. For these, we choose equally spaced step functions over the interval [0, 1]. That is,

$$t_i = \frac{i - 1}{k - 1}, \quad i = 1, \ldots, k.$$

Matrix H can be computed from knowledge of E. Each of the e_{ij} in (8), and hence E and H, can be computed by employing the IMSL routines DBINPR and DBETDF. Similarly, Matrix G is computed from knowledge P and E.

4 EXPERIMENTAL RESULTS

We carried the proposed method of computing the testability profile and estimating coverage data using random and deterministic test generation.

Random test generation. For random test generation the proposed method was applied to three of the large ISCAS-85 circuits, C2670, C6288, and C7552 [3]; C2670 was chosen due to its resistance to random testing. For each of the circuits a random sample of 1000 faults was selected. On the sample of faults random patterns were generated and simulated using a deductive fault simulator [2]. Unlike test generation procedures, however, each fault was simulated for each of the generated patterns and a count was recorded of the number of times each fault was detected. On each sample, patterns were generated while noticeable changes in sample coverage were observed. For both, C2670 and C7552, minor changes in the sample coverage occurred on random patterns exceeding 200 vectors. For these circuits we chose 300 random patterns. Similarly, for the C6288 circuit minor changes in sample coverage occurred for random patterns exceeding 50 vectors. For this circuit, we chose 100 patterns. The X_i and W_i counts obtained from the sample of faults were then used to estimate the random testability profile using the IMSL routine "DQPROG." The number of parameters used in the testability model was 50 for each of the circuits.

The estimated testability profile was then used to estimate the random coverage distribution of the three circuits without generating actual random tests. To do this we used the equation for random coverage, $y_n = 1 - \int_0^1 (1 - x)^n p(x)dx$. The expected random coverage was computed for each circuit for 5000 random vectors. In a separate run, we computed the actual random coverage for each circuit for the same number of vectors. Figure 3, shows the expected and actual coverage curves for the C2670 and C7552 circuits, respectively. Table 1, includes the initial coverage data (estimated and actual) for the three circuits. As can be seen from the table, initial estimates of coverage do not agree with actual ones. This is due to the fact that coverage by the first random vector can vary by up to 20% in some of the circuits

TABLE I
Initial Estimated and Actual Coverage Data

Circuit	Vector	Actual Coverage	Estimated Coverage
C2670	1	17.946	27.341
	50	73.207	79.490
	100	78.412	82.278
	200	81.507	83.074
C6288	1	35.343	30.991
	50	99.225	98.211
	100	99.483	99.471
	200	99.560	99.563
C7552	1	15.377	34.720
	50	81.947	84.755
	100	87.099	88.135
	200	89.761	90.044

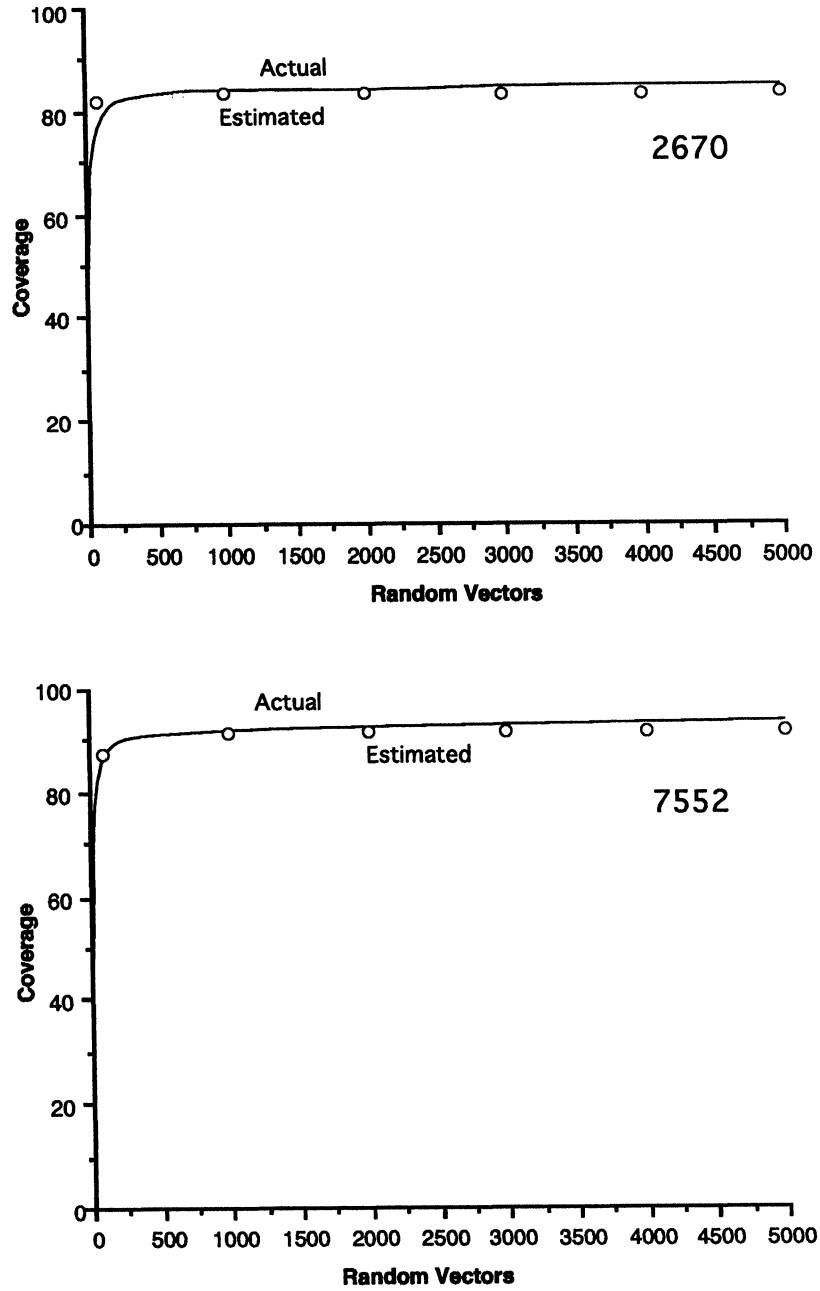

FIGURE 3 Estimated and actual random coverage distribution.

studied. This variance, however, is removed as the number of vectors generated increases. Initial estimates of coverage can be improved if "fault dropping" is used [9]. When fault dropping is used, X_i is the value of the vector number for which fault f_i is first detected.

Deterministic test generation. For the deterministic test generation case the proposed method was used on three of the largest ISCAS-89 circuits, S35932, S38417, and S38584 [5]. Although these are known to be sequential circuits, we have regarded them as combinational by considering all the flip-flops fully controllable and observable, as if they were connected in a full-scan chain.

Here unlike the random test generation case, however, two samples of faults were used; one sample to generate the deterministic vectors, and another sample to collect the X_i and W_i counts by simulating these vectors on the new sample. To generate the deterministic vectors we used the PODEM test generator on a sample of 500 faults [10]. The number of tests generated were 27 for the S35932 circuit, 103 for the S38417 circuit, and 80 for the S38584 circuit. All remaining undetected faults were identified as redundant or aborted (an aborted fault is a fault for which a test cannot be found within a time limit set on a test generator search time; this time limit is a result of the NP-complete nature of test generation [12]).

The generated tests were then simulated without fault dropping on a different sample of 1000 faults. For this the deductive fault simulator was used. (Here, it is important to mention that a sample size of 1000, and not 500, faults was chosen in order to get a better estimate of the detection probabilities; this sample size, however, is still very small relative to the size of the actual fault population, well under 5% for any of the three circuits). The testability profile parameters were then estimated from the X_i and W_j counts using the IMSL routine "DQ PROG." The number of parameters chosen for estimating the testability profile were approximately half the number of vectors generated. The number of parameters for the S38417 circuit was 50. The numbers of parameters chosen for the S35932 and S38584 were 20 and 40, respectively. Note that 20 parameters were chosen for the S35932; this was done because the number of vectors generated was small (27 vectors). Table 2 shows the non-zero computed parameters for the three circuits.

The predicted distribution of the deterministic fault coverage was obtained from $y_n \approx 1 - I(n) + n/Y$. To compare the distributions of the predicted and actual population coverage the standard test generation process was performed on the entire fault population. In a separate run, tests were generated for the three circuits. For the S35932 circuit 78 vectors were generated. The tests covered 89.809% of the faults. For the S38417 (S38584) circuit, a test set of 1318 (900) vectors was generated. The test set covered 99.410% (95.502%) of modeled faults. Figure 4 shows the curves of actual and estimated fault coverages of the three circuits.

TABLE II
Computed Parameters for the Three Circuits

s38417		s38584		s35932	
a_1	0.035455	a_1	0.058022	a_1	0.099899
a_2	11.245017	a_2	9.830469	a_2	0.086855
a_3	1.968737	a_4	8.809089	a_3	1.799668
a_4	0.497892	a_7	1.835551	a_4	5.858076
a_5	3.717851	a_{10}	1.385712	a_5	2.852115
a_8	4.463150	a_{11}	3.366614	a_9	4.782398
a_9	2.014120	a_{16}	2.449521	a_{10}	0.282283
a_{13}	6.406144	a_{19}	6.144186	a_{12}	1.076726
a_{18}	3.352960	a_{22}	0.099103	a_{13}	0.363795
a_{19}	0.145703	a_{23}	1.445490		
a_{23}	4.441681	a_{26}	0.571235		
a_{24}	1.082393	a_{27}	0.312525		
a_{27}	5.846535	a_{33}	0.445554		
a_{28}	0.488900	a_{37}	0.042079		
a_{33}	0.415081				
a_{38}	1.078862				
a_{47}	0.036695				
a_{48}	0.060981				

5 CONCLUSION

This paper considered a testability model similar to that of *actual* testability distributions. As a result the model generalizes a previous beta testability model. A relationship between testability and fault coverage were used to predict random and deterministic coverage distribution without the need to generate test vectors or to employ fault simulation. Applications of the presented work include: 1) prediction of test set length needed to cover a certain fraction of modeled faults, 2) test generation by fault sampling, and 3) estimation of the testability profile of a circuit.

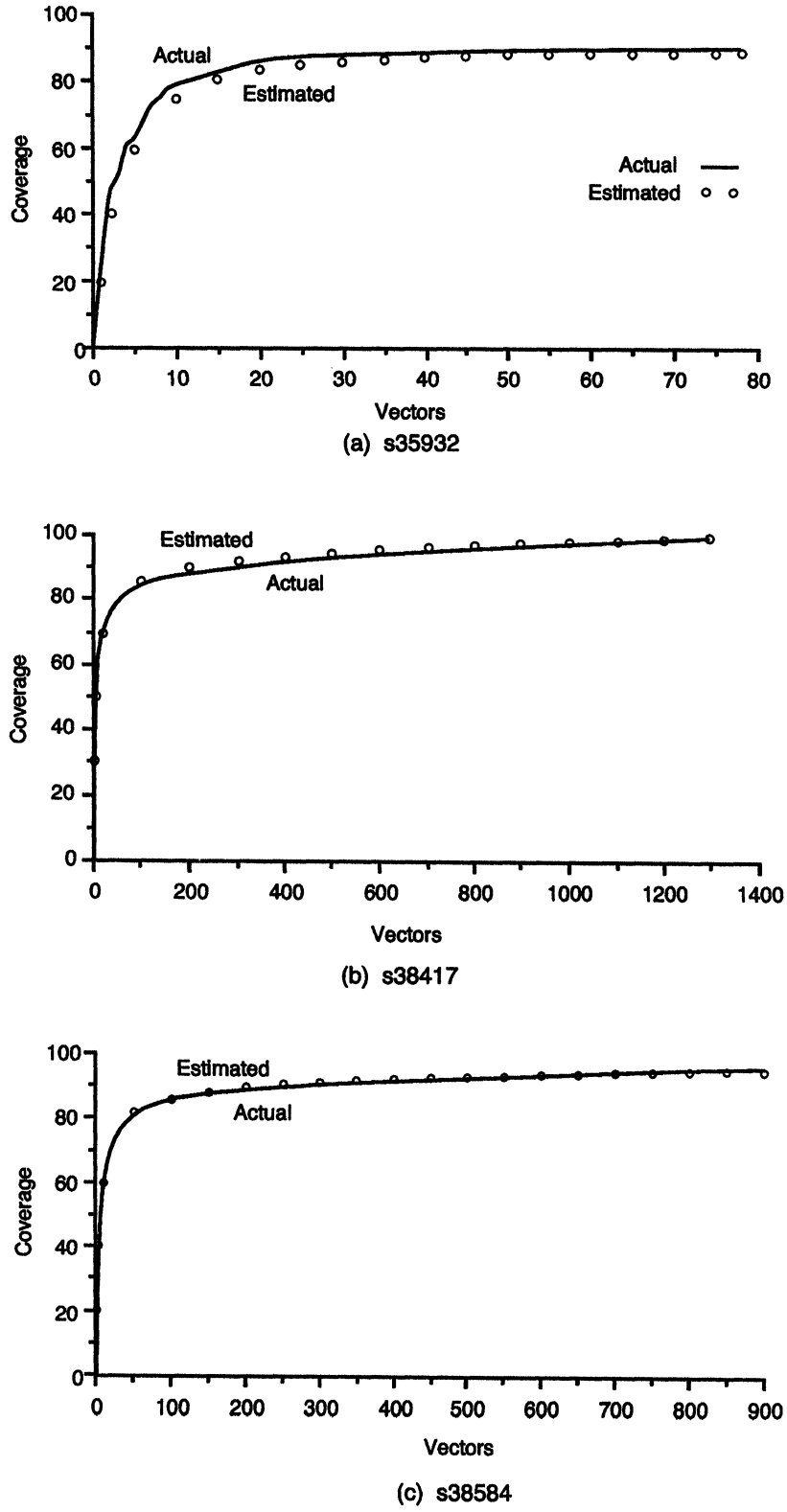

FIGURE 4 Estimated and actual deterministic coverage distribution.

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Biographies

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