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Application of Dynamic Supply Current Monitoring to Testing Mixed-Signal Circuits

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This paper applies the time-domain testing technique and compares the effectiveness of transient voltage and dynamic power supply current measurements in detecting faults in CMOS mixed-signal circuits. The voltage and supply current (i_{DDT}) measurements are analyzed by three methods to detect the presence of a fault, and to establish which measurement achieves higher confidence in the detection. Catastrophic, soft and stuck-at single fault conditions were introduced to the circuit-under-test (CUT). The time-domain technique tests a mixed-signal CUT in a unified fashion, thereby eliminating the need to partition the CUT into separate analogue and digital modules.

Keywords: CMOS, VLSI, mixed-signal, supply current, testability, fault coverage

1. INTRODUCTION

Testing is one of the major bottle-necks in the production of integrated circuits (ICs). As the electronic circuits and systems realised on ICs grow in complexity and density due to improved VLSI (Very Large Scale Integration) fabrication processes, the task of testing also becomes more complex leading to an increase in the time, and hence cost of production.

For digital ICs, including complex VLSI ones, the task of testing is now manageable. This has been achieved by the use of simple fault-models, devising efficient test pattern generation algorithms to detect the faults synthesized by the fault-models [1–3], and the introduction of design-for-testability (DFT) techniques during the early stages of an IC design to enhance its testability [4,5]. Software test tools and automatic test equipment (ATE), that implement most of the testing algorithms and testability enhancement techniques for digital ICs, are now widely available.

The testing algorithms and DFT techniques for digital ICs, and the test tools that implement them, unfortunately, have no counterparts for analogue integrated circuits. This is due to the complex characteristics of analogue circuits. The characterisation of analogue circuits depends on continuous descriptive variables, such as magnitude and frequency for amplifier gain, rather than the discrete variables of logic

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levels in a digital circuits. This makes the design and test of an analogue circuit more knowledge intensive than its digital counterpart. Furthermore, the requirement to handle the complex, and many times conflicting, parameters of an analogue circuit results in the lack of efficient simulation and test tools similar to those for digital circuits. A concerted effort has been put, especially during the past two decades, to devise testing algorithms for discrete analogue circuits and systems [6]. The algorithms, however, cannot be readily extended to testing analogue ICs due to the need for access to a high number of nodes, and the limitation on the number of components they can deal with [7]. At present, testing an analogue IC involves verifying that the manufactured IC meets the design specifications, such as gain, bandwidth and noise margin. This process is time consuming and costly.

Mixed-signal integrated circuits are ICs that have both analogue and digital circuitries on a single chip. It is common for a single mixed-signal IC to support analogue voltage references, amplifiers, comparators, analogue-to-digital (A/D) and digital-to-analogue (D/A) converters, and a wide range of digital components including microprocessors for data processing. Such ICs result in an improvement in system performance and reduction in cost. However, the incorporation of analogue and digital circuits on a single device present a formidable problem for testing compared to pure analogue or digital ICs. This is due to the difficulties associated with testing analogue circuits, which were outlined above, and the lack of controllability and observability of embedded circuit modules. The testing task is exacerbated further by the presence of interface circuit blocks, such as A/D and D/A converters, and other circuit modules (e.g switched capacitor circuits) that exhibit both analogue and digital characteristics.

In practice, mixed-signal ICs are tested by partitioning the device into separate analogue and digital modules, by including extra probe pads to provide access to internal signals, and applying mode-specific tests to each module using separate analogue and digital test setups. The inclusion of probe pads results in an increase in the wafer area required, reduces IC reliability and performance, and increases its overall cost. The use of powerful digital signal processing (DSP) techniques to emulate the analogue test instruments has enabled the digital and analogue tests to be performed by a single measurement system, thus enabling control of signal timing to be maintained [8]. However, the use of this approach does not eliminate the partitioning requirement due to the need to inject and monitor the response to different types of test vectors.

A testing strategy for mixed-signal circuits called "time-domain testing" was proposed [7,9]. The technique eliminates the requirement to partition a mixed-signal circuit-under-test (CUT) by testing the CUT in a unified fashion. An overview of the technique is presented in a later section of this paper. A prototype system that implements the time-domain technique and some practical results were presented in [10].

In this paper we present the results of applying the time-domain technique to testing a CMOS mixed-signal circuit. Both the voltage at the output nodes of the circuit and variation in the dynamic power supply current (i_{DDT}) are measured and processed to evaluate their effect on fault-coverage.

2. OVERVIEW OF TIME-DOMAIN TECHNIQUE

The time-domain testing technique is based on the excitation of the CUT with a sequence of pulses, and subsequent measurement of the transient response at the output node/s [7,9–10]. Both the transient voltage at the output node/s and the transient current i_{DDT} of the supply current are measured. The transient current (i_{DDT}) testing technique is similar to the I_{DDQ} testing technique [11–12], except that I_{DDQ} testing is performed under static conditions while i_{DDT} testing is performed under dynamic conditions.

A major advantage of the time-domain approach is that the transient response contains a wealth of information about the CUT. This information can then be processed by applying digital signal processing (DSP) and other techniques to extract measures of the various CUT parameters. In this paper, the primary objective when processing the transient response data

is to establish whether the CUT is faulty or not (i.e. go/no[00ff]2Dgo), and not to locate and identify the type of fault present if any.

The type of test sequence to be applied to a CUT is a pseudo random binary sequence (PRBS). The PRBS is chosen because it can be readily generated by a digital tester, such sequences have well defined properties [13], can be used to extract the impulse response of linear analogue CUT and the pulse width can be tailored to force large Fourier components to fall within the sensitive region of the circuit response [7,14]. If the CUT is a mixed-signal network, the response generated by applying a PRBS test signal can be used as a signature to characterize the network under-test.

3. ANALYSIS METHODS

Three methods are proposed to analyze the transient response data extracted at the external nodes of a CUT as a result of exciting it with a PRBS signal. The objectives are to establish which type of measurement (i.e. voltage or current) is best at detecting a particular fault, which method of analysis achieves the highest fault-coverage and which one is most efficient in terms of computation. The methods of analysis are:

1- Samples Values
2- Rate of Change
3- Response Digitization

3.1 Samples Values

In this method a fault is detected by comparing the values of the samples of the response of the CUT with those of the fault-free toleranced response. The number of instances (i.e samples) at which the CUT response falls outside the tolerance envelope are counted, and the percentage of deviation from the ideal response is accumulated. A new parameter called the Coefficient of Variation (CV) is calculated for each fault that was detected at least at one instant. The CV defined in this paper is different from the standard definition of the statistical coefficient of variation. The objective of calculating CV is to determine which type of measurement, voltage or current, detects a particular fault with higher degree of confidence. CV is defined by Equations 1 and 2.

$$D_i = |(Yf_i - Yn_i)/\bar{Yn}| * 100\% \quad (1)$$

$$CV = (dn/M) * \sum_{i=1}^{M} D_i \quad (2)$$

where:

i = 1,2,...M
M = Total Number of Samples
D = Percentage of Deviation
$\bar{F}_n$ = Response of Fault-Free CUT
Yn = Average of Fault-Free CUT Response
Yf = Response of CUT
dn = Number of Detection Instances

CV is then normalised to make it easier to compare the results of processing the transient responses of the voltage and current measured. The example below demonstrates the samples values method.

Example: For a particular circuit assume that the tolerance is ±10% and the number of samples collected for the analysis of its voltage response is M = 10. If under fault-free (Yn_i) and a faulty condition (Yf_i) the responses are

Yn_i = [0, 0.85, 1.5, 2.3, 3.45, 4.8, 3.2, 2.95, 2.0, 1.25]
Yf_i = [0, 1.05, 1.58, 2.1, 2.85, 3.67, 3.4, 3.58, 3.25, 2.15]

applying Equ.1 gives

D_i = [0, 8.97, 3.59, 8.97, 26.91, 50.67, 8.97, 28.25, 56.05, 40.36]

The number of detection instances dn = 6, because samples 1, 3, 4 and 7 fall within the bounds of the nominal toleranced response. Applying Equ.2 gives

CV = 139.64. When the CVs for all the faults are calculated the results are normalised and compared with those for the current response. If for a particular fault condition the normalised voltage CV is higher than the normalised current CV, it would then be concluded that the fault is best detected by voltage measurement.

3.2 Rate of Change

In this method, the rate of change (R_t) of the response of a CUT between the sampling intervals (Δt) is calculated according to Equation 3.

$$R_t = (m_{i+1} - m_i)/\Delta t \quad (3)$$

where m_i and m_{i+1} are the values of the response at samples (i) and (i + 1) respectively.

The rates of change for the CUT is then compared with that of the fault-free response. This method of analysis is capable of detecting faults which produce responses similar to that of the fault-free one but are shifted in time.

3.3 Response Digitization

In the digitization method of analysis the transient response waveforms of both output voltage and supply current are digitized into 3-levels: 1, -1 and 0. This is achieved by assuming a threshold value, V_{th} and I_{th} for voltage and current respectively, with a small bound round it. The upper and lower bounds for the voltage response are V_{thH} and V_{thL} respectively. Similarly, the bounds for the current response are I_{thH} and I_{thL}. These bounds are the worst case tolerance values for each response. If a sample data value falls above the upper-bound (V_{thH} or I_{thH}) of the threshold value it is considered a logic high (1), if it falls below the lower-bound (V_{thL} or I_{thL}) it is considered a logic low (-1), and otherwise the logic is considered unresolved and denoted by 0. The digitized fault-free and CUT responses are then compared to determine the number of instances at which a fault is detected.

Having tight bounds round a response increases the sensitivity of the measurement to faults and may lead to higher detection rates. However, the bounds should reflect the actual tolerance of the circuit. Otherwise, misleading high detection rate may be achieved by, for example, the imposition of artificially tight bounds.

Varying the threshold value may lead to the detection of faults that otherwise will not be detected, and an increase in the number of detection instances for some faults. Therefore, the program that implements the digitization method varies the threshold value by requesting the number of times the analysis is to be repeated. It uses this to divide the space between the maximum and the minimum values of the fault-free response to a uniform set of threshold values, each one of these values is considered a test. The program keeps track of all these tests, then compares them to determine the overall fault-coverage and which test is best at detecting a particular fault and the highest number of detection instances achieved.

4. CMOS MIXED-SIGNAL CIRCUIT EXAMPLE

To demonstrate the effectiveness of the time-domain approach and the analysis methods in testing mixed-signal ICs the simple circuit shown in Figure 1 was simulated and tested. The circuit consists of four modules: a low-pass filter (LPF) with a 3-dB bandwidth of 2-KHz, a sample and hold (SH) circuit, a 2-bits analogue-to-digital converter (ADC), and a full-adder digital logic network. The schematics of the operational amplifier, comparator and analogue switch are illustrated in Figure 2 [15], Figure 3 [16] and Figure 4 respectively. The logic gates are all standard cells.

The CMOS mixed-signal circuit in Figure 1 was tested by injecting a 15-bits PRBS test sequence at the LPF input (Vin), with a 250 μsec bit interval. The

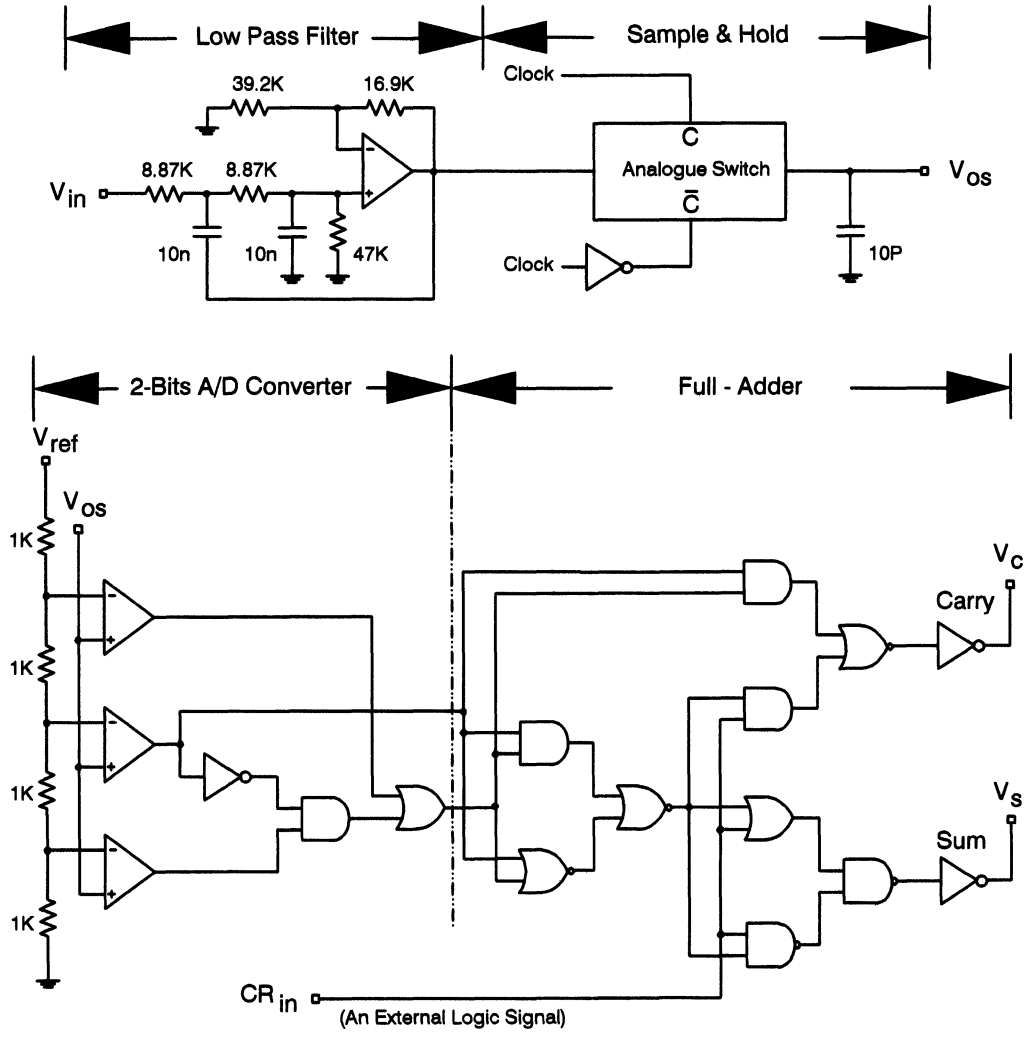

FIGURE 1 CMOS mixed-signal circuit tested.

transient voltage responses at Vs and Vc, and the supply transient current i_{DDT} were sampled every 10 μsec, resulting in 375 samples for each waveform. The PRBS input signal and the fault-free transient responses at Vs, Vc and i_{DDT} are illustrated in Figure 5.

A total of 140 single fault conditions were simulated. Of these faults 115 were catastrophic faults in the MOS transistors of the various modules, 5 soft faults in the resistive and capacitive components of the LPF, SH and ADC, and 20 stuck-at (s-a-1 and s-a-0) faults at the terminals of the digital logic gates. The fault model adopted for catastrophic faults in MOS transistors is depicted in Figure 6. The model is based on the studies of integrated circuits yield [17–18], and the work on the likely catastrophic faults in MOS transistors reported in [19–20]. The faults synthesized by the model in Figure 6 and the status of the associated switches are summarized in Table I.

All the results obtained are based on simulating the mixed-signal circuit under fault-free and faulty conditions using HSPICE [21], the analogue circuit simulator. The methods of data analysis, described in the previous sections, were all implemented using the

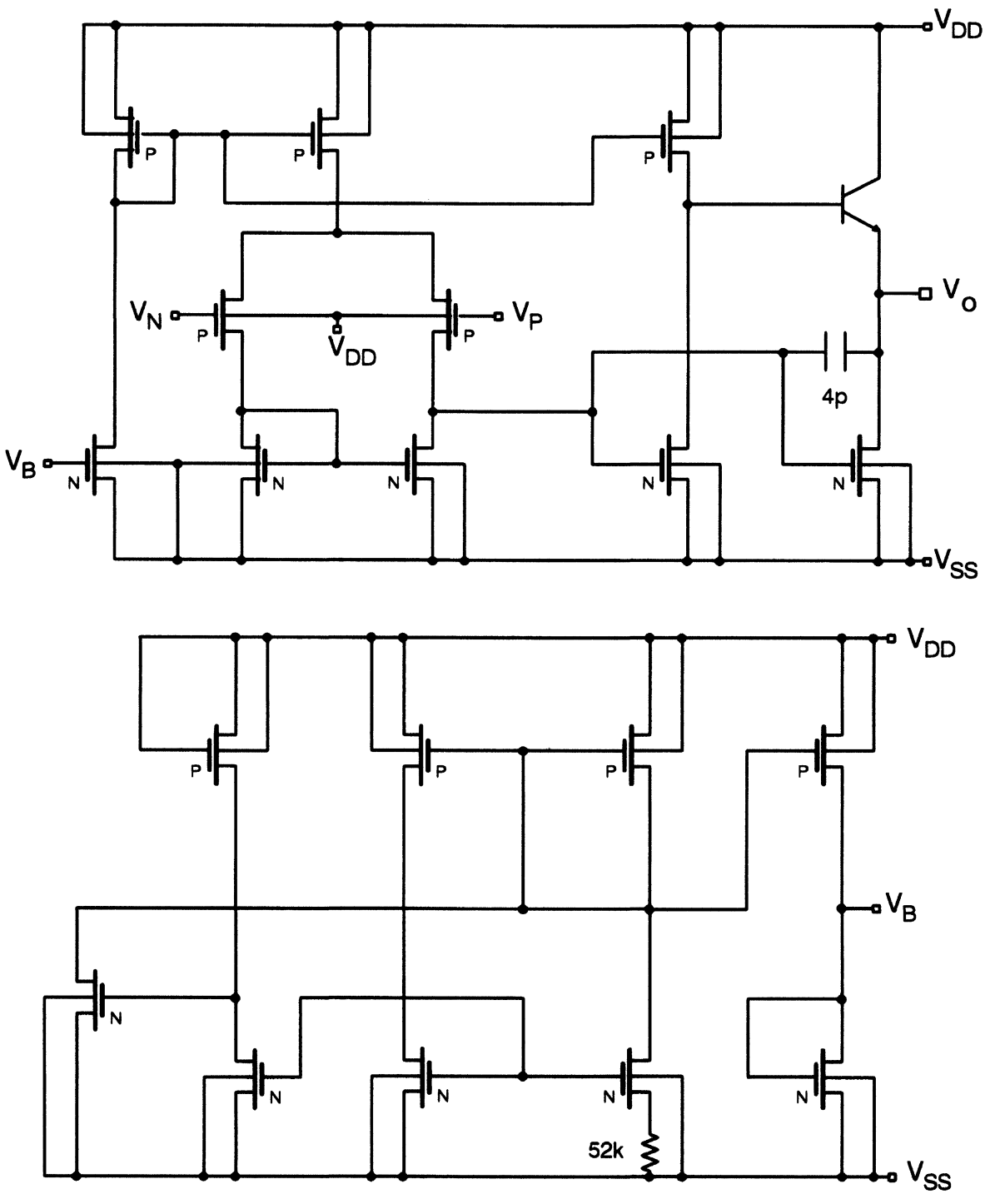

FIGURE 2 Schematic of the operational amplifier.

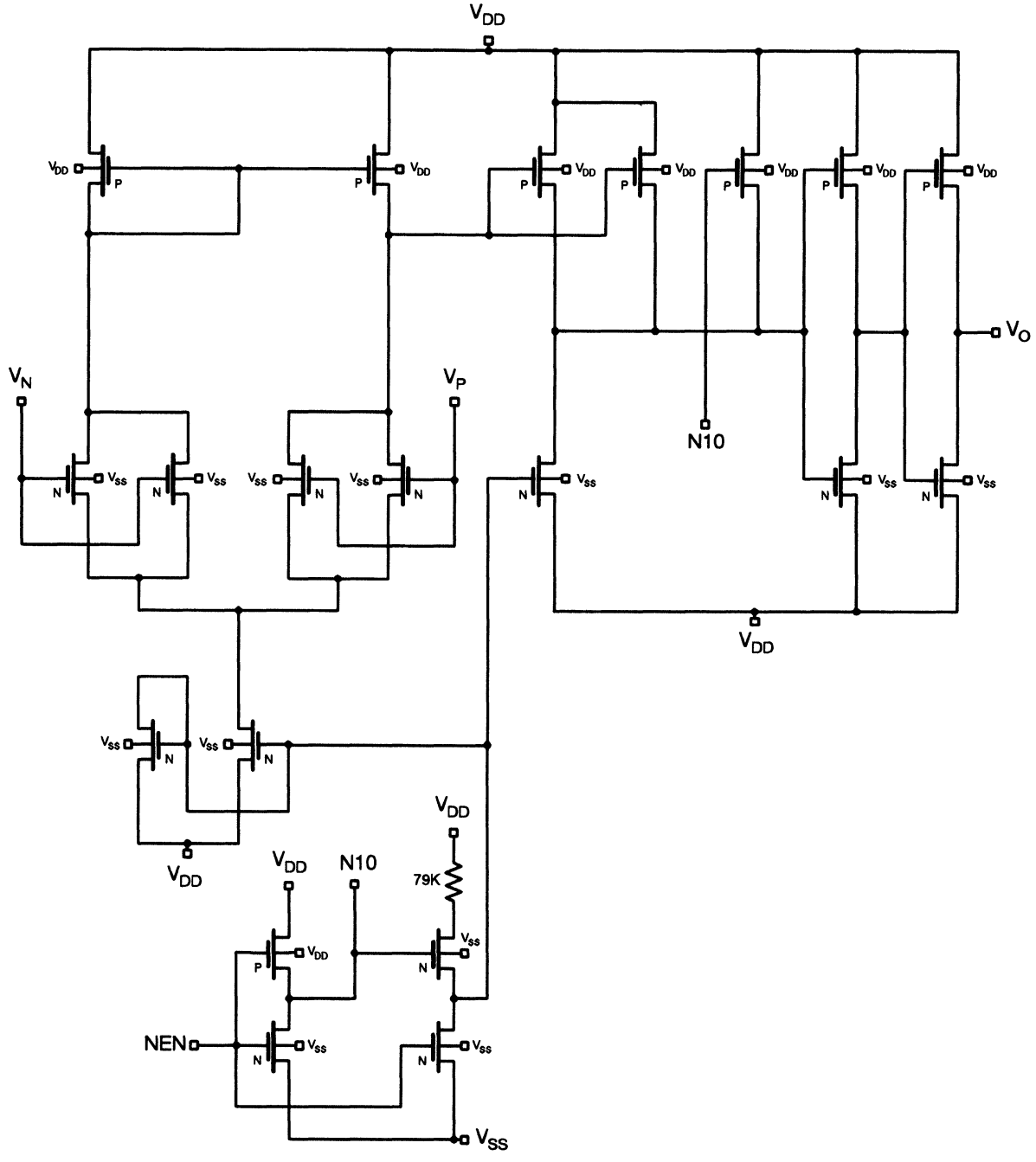

FIGURE 3 Schematic of comparator circuit.

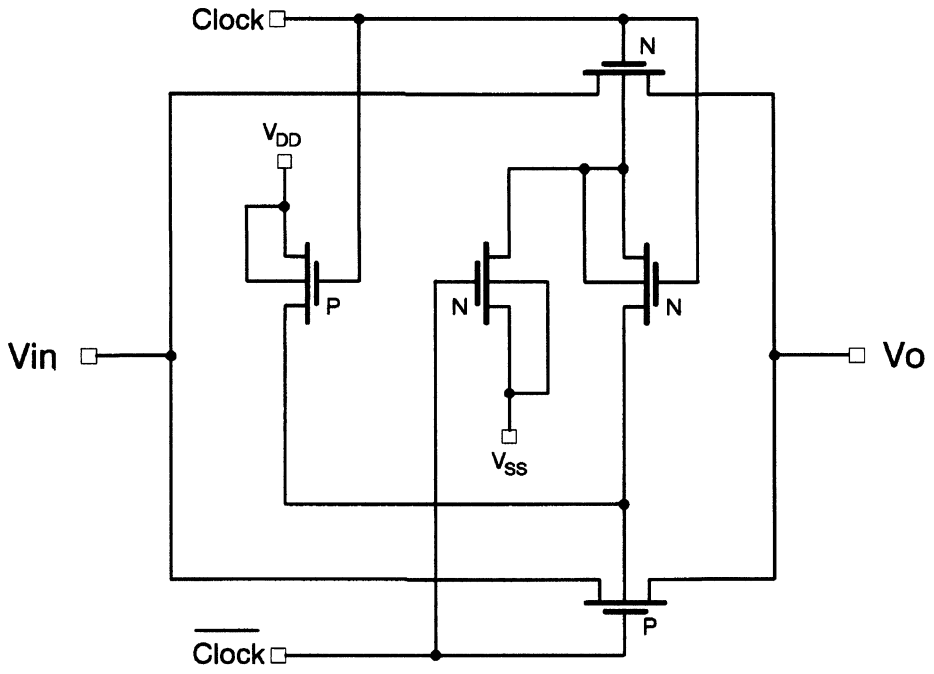

FIGURE 4 CMOS analogue—switch circuit.

mathematical software package MATLAB [22]. In all cases, if the response of the CUT falls outside the bounds of the toleranced response the circuit is considered faulty, hence a fault is detectable.

Analysis of Vs, Vc and i_{DDT} transient response data based on samples values, depicted in Figure 7, shows that the three measurements achieve 100% fault-coverage each. To determine which one of the measurements is best at detecting a particular fault the normalised CVs of Vs, Vc and i_{DDT} were calculated and plotted in Figure 8. The normalised CVs indicate that Vs, Vc and i_{DDT} are best at detecting 72, 32 and 36 faults respectively.

Figure 9 illustrates the results of applying the rate of change analysis method to Vs, Vc and i_{DDT}. It shows that the fault-coverage achieved by each one of the three measurements is 100%.

The application of the digitization method of analysis to Vs, Vc and i_{DDT}, with 10 tests specified, resulted in a fault-coverage of 74.29%, 72.86% and 100% respectively. The plots of the test best suited to detect particular faults and the corresponding highest number of detection instances for Vs, Vc and i_{DDT} are illustrated in Figure 10, Figure 11 and Figure 12 respectively.

5. CONCLUSIONS

The simulation results of the mixed-signal circuit example above demonstrate that the time-domain testing is capable of testing such circuits in a unified fashion, and hence eliminating the need for partitioning. Analysis of the transient voltage and power supply current (i_{DDT}) data indicate that both measurements are complementary in terms of achieving a high percentage of fault-coverage with a high degree of confidence. Of the three methods of data analysis, the response digitization method is the most efficient in terms of computation, because it eliminates the need for floating point computation. The digitization

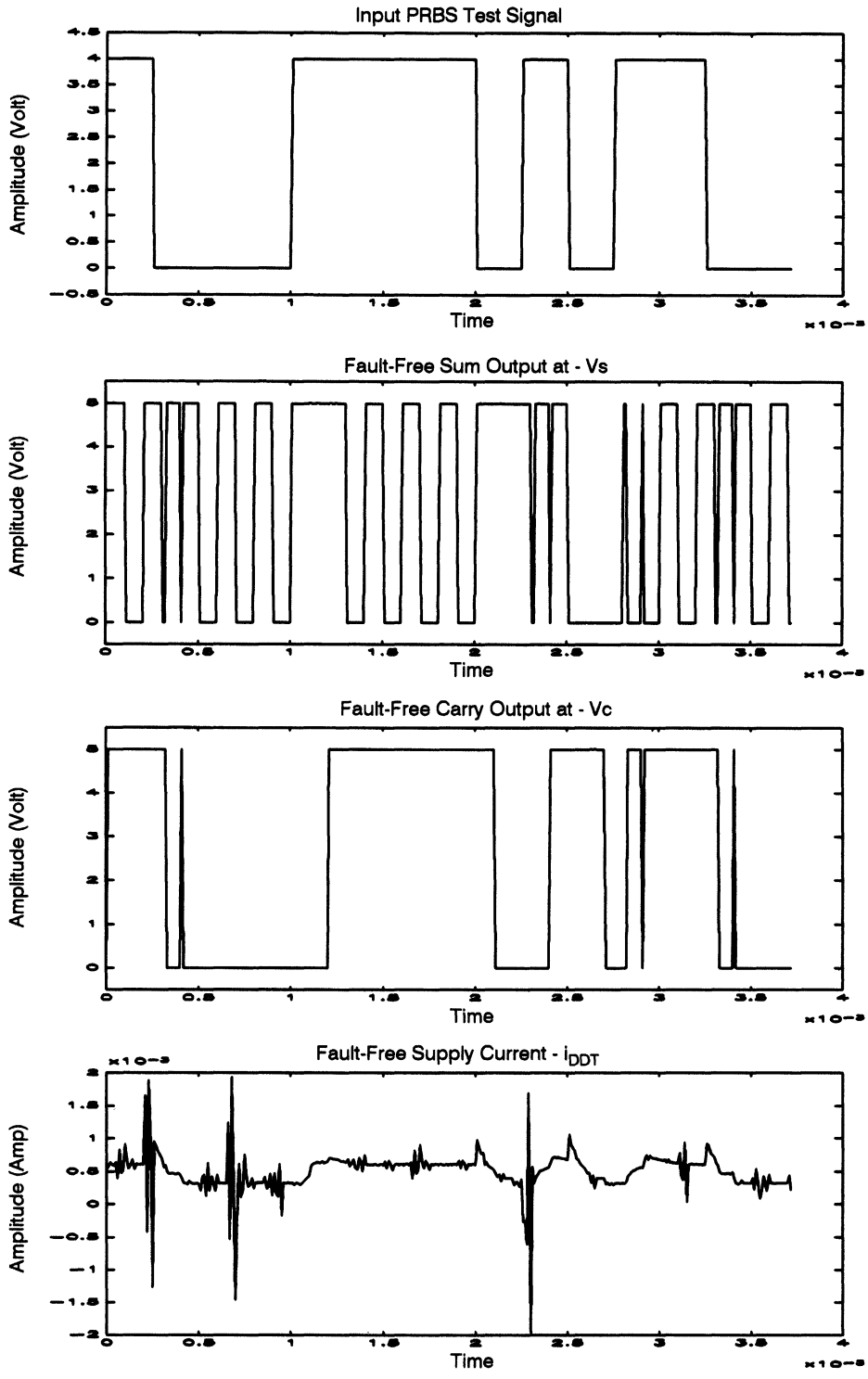

FIGURE 5 Input PRBS and fault-free responses Vs, Vc & i_{DDT}.

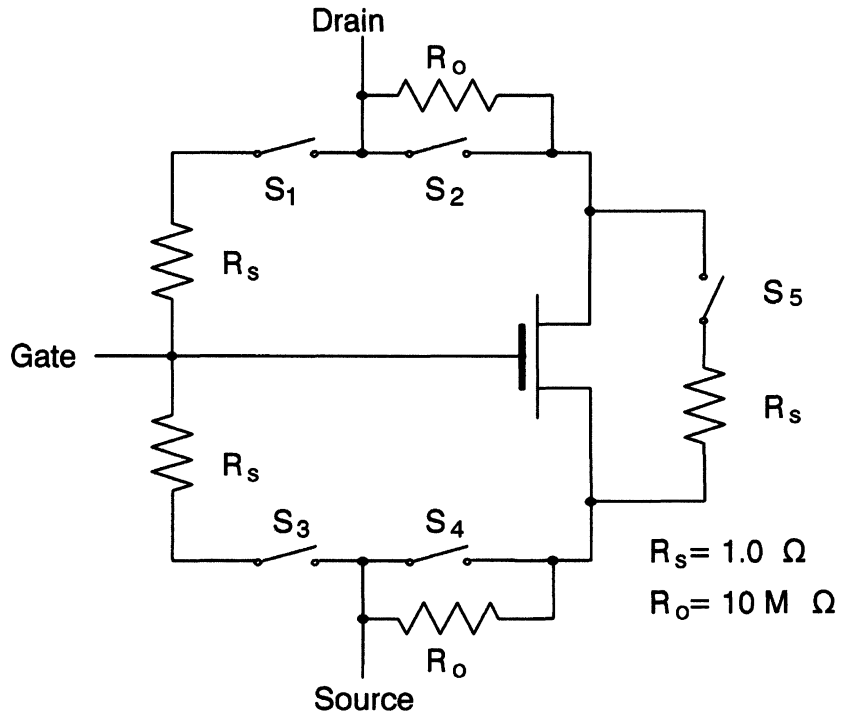

FIGURE 6 Physical MOS transistor fault model.

method can also be implemented on a digital tester, hence resulting in saving in both testing time and cost.

The results presented above are all from the analysis of the extracted simulation data. Implementing the testing technique and methods of analysis in a practical system may lead to a reduction in the detection rates due to the resolution of the measurement system. The resolution of such a system would be particularly important for the data rate method of analysis due to its high sensitivity compared with the other methods. Implementation on a practical system, however, is not expected to result in a substantial reduction in the detection rates discussed above.

The effect of the PRBS length and bit rate on the detection rate was investigated in [7]. It was concluded that in general a longer PRBS would result in a higher rate of detection because the sequence will be closer to white noise and hence exercise the CUT in more states. However, the methods of analysis still lead to the same conclusions presented above.

TABLE I Likely MOS faults and switches status

MOS Device Failure	Status of Fault Model Switches				
	S1	S2	S3	S4	S5
Drain Contact Open	OFF	OFF	OFF	ON	OFF
Source Contact Open	OFF	ON	OFF	OFF	OFF
Gate-Drain Short	ON	ON	OFF	ON	OFF
Gate-Source Short	OFF	ON	ON	ON	OFF
Drain-Source Short	OFF	ON	OFF	ON	ON

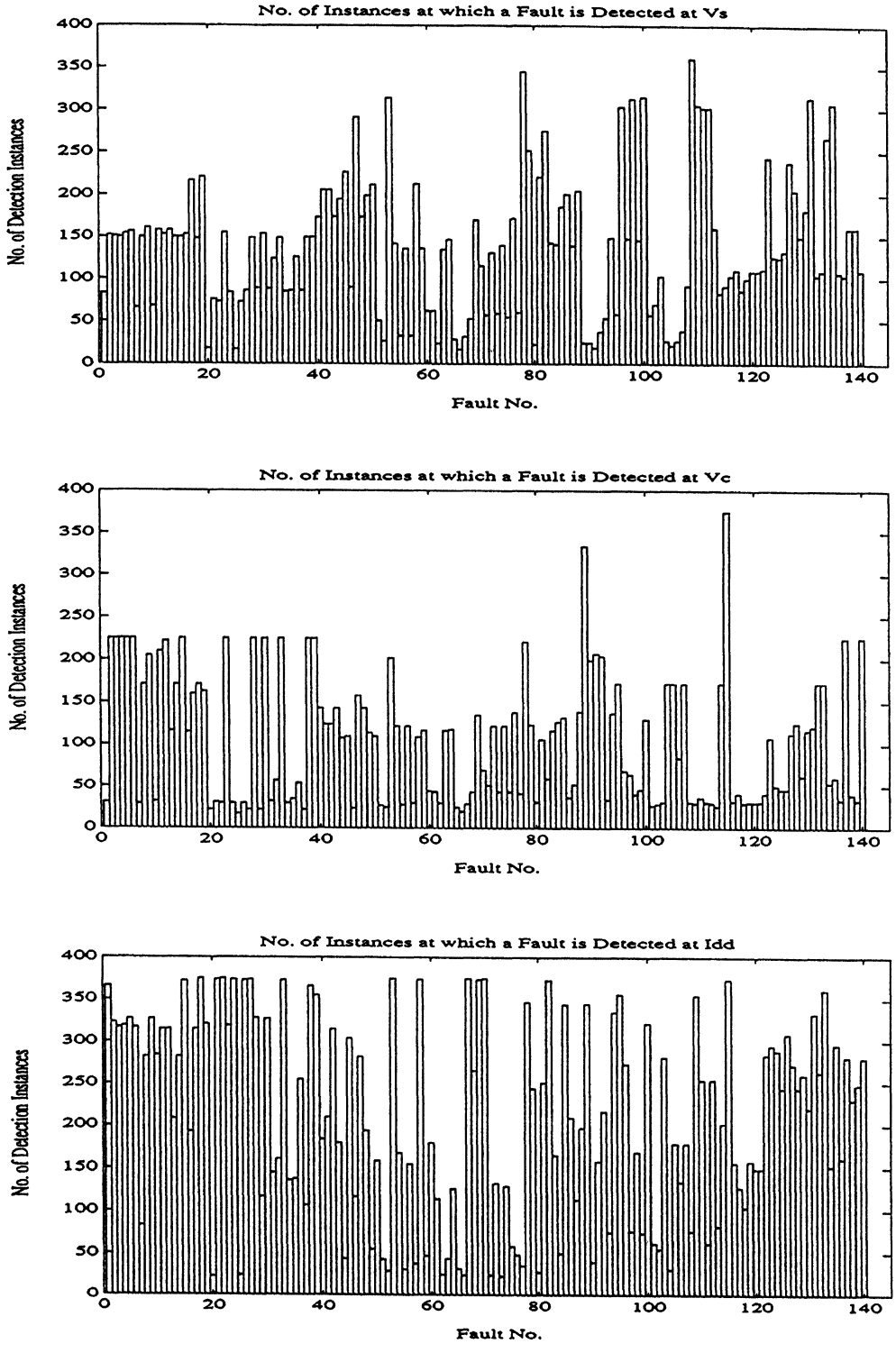

FIGURE 7 Detection instances by Vs, Vc & i_{DDT} of mixed-signal circuit.

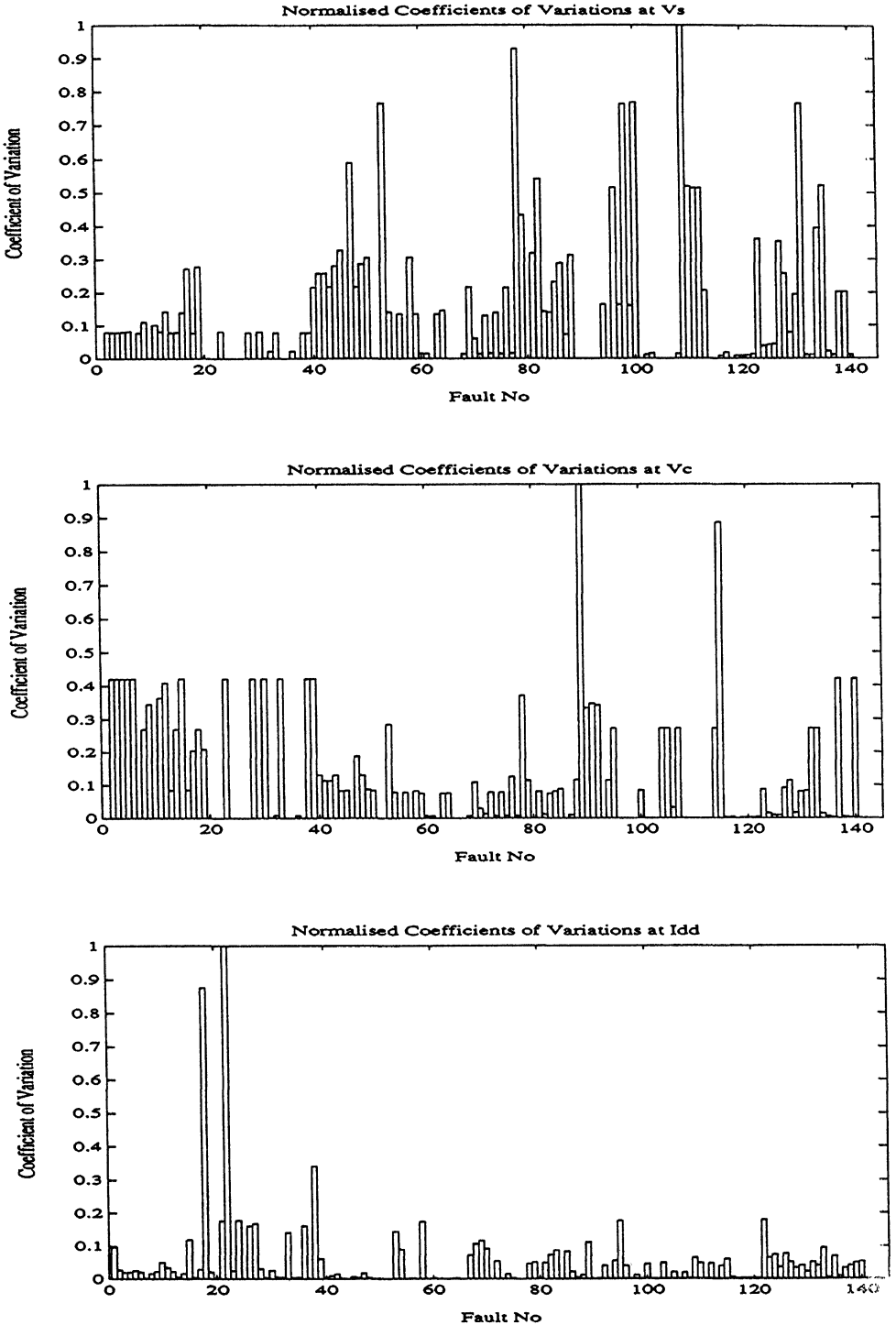

FIGURE 8 Normalised CVs of Vs, Vc & i_{DDT} of mixed-signal circuit.

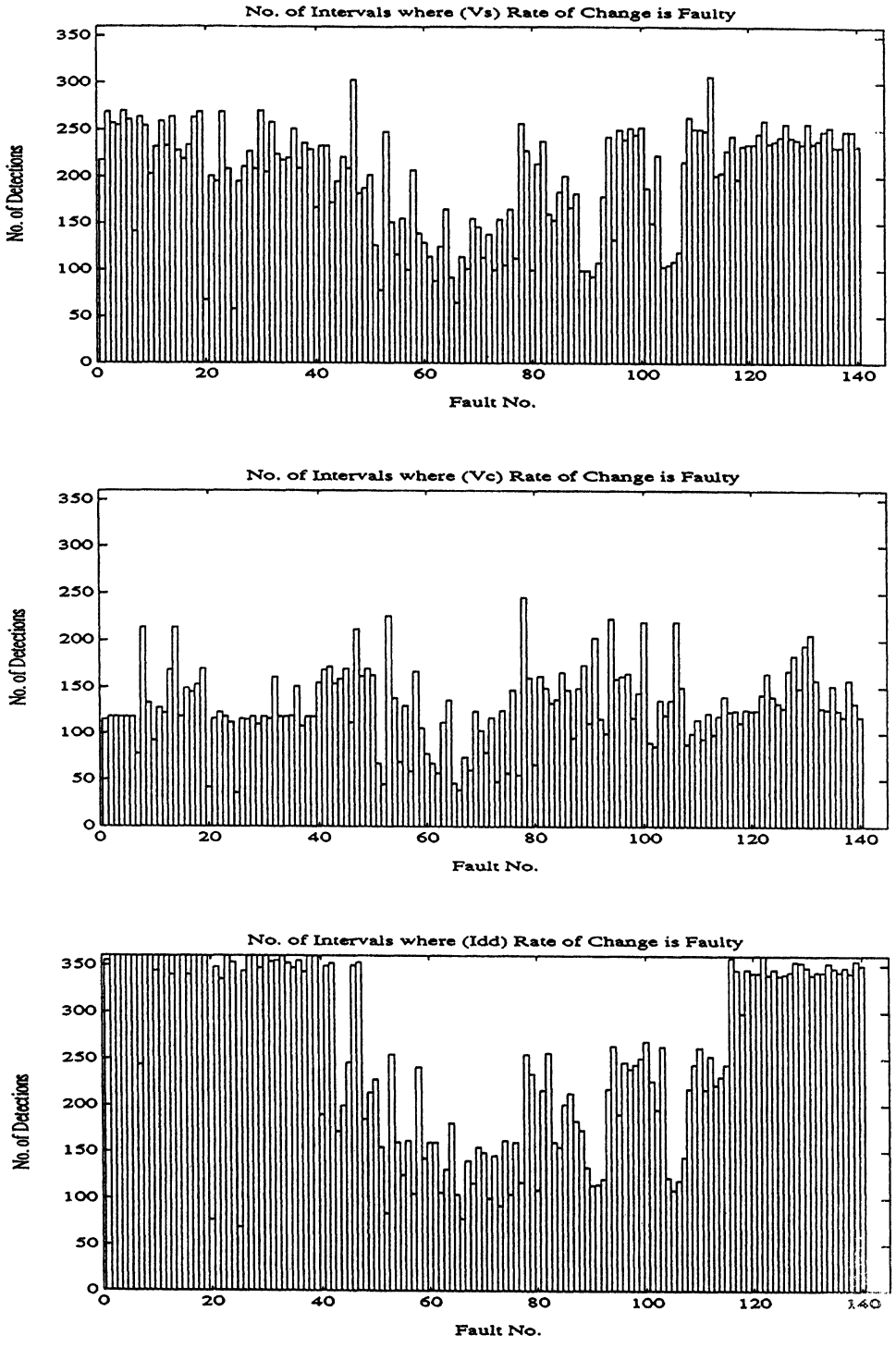

FIGURE 9 Det. intervals by Vs, Vc & i_{DDT} rate of change of mixed-signal circuit.

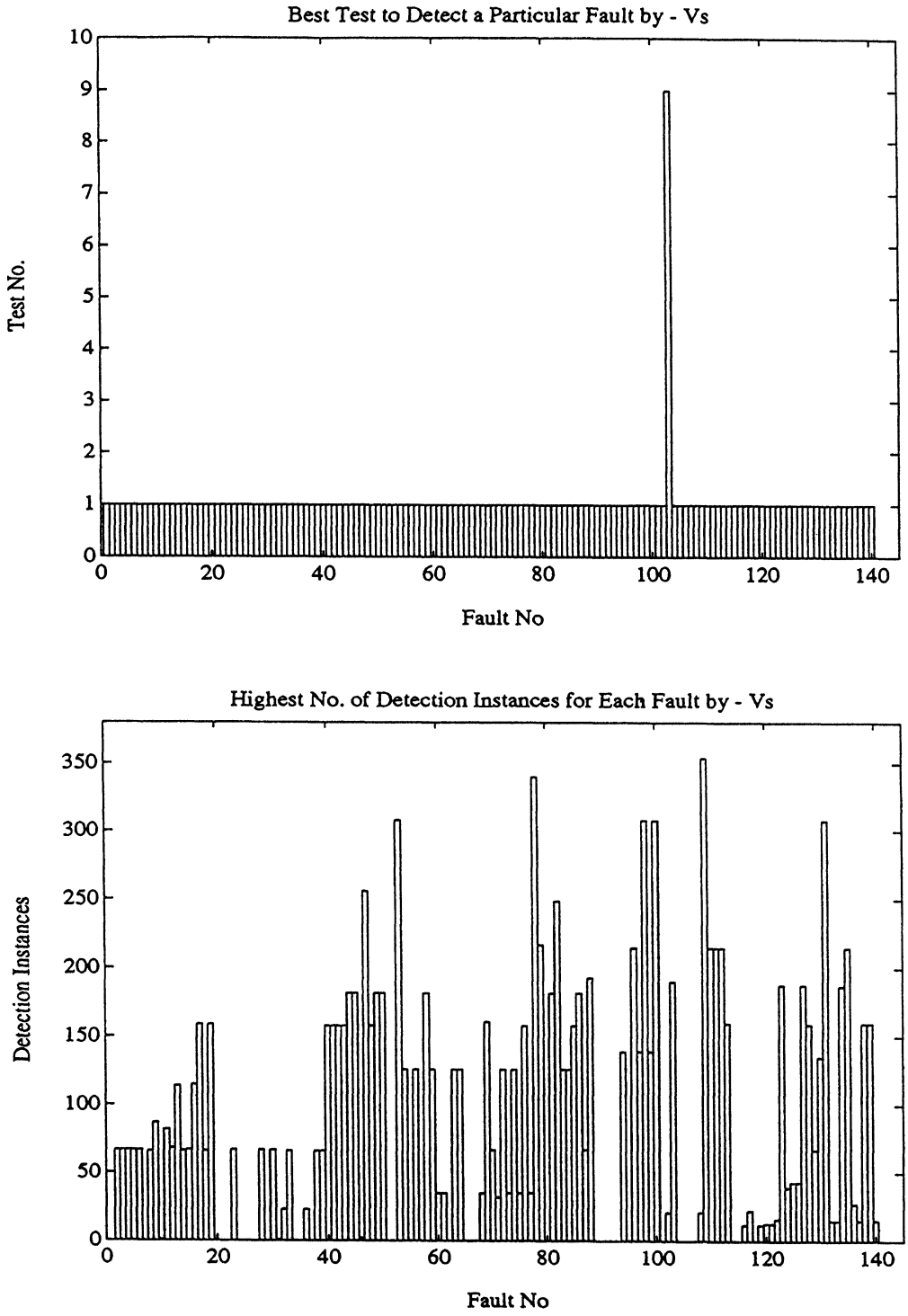

FIGURE 10 Best test & highest detection by digitized Vs of mixed-signal circuit.

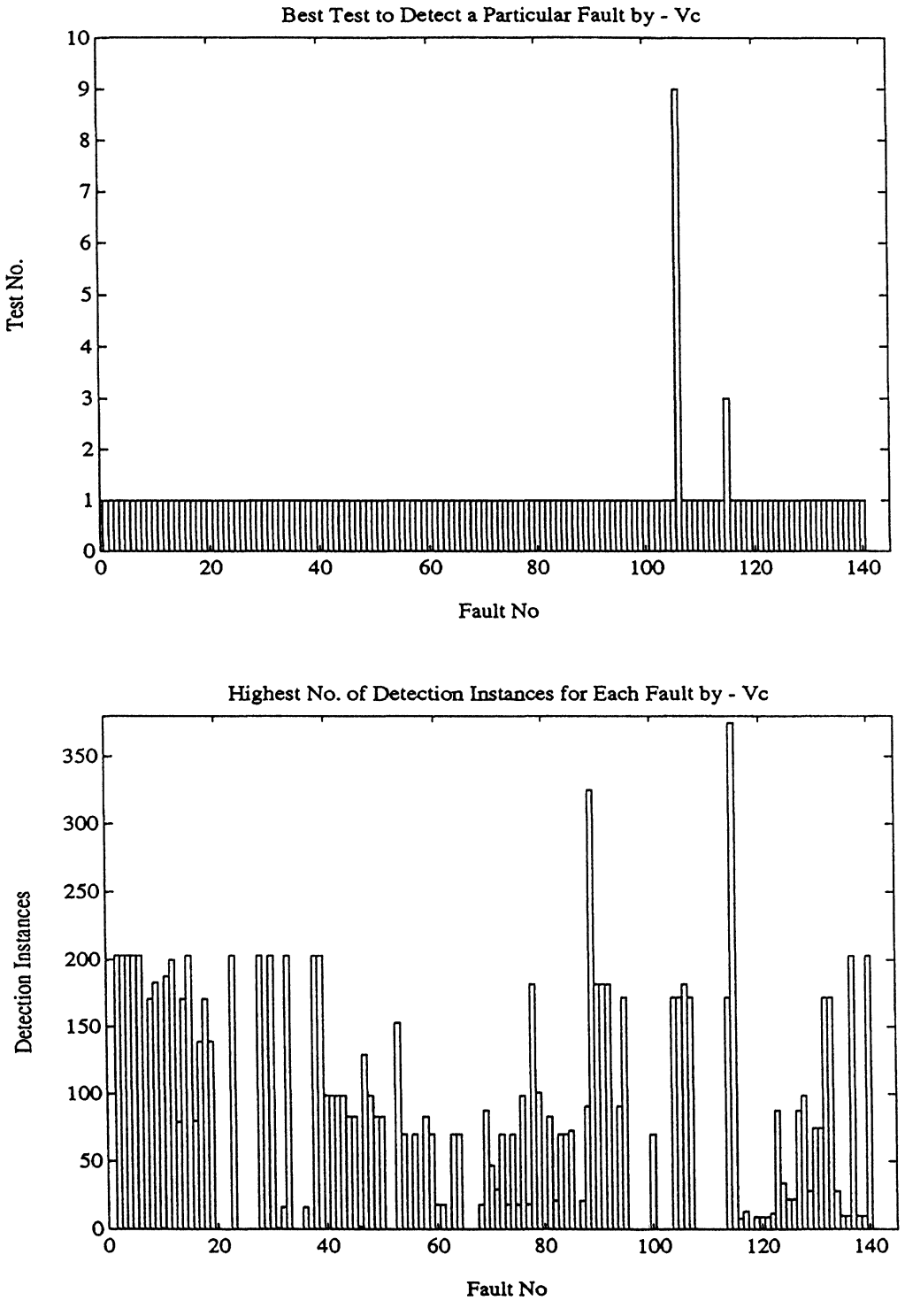

FIGURE 11 Best test & highest detection by digitized Vc of mixed-signal circuit.

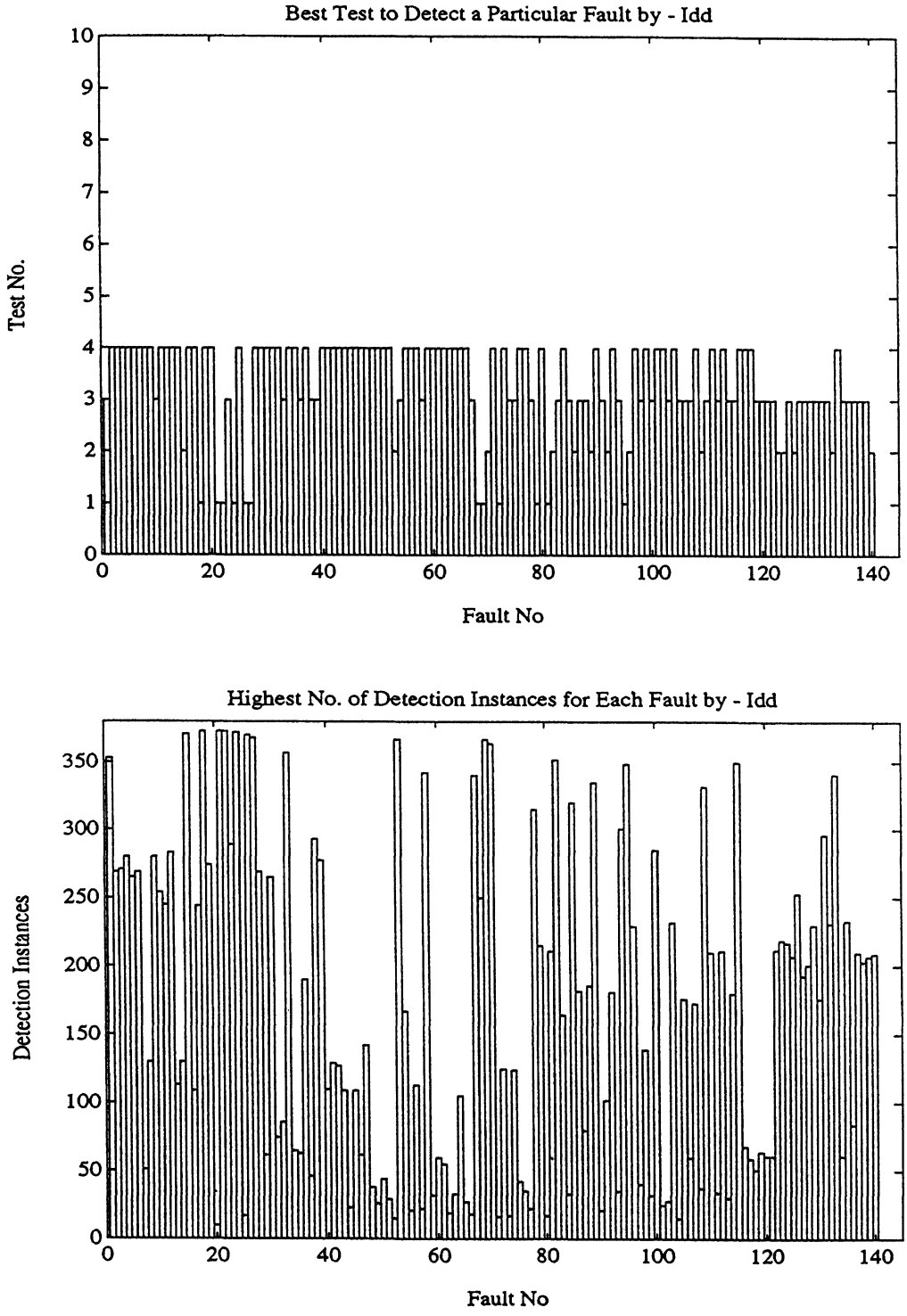

FIGURE 12 Best test & highest detection by digitized i_{DDT} of mixed-signal circuit.

In its present form, the time-domain testing approach is unlikely to lead to a complete unified test solution for complex mixed-signal circuits due, for example, to a reduction in the PRBS signal resolution and change in its characteristics. However, the technique is expected to be of substantial benefit when used in conjunction with the mixed-signal test bus [23] or other analogue built-in self test techniques [24].

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Peter R. Shepherd received his BEng in Electronic Engineering from the University of Sheffield. He worked for Plessey Semiconductors as a Process Engineer manufacturing VLSI circuits. He then studied

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