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I_{DDQ} Testing Experiments for Various CMOS Logic Design Structures

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In this paper, we present two studies. The first study constitutes an assessment of the effectiveness of I_{DDQ} (quiescent power supply current) in detecting transistor-level defects for three CMOS logic design styles. This study was carried out by designing, simulating, fabricating, and testing CMOS devices with built-in defects. The second study involves an assessment of I_{DDQ} in a production-type environment and the effect of burn-in on I_{DDQ} levels. This study was carried out in a production facility. The results show that I_{DDQ} testing can detect some types of defects in precharge and pseudo-NMOS circuits but may require partitioning circuitry for the latter.

Keywords: Quiescent power supply current, fully complementary logic, pseudo-NMOS logic, precharge logic, burn-in, logic test

I. INTRODUCTION

Today, companies such as IBM, FORD and PHILIPS [19] are pursuing the ultimate goal of reaching what Taguchi calls "zero defect" level [3], commonly known as Six-Sigma. This new quality goal places very tight performance standards on design, manufacturing, and testing.

The testing approaches in-use today are mostly built around voltage-monitoring techniques and mainly based on the stuck-at fault model. Conventional approaches towards meeting the above quality goals are carried out using an aggregate of test methods including; functional testing, environmental stress screening, statistical product monitoring, and other quality assessment programs, the aim of which is to improve fault coverage. Most of these approaches rely on the stuck-at fault model for test generation which unfortunately is not adequate because it does not accurately model common CMOS defects [22] such as gate-oxide shorts and bridging defects. The present stuck-at testing procedure is not capable, by itself, of detecting all typical IC process defects and hence is insufficient to independently improve quality and reliability of electronic modules to the ultimate Six-Sigma level.

One of the new approaches that has been shown to improve fault coverage of CMOS devices is quiescent power supply current (I_{DDQ}) testing [25] [22] [24] [16] [4] [8] [7]. The I_{DDQ} test method has been shown to be effective in detecting some types of defects that escape

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traditional logic stuck-at tests and a modification to I_{DDQ} has been also shown to improve defect coverage in SRAMs . However, I_{DDQ} test studies have been mostly limited to circuits designed using FCMOS logic. In this paper we present the results of physical experiments that address two issues relative to I_{DDQ} testing. First is the effectiveness of I_{DDQ} in non-FCMOS logic structures, and second is the effectiveness of I_{DDQ} in a production type environment.

The next section presents some background material on defects, fault models, and I_{DDQ} testing. Section III presents the design of two experiments on I_{DDQ} testing, the results of which are analyzed in section IV. Finally, section V provides some concluding remarks.

II. BACKGROUND

This section presents an analysis of CMOS IC defects and their effect on circuit functionality as well as a review of previous work on I_{DDQ}.

II.A. IC Defects and Faults

In this paper, we will use the term defect to mean a deviation from the original design in a manufactured IC that causes a measurable change in a circuit parameter (i.e. voltage, current, timing, etc.). There are global defects that affect a large area of the original wafer, and local defects that affect a much smaller area, such as a single transistor. Cracks or scratches on the wafer, crystalline defects, or major fabrication process errors are examples of global defects. These types of defects usually affect the whole circuit. Local defects, which result from missing or extra material, usually directly affect only a few transistors. In addition the term fault will be used to refer to the effect a defect has on some parameter. When a defect causes an erroneous logic output, it will be called a logic or functional fault. If the defect causes an elevated quiescent power supply current, it will be called an I_{DDQ} fault.

Gate Oxide Shorts

A gate oxide short is a conductive connection through the thin oxide that insulates the gate of a MOSFET transistor from the silicon surface. This conductive connection can be from the gate to the channel (and thus substrate), or to the source or drain diffusion areas (see Figure 1). Gate oxide shorts that occur between the gate and drain or the gate and source are usually caused by electrical overstress or electrostatic discharge (EOS/ESD). The reason behind the occurrence of these defects is believed to be the presence of higher electrical fields at the edges of the gate, as opposed to its interior [21].

Gate oxide shorts that occur in the channel region are usually due to silicon surface defects or gate oxide imperfections caused by contaminants, such as sodium. Since these defects occur randomly in transistors, the large channel area would be more subject to them than the small overlap of the gate over the source or the drain. These contaminants can cause the oxide to be thinner, or can enhance the electrical field in the oxide area. The enhanced field can cause an increase in electrons being injected into the oxide by tunneling, causing an increase in the electrical field. This positive feedback continues until heating causes the oxide to break down, forming a conductive silicon filament [21].

Gate oxide shorts can occur during fabrication or at initial testing, and also after the IC has left the factory. Both types of gate oxide shorts are subject to time dependant breakdown. Burn-in is sometimes used to accelerate the IC life cycle at the manufacturing site by subjecting the IC to elevated temperatures and voltages. Though some of the gate oxide shorts may not cause logic faults, they may cause I_{DDQ} faults. Elimination of the circuits with I_{DDQ} faults can

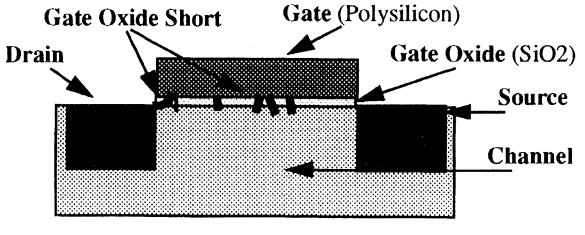

FIGURE 1 A gate oxide short.

help increase the manufacturer's product reliability. Studies have indicated that gate oxide shorts continue to grow with age and eventually cause logic faults [10][21], wherein the transistor becomes stuck-on.

Bridging Defects

Bridging defects are unintended conductive connections between two or more nodes. Bridges can occur between nodes of the same transistor or between nodes of different transistors. In particular, a gate oxide short is a special type of bridging defect. In this paper, gate oxide shorts between the gate and substrate will be considered separately from other bridging defects. A bridge between the source and drain of a transistor can cause the transistor to always conduct. This can be caused by either a missing section of the gate over the transistor channel area or diffusion bloating around the gate resulting in an extra area of diffusion from the drain to the source (see Figure 2) [12]. A high voltage applied to the drain can cause an abnormal condition called punchthrough. Punchthrough can result in the transistor's channel becoming permanently conductive [26].

Extra metal or a breakdown in the insulating layer between conducting elements results in transistor nodes being shorted to one another (see Figure 3). This is how many intertransistor bridging defects occur during fabrication. A report by Acken [1] found the majority of bridges to be below 500 ohms in resistance, while those with higher resistance were over 50 kilo-ohms. Intertransistor bridging defects will usually result in logic faults, due to the typical low resistance of the bridges. There have been studies of the effects of different resistance values for bridging defects on circuit operation [6] and [18]. Only the lowest values of resistance result in logic faults, but even high resistances result in noticeably elevated quiescent current levels. Increased propagation delay and degraded logic levels are also noticeable at higher resistance levels [21]. These effects may cause functional faults and can result in an intermittent faulty behavior.

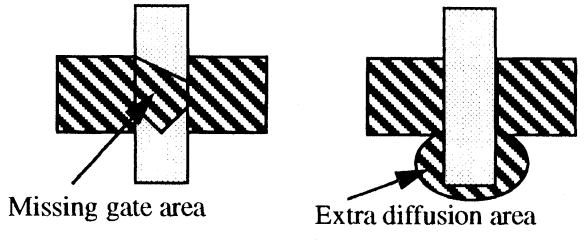

FIGURE 2 A drain-source short.

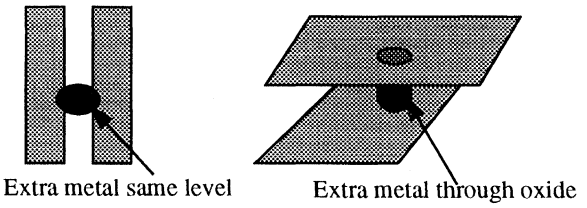

FIGURE 3 Intertransistor bridging defect.

Open Defects

Contaminant particles on the photolithographic masks can result in open areas of metal or polysilicon connecting runs. Electromigration and mechanical stressing can also cause a run to be open. One of the methods used to model the effect of open defects has been the transistor stuck-open fault. This model assumes that the affected transistor is always off and that the logic level at its drain (or output) is a function of the other connected transistors. For FCMOS circuits, Maly has suggested that this model is accurate for only a few of the possible types of opens that can occur [15].

The effect of an open in a circuit depends on where the open occurs with respect to the connected transistors. To understand how different types of opens affect the operation of a circuit, an accurate model of a MOSFET transistor is needed (see Figure 5). This model includes capacitances between all nodes of the transistor and thus the voltage on one node has an effect on the other nodes through charge sharing. The parasitic diodes formed at the p-n junction of the diffusion area (source or drain) and the substrate also affect the operation of the transistor.

For an open in the transistor's source (d1) in Figure 4, the transistor is connected to the substrate through the parasitic diode. The substrate will be at

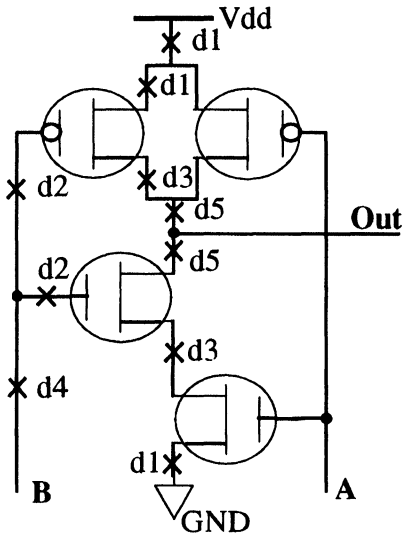

FIGURE 4 Locations of possible opens.

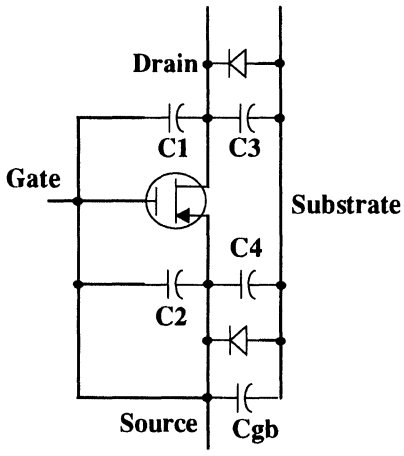

FIGURE 5 A detailed MOS transistor model.

GND for an n-channel transistor and at Vdd for a p-channel transistor. The time in which this parasitic diode can change the voltage level at the drain when the transistor is on depends on many process parameters [15]. An open gate (d2) in Figure 4, can be capacitively coupled to the drain, source, or substrate of the transistor, as well as to other signal paths in the circuit. The logic levels on these signal paths could affect the voltage level at the gate. Neglecting external capacitances, the voltage between the drain and source determines the voltage on a floating gate. If the drain to source voltage is less than the threshold voltage, the voltage at the gate is insufficient to cause the transistor to conduct (neglecting subthreshold conduction) [15].

A floating signal line that is connected to two or more gates (d4) in Figure 4 is affected by the same factors as an open gate. The voltage on both gates will be the same, but the effects may be different. Maly [15] suggests that such a defect can result in: 1) the p-channel transistor on with the n-channel transistor off, 2) the n-channel transistor on with p-channel transistor off, or 3) both transistors on.

An open drain, (d3) in Figure 4, behaves like a classic stuck-open fault. The drain can float to a voltage or be drained to the value at the source, but it is not connected to the rest of the circuit. Therefore, it behaves as though it is always off. An open that disconnects either the n-channel or p-channel network from the output (d5) behaves like a stuck-at fault. The connected network would still drive the output to Vdd or to GND which would behave as a stuck-at fault.

II.B. I_{DDQ} Testing

I_{DDQ} testing can be used to detect faults in CMOS ICs [25] [22] [24] [16] [4] [8] [7]. Consider the behavior of a general FCMOS gate as shown in Figure 6a. A typical FCMOS circuit has a pull-up network, consisting of p-channel transistors, that is responsible for bringing the output F to a logic one (high); and a pull-down network, consisting of n-channel transistors, that is the logic complement of the pull-up network. It is responsible for bringing the output F to a logic zero (low). In steady state and depending on the inputs, the output node of each FCMOS gate is connected to either the power (Vdd) bus, through the p-transistors, or to the Ground (GND) bus, through the n-transistors, but not to both Vdd and GND simultaneously. Therefore, in the steady state, there should be no path between Vdd and GND which entails that there is practically no current flow between Vdd and GND. In actuality there will be some p-n junction leakages, but the current flow should be in the nA range for an FCMOS IC. Thus I_{DDQ} can be

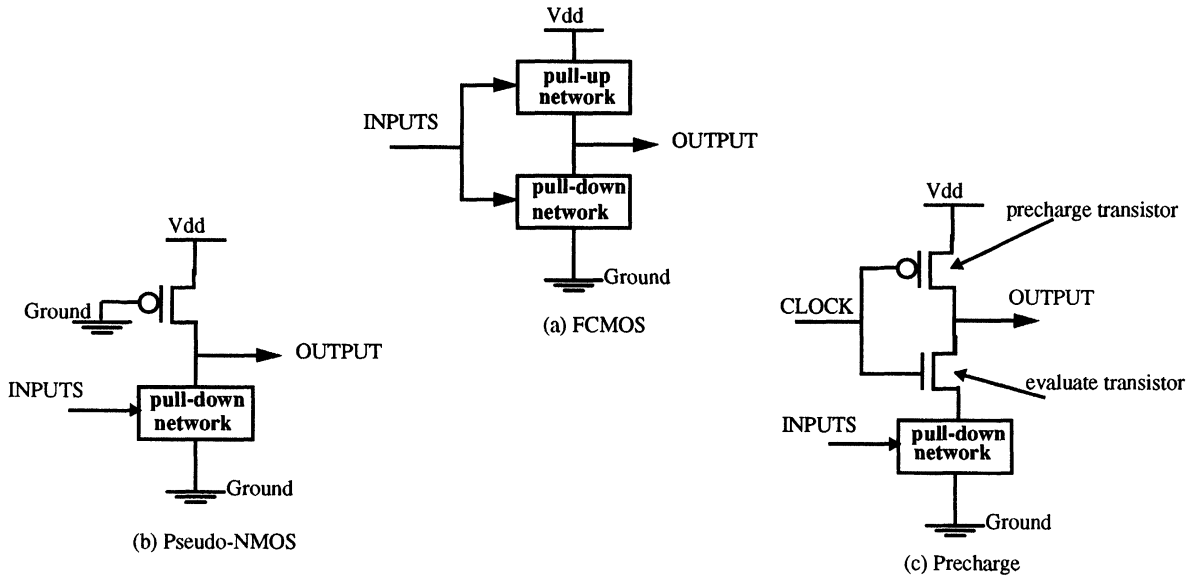

FIGURE 6 General model of logic design structures.

used to detect some types of defects that cause an elevated I_{DDQ} level, such as bridging faults and gate-oxide leakages [20] [22]. Specific test patterns have to be applied in order to manifest the effect of the defect on the magnitude of I_{DDQ}. For example, to detect an undesired short between two nodes, the applied test pattern must drive the two nodes to opposite potentials forcing an elevated I_{DDQ} current to flow. These types of defects may not be detected by stuck-at fault (SAF) testing if they cannot be modeled by the SAF model [25] [22] [24] [16] [4] [8] [7]. Other types of faults that I_{DDQ} testing can detect, where conventional logic testing may be limited, are logically redundant single SAFs and multiple SAFs.

The I_{DDQ} testing approach is mostly confined to CMOS structures, where the properties of the quiescent current can be deployed to expose defects. Circuits fabricated with other technologies such as NMOS or TTL may allow a normal path between power and ground that may render a current test technique ineffective. In addition, this testing approach is inherently slow due to parasitic capacitances which delay the settling of the current to its steady state value.

The limitations described above are being addressed by researchers. For example, built-in current testing methods have been proposed [13] that will improve the testing speed and resolution. Also, it is anticipated that a new generation of Automatic Test Equipment (ATE) will make I_{DDQ} testing more feasible. Other studies have incorporated I_{DDQ} testing to the testing of Hybrid systems [2] and TTL technology [5] using statistical signal processing techniques.

III. I_{DDQ} MEASUREMENTS OF CMOS CIRCUITS

Figures 6a, 6b, and 6c show the general structure of FCMOS, pseudo-NMOS, and precharge logic respectively. The previous section delineates the use of I_{DDQ} for FCMOS designs. In a pseudo-NMOS circuit, a path exists between Vdd and GND any time the pull-down network is asserted which results in an elevated I_{DDQ}. However, some open faults can break the path from Vdd to GND so that no significant I_{DDQ} can be recorded and the open defect is detected.

However, bridging defects are more difficult to detect in pseudo-NMOS because of the continuous path between Vdd and GND. In the case of precharge logic, the precharge and evaluate transistors (see Fig 6) are never asserted at the same time. A defect may or may not be detected depending on the defect type and its location in the precharge logic circuit. In this section we describe the design of an experiment that will qualify the types and locations of defects that may/may not be detected by I_{DDQ} testing for the above design logic styles. We also describe the design of an experiment to better qualify the use of I_{DDQ} testing in a production type environment. The results of these experiments will be analyzed in section IV.

III.A. Experiment 1

The goal of this work is to examine the effect that defects have on the quiescent power supply current for design methodologies other than FCMOS. It was decided early on that the circuit to be used to study these effects should be a fairly simple and standard circuit. As a result, we employed a half-adder circuit. This section first details the overall design of the FCMOS, pseudo-NMOS, and precharge circuits. This is followed by a discussion on the choice of defects that were implemented in the circuits. It should be noted that all circuits were simulated using Spice and were fabricated using MOSIS 2 um n-well CMOS process technology.

Overall Design

The ICs were designed in FCMOS logic, pseudo-NMOS logic, and precharge logic. For each IC design, four copies were fabricated and tested. The ICs were packaged in the MOSIS 40-pin TinyChip pad frame. Each chip contains 24 half-adders (except for the precharge which contains 23) organized into three groups of eight. Within each of these groups, one circuit is defect-free while each of the remaining half-adder circuits contains a single defect. Each half-adder circuit on the IC required a separate power supply so that the quiescent power supply current resulting from the defect within that circuit could be monitored in isolation. In addition to a "Vdd" pin, each half-adder required two inputs (A and B), two outputs (Sum and Carry) and a GND connection. The GND was common to all points on the fabricated IC.

The inputs and outputs were shared among the half-adder circuits. This was accomplished by using a transmission gate powered by each half-adder's Vdd (Vdd1, Vdd2, etc. in Figure 7) as shown in Figure 7. The transmission gates as well as other supporting circuitry such as input/output buffers are powered by the IC's main Vdd, and not by any half-adder's Vdd. Therefore, only one of the eight half-adders is powered-up at any time so as to ensure no interference between the supporting circuitry and those under test.

Built-in Defects

As mentioned earlier, each group of circuits contained one defect-free circuit to use as a benchmark for the defective circuits within that group. The defects implemented are intended to be reflective of the possible defects that could occur, hence, there is roughly one third bridging defects, one third gate oxide shorts, and one third open defects, for a total of 68.

Bridging Defects and Gate Oxide Shorts

The resistance of the bridging defects and gate oxide shorts ranged from negligible resistance to 500 kilo-ohms. The 500 kilo-ohm resistance was used as a gate oxide short in an FCMOS circuit in order to test the upper limit of detecting an I_{DDQ} defect. The design of a gate oxide short with a given resistance is shown in Figure 8. For a bridging defect of negligible resistance, the shorted nodes were connected by metal.

Open Defects

About a third of the open defects is floating gates while the remaining two thirds are floating sources. Spice simulation indicated that, under some conditions, a floating transistors' source can still operate

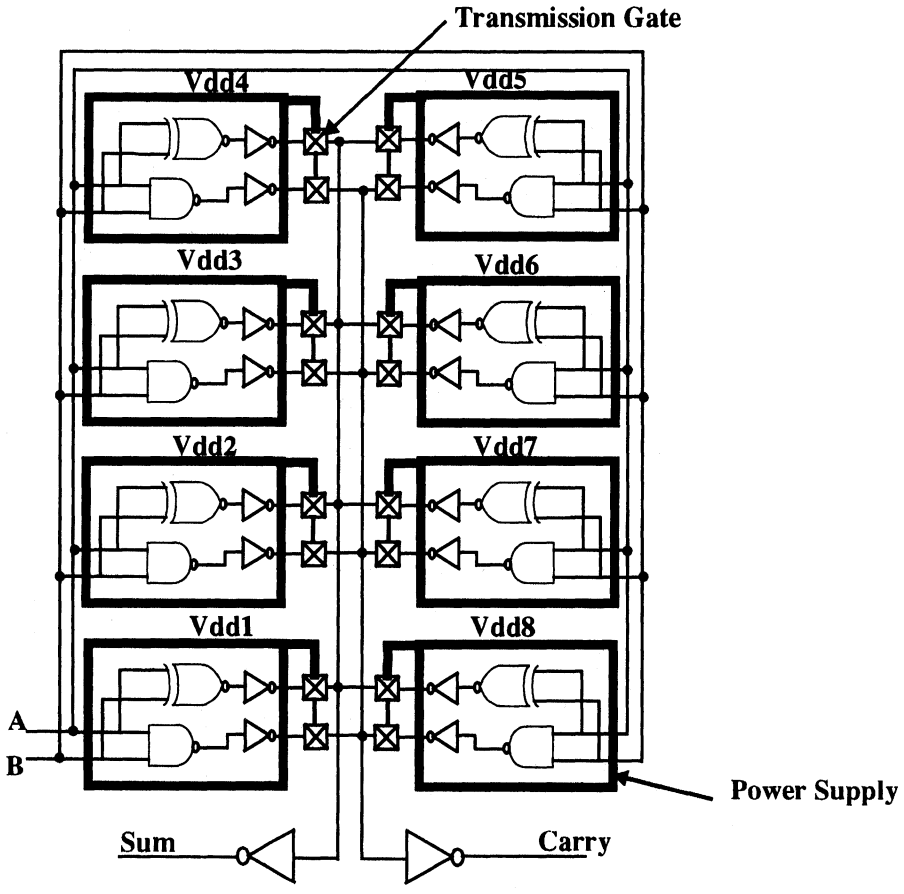

FIGURE 7 Schematic of the half-adder chip.

normally under some input conditions. The Spice model used for an open defect is a capacitor between the node connected to the main circuit, and the substrate. A 100 mega-ohm resistor was placed in parallel with the capacitor to get Spice convergence. The capacitance at the floating nodes for the open defects was incidental (a function of the layout), except for two FCMOS circuits. A 0.1 picofarad capacitor was designed placed between the floating gate at the B input-controlled n-channel transistor for the AND gate (see Figure 9) and the A input. A 0.01 picofarad capacitor was placed between the Carry output and the input to the EXOR inverter. These capacitances were used to examine the effect that a large floating connection line would have on the circuit. The capacitors were designed by placing a large square area of metal-one over a larger square area of polysilicon. The capacitance is determined by the area of metal-one. The reason for making the polysilicon area larger than the metal one area is to ensure that normal alignment tolerances in fabrication would not affect the capacitor. The 0.1 picofarad capacitor was 2250

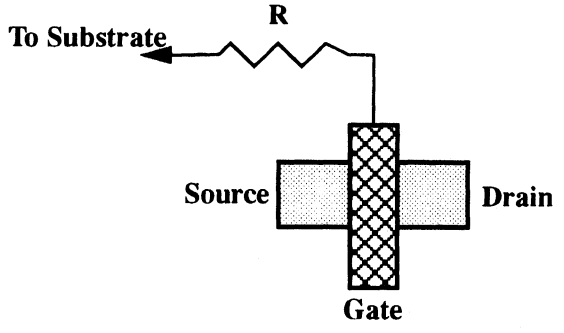

FIGURE 8 Mechanism for bridging defects and gate oxide shorts.

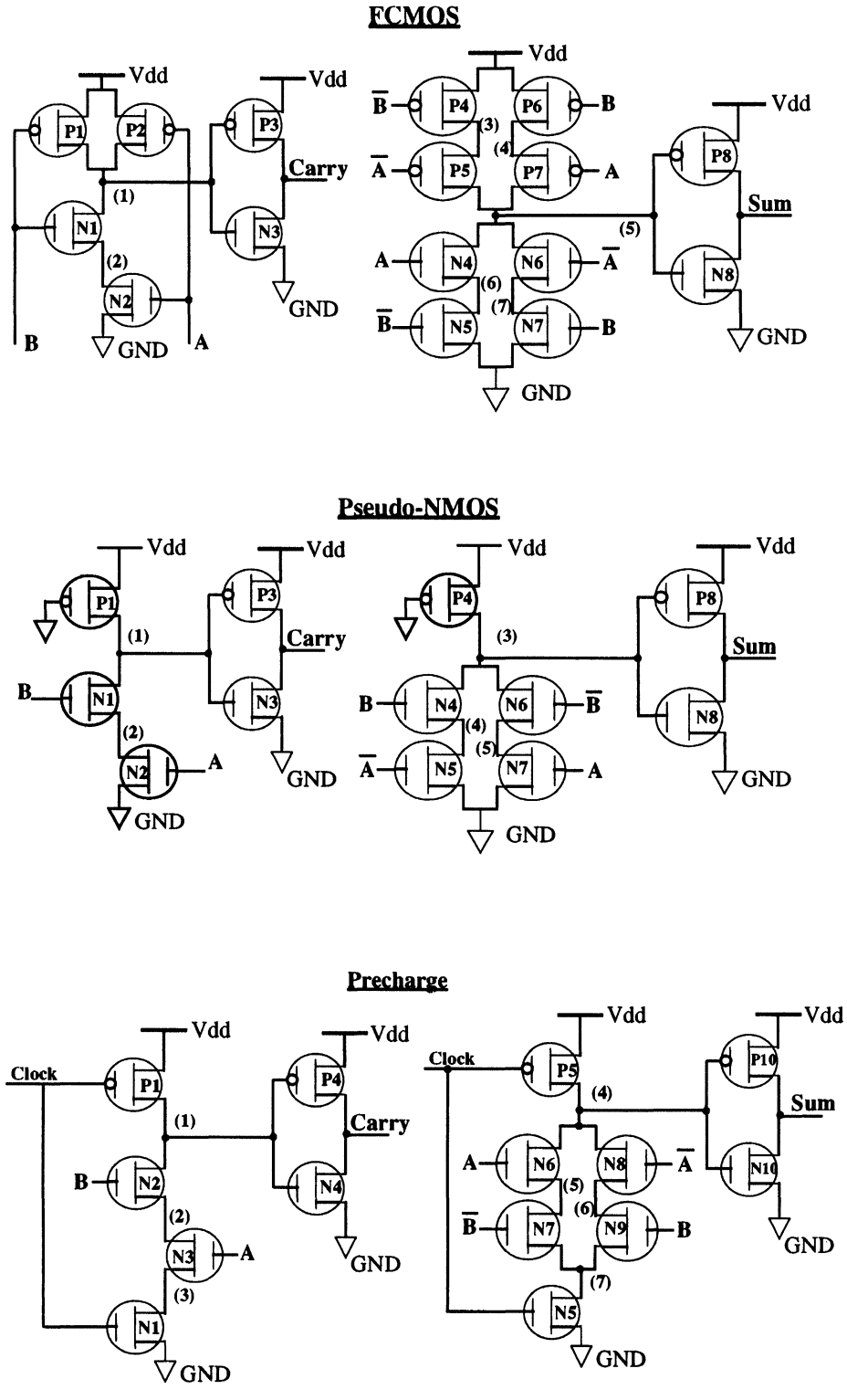

FIGURE 9 A half-adder circuit in different design techniques.

square microns while the 0.01 picofarad capacitor was 220 square microns.

Testing Equipment

The Hewlett-Packard 81810S IC Design Verification System was used to physically test the fabricated ICs. The circuit inputs were supplied by HP8180A Data Generator with the circuit's main power supply being supplied by an HP6624A System Power Supply and the output voltages being monitored by an HP4142 DC Source/Monitor Unit. In addition, power for the sub-circuits under test was supplied by the HP4142 while the current supplied to the circuit was being monitored. Each current measurement required at least sixty microseconds to perform.

III.B. Experiment 2

The second experiment focuses on two issues. First, we study the effectiveness of I_{DDQ} testing in improving fault coverage of IC chips with respect to stuck-at testing in a production-type environment. Second, we examine the effects of thermal stress on I_{DDQ} testing in order to investigate the effectiveness of I_{DDQ} in detecting latent defects. In this study, two CMOS IC parts were chosen as test vehicles: a National Semiconductor 74HC00 quad, 2-input NAND was chosen as an example of a simple combinational CMOS circuit while a HM6264, 8kx8 SRAM was used as an example of a more complex CMOS circuit. The tested IC chips were selected from the production line in the IBM-Charlotte card assembly plant. Some of these chips were identified as faulty during production testing.

An experiment was set up with the purpose of studying "process-like" defects by inducing them in good SRAMs and NAND packaged chips. The effects of the induced defects were exposed and characterized by measuring the current and voltage response while the device under test was being stimulated. First, a continuity test was applied to all chips. This procedure, in effect, curve traces each chip pin and compares it to its corresponding trace of a "*golden*" chip. By varying the applied voltage form -2 volts to $+2$ volts while forcing a current, an I-V curve of each pin is obtained. This procedure will expose any short or open input/output pins or contact deficiencies. This test was performed using the UTI-80 auto curve tracer. The second stage of testing was performed on a computer-based single-module tester. This tester can stimulate a chip with predefined input patterns and verify the correctness of the outputs' voltage response. This setup was used for the purpose of logic (voltage) testing.

An HP-2342A Multimeter was integrated into the test system and the software was altered accordingly to enable current measurements. The multimeter was configured to take D.C. current measurements upon the receipt of a trigger. Current measurements were taken at the maximum supply voltage (Vdd) allowed for the chip as recommended by Hawkins *et al.* [4] to ensure the detection of defects that have strong nonlinear characteristics.

Defect Generation

In order to emulate the effect of some of the earlier mentioned defects, a defect induction method was devised and applied on two different CMOS IC parts (NANDs and SRAMs). First, the operation of each chip under test (CUT) was functionally verified. Next, the CUT was etched open using a chemical jet-etching device that applies a stream of a hot acid (about 230 °c) onto the surface of the packaged chip. After thoroughly cleansing the etched chip by pressured air and water, the functionality of the chip was verified again (voltage testing only) to eliminate any "dead chips" and save upcoming testing efforts. In the following step, defects were induced to each etched chip.

Two methods were used to insert defects in this experiment. In the first method, a Xenon laser beam focused to micro-accuracy was used to create a cavity in the diffusion with the aid of a microscope. Different locations can be selected to induce opens. In the second method, a "Micromanipulator" station was

used. This station uses a micro-probe, 5 micrometers, to probe the surface of the chip and is capable of creating a short between any two tracks, or nodes, by smearing across the tracks horizontally. A short can be verified by means of either probing the two shorted nodes with the aid of an oscilloscope or by taking a close-up photograph of the defective area. Conversely, an open circuit can be produced using this method of defect induction. Following the induction of a defect, each chip underwent an extensive voltage and current monitoring test.

Test Method

For the NAND chips (quad 2-input gates), 2^8 (256) test patterns were applied to exhaustively test the chip and rule-out any interactions between the different NAND gates on the chip. The voltage response of each chip was compared to the fault-free chip response and current measurements (1 reading per pattern) were taken. To characterize the current response, the mean and standard deviation were calculated assuming that the current measurements followed a Normal (Gaussian) distribution. An I_{DDQ} value was considered abnormal only if both of the following conditions were met:

1. An I_{DDQ} measurement must deviate by more than three standard deviations from the mean value;
2. it must be different from that of the corresponding golden-chip value.

The assumption that the measurements followed a Normal distribution is justified by the Central Limit Theory. The Central Limit Theory states that for a large sample size, the mean of a sample possesses a sampling distribution that is approximately Normal regardless of the probability distribution of the sampled population. For a reasonable approximation, a sample size of 30 is needed [11], in our case the sample size was 256. The current measurements were taken under the maximum allowed voltage of 6 volts.

The SRAM requires a special testing program. For voltage testing, the well known checkerboard pattern was used. Simply described, the checkerboard algorithm requires the writing of an alternating pattern of logic 1's and 0's to physically adjacent cells. Then, the tester reads out each address and verifies its contents. However, for current testing purposes a different approach was used. The measurement cycle was initiated by writing an all-zero pattern to all addresses while taking a current reading per address. Next, the read cycle was initiated followed with a current measurement at every address. The measurements were taken for write/read all zeroes and again for a write/read all ones. The chip's current signature consisted of a total of 32,368 current measurements. This I_{DDQ} testing procedure of writing and reading logic 0's and 1's to all cells in the memory matrix is sufficient to detect any abnormal current [9] and [17]. The standard deviation and overall mean were calculated for each of the four measurement cycles. This was used to provide an index of failure. Assuming a Normal distribution, any data point (a current measurement) that deviates by more than 3 sigma (standard deviation) on either side from the mean, is flagged as an abnormal value only if it did not agree with the corresponding golden chip value.

The final stage of this testing effort involved *burn-in*. A card was designed with a capacity of 16 chips (see Figure 10) that was later placed in an environmental-stress chamber, by Standard Environment System-TB/2, where the temperature was cycled over a hundred degrees centigrade range while the chips were being stimulated under voltage stress. The card could be stimulated by the 13-bit address generator

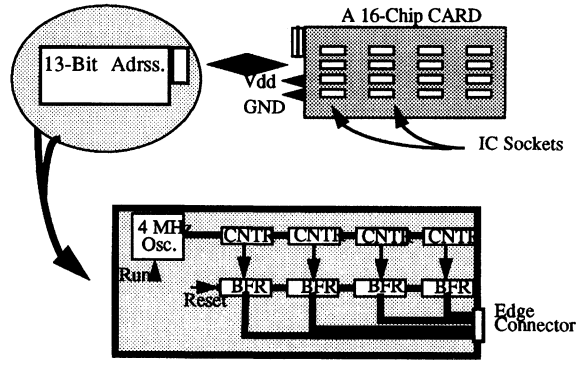

FIGURE 10 Schematic of the card used for burn-in testing.

which consists of four 4-bit counters (CNTR) running at 4MHz, and four 4-bit buffers (BFR) providing addresses for all of the 16 chips (Figure 10).

IV. EXPERIMENTAL RESULTS AND ANALYSIS

In this section, we analyze the results of the two experiments discussed in the previous section.

IV.A. Results of Experiment 1

A summary of the testing results is given in Tables I–IV. The row labeled "Voltage" lists the number of defects for each design type that produced voltage-detectable logic faults. The row labeled "Voltage Only" lists the number of defects that was detected by voltage testing that could not be detected by current testing. The explanations for the rows labeled "Current" and "Current Only" are similar. A fault is said to be detectable by I_{DDQ} testing if the good circuit I_{DDQ} level is measurably different than the faulty circuit I_{DDQ} level. For example, in the cases of FCMOS and precharge logic, good circuit I_{DDQ} is in the nA range while faulty circuit I_{DDQ} is in the uA range. In the case of pseudo-NMOS, depending on the input pattern, the good circuit I_{DDQ} can be in the nA or uA range. Tables V–VII show the ranges of I_{DDQ} for circuits that failed the I_{DDQ} test. For example, the first row/column of Table V specifies that for the 0 ohm bridge defect and depending on the location of the defect, the measured I_{DDQ} was as low as 275 micro-Amps for one bridge location and as high as 547 micro-Amps for another.

TABLE I Summary of detections of bridging defects

	FCMOS	Pseudo-NMOS	Precharge
Voltage	1	2	5
Current	9	12	7
Voltage Only	0	0	2
Current Only	8	10	4
Total # of Bridges	**9**	**12**	**9**

TABLE II Summary of detections of gate oxide shorts

	FCMOS	Pseudo-NMOS	Precharge
Voltage	0	0	1
Current	6	4	5
Voltage Only	0	0	0
Current Only	6	4	4
Undetectable	0	1	0
Total # of Shorts	**6**	**5**	**5**

TABLE III Summary of detections of open defects

	FCMOS	Pseudo-NMOS	Precharge
Voltage	6	6	7
Current	3	6	3
Voltage Only	4	0	5
Current Only	1	0	1
Undetectable	1	0	0
Total # of Opens	**8**	**6**	**8**

TABLE IV Overall summary of detected defects

		FCMOS	Pseudo-NMOS	Precharge
Physical	Voltage	7	8	13
Testing:	Current	18	22	15
	Voltage Only	4	0	7
	Current Only	15	14	9
	Undetectable	1	1	0
Spice	Voltage	4	7	10
Testing:	Current	18	19	16
	Voltage Only	1	1	6
	Current Only	15	13	12
	Undetectable	4	3	0
Total # of Faulty Circuits		**23**	**23**	**22**

The often wide range of I_{DDQ} values in these tables is partly due to the fact that the defects were placed at different locations in the circuit.

Bridging Defects

There were nine bridging defects inserted into the FCMOS half-adder design, twelve in the pseudo-NMOS design, and nine in the precharge design. A summary of the testing results is given in Table I. The majority of the bridging defects were detected by current testing. However, voltage testing only detected one defect in FCMOS, a direct short across an inverter. This defect was detected by voltage testing in the pseudo-NMOS circuits, as well as in the pre-

TABLE V FCMOS logic faulty IDDQ ranges in micro-amps

Bridge	Gate-oxide short	Drain/Source Open	Gate Open
for 0 Ohm; 275–547 for 60 Kilo Ohm; 20–89	for 60 Kilo Ohm; 3–88 for 500 Kilo Ohm; 8–9	none	126–338

TABLE VI Pseudo-NMOS logic IDDQ ranges in micro-amps

Bridge	Gate-oxide short	Drain/Source Open	Gate Open
for 0 Ohm; 239–573 for 30 Kilo Ohm; 158–418 for 60 Kilo Ohm; 81–345 for 90 Kilo Ohm; 49–314	for 30 Kilo Ohm; 242–273 for 60 Kilo Ohm; 84–347	246–370	7–406

charge circuits. In addition, a direct short between nodes 4 and 5 (see Figure 9) was detected by voltage testing in the pseudo-NMOS design. The remainder of the bridging faults in FCMOS and pseudo-NMOS were not detectable with voltage testing due to the high resistance of the bridges. The precharge design had five bridging defects that were detected by voltage testing, three of which were direct shorts and the rest were 60 kilo-ohms. Two of the bridges detected by voltage testing did not cause an elevated power supply current and, thus, were not detected by current testing. Both were bridges between nodes of the n-channel evaluation logic. The reason they did not create an I_{DDQ} fault was due to the fact that the path from Vdd to GND for a precharge design is controlled by the clock. When the clock is low, the p-channel transistor allows the evaluation node to charge to five volts. However, when the clock goes high, the evaluation node is cut off from Vdd and will discharge to zero volts if the n-channel logic, the n-channel transistor that is controlled by the clock, forms a path to GND. Though the two shorts bypassed normally-off transistors, they did not form a continuous path from Vdd to GND and thus did not register an elevated I_{DDQ}.

Gate Oxide Shorts

Table II summarizes the results of physical testing on the gate oxide shorts designed into the half-adder circuits. There were six gate oxide shorts implemented in the FCMOS half-adder design, five in pseudo-NMOS, and five in precharge. One of the precharge circuits had a high resistance bridge between the evaluation node 1 and GND that caused an I_{DDQ} fault as well as a logic fault.

Open Defects

There were eight open defects designed in the FCMOS half-adder design, six in the pseudo-NMOS half-adder design, and eight in the precharge half-

TABLE VII Precharge logic IDDQ ranges in micro-amps

Bridge	Gate-oxide short	Drain/Source Open	Gate Open
for 0 Ohm; 165–314 for 60 Kilo Ohm; 35–184 for 120 Kilo Ohm; 37–193	for 60 Kilo Ohm; 72–83 for 120 Kilo Ohm; 44–324	none	146–254

adder design. The results of physical voltage and current tests on the defective circuits are summarized in Table III. In the case of FCMOS, the only undetectable open defect was an open source for transistor P5 (see Fig. 9). The defect affected the circuit on each of the four chips differently. Apparently, the transistor with the open source (P5) had differing rates of leakage to the substrate for each of the four chips. The remaining open sources (or open drains) for FCMOS half-adders caused logic faults, but did not cause I_{DDQ} faults. All but one of the floating gate defects for FCMOS were detected by current testing. This defect was designed with a 0.1 picofarad capacitor connected between the floating gate at transistor N1 and the A input (see Figure 9). The effect of this capacitor was to keep transistor N1 completely shut off. The rest of the floating gates defects caused a transistor to partially conduct, thus causing an elevated current with at least one of the four input patterns.

All of the open defects in the pseudo-NMOS circuits were detected by both current testing and voltage testing. The open sources caused I_{DDQ} faults, detected not by an increase but by a decrease in the power supply current. Three of the four possible input patterns for the pseudo-NMOS half-adders caused a normal quiescent power supply current of approximately 250 micro-amps. However, the open source defects caused the normal path from Vdd to GND to be broken which resulted in a faulty nano-amp I_{DDQ}. The floating gate defects for the pseudo-NMOS design all caused increased I_{DDQ}.

All of the half-adder circuits for the precharge design with floating gates caused I_{DDQ} faults, in addition to logic faults. All of the circuits with open source defects caused logic faults.

Table IV provides an overall summary of this experiment and compares the simulation results with the actual test results. In comparing the simulation results with the experimental results, we found that in the case of bridge defects, Spice results, although not accurate, were within the general range of experimental measurements. In the case of some open defects, Spice was unreliable. For example, for some opens, Spice gave I_{DDQ} values as high as 300 micro-Amps when in fact the actual I_{DDQ} readings were in the nano-Amp range. For some opens, Spice also gave incorrect results for the voltage tests.

IV.B. Results of Experiment 2

We will first examine the results of the NAND chips' tests followed by the SRAM chips' test.

NAND Results

The logic (voltage) test and the I_{DDQ} test were conducted before and after defect induction to verify functionality. The results of voltage and current tests are summarized in Table VIII, where a "P" indicates that the chip passed the test, and "F" indicates that it failed (herein "failed a test" implies a detection). To investigate the effect of voltage stress, all of the 16 NAND chips were subjected to the same voltage test but at 6 volts. The results were compared to the normal 5 volts test. No discrepancies were found between the results of the two tests, i.e. both the 5 and 6 volts tests flagged the same test pattern results as being bad.

TABLE VIII NAND results

Func P/F	iDD P/F	Test Remarks
F	F	low IDDQ
P	F	low IDDQ
F	F	high IDDQ
F	F	high IDDQ
F	F	hi/lo IDDQ
F	F	high IDDQ
F	F	low IDDQ
F	F	high IDDQ
F	F	low IDDQ
P	F	high IDDQ
F	F	high IDDQ
F	F	high IDDQ
F	F	high IDDQ
F	F	high IDDQ
P	F	low IDDQ
F	F	high IDDQ

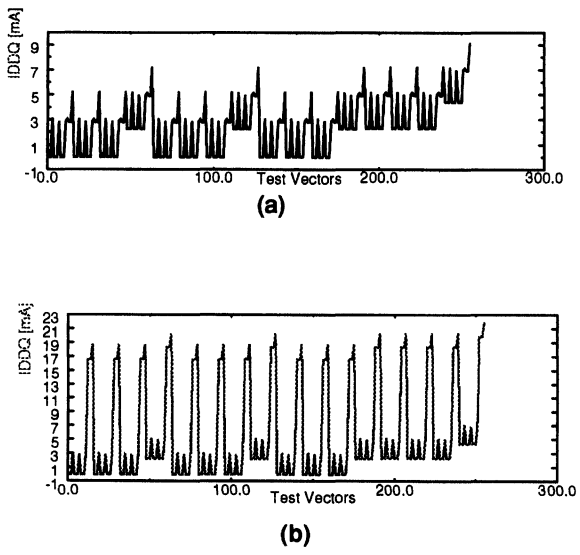

FIGURE 11 An example of a NAND chip before/after defect insertion.

An example of the current response of a NAND chip before and after defect induction can be found in figures 11 and 12. In fig.11-a, the normal average current is 2.505 mA, while in fig. 11-b the average is 5.86 mA which is indicative of a defect. In addition, the two graphs a and b are clearly different, in form and magnitude, thus suggesting a faulty chip. Figure 12 shows more of the same deviant behavior experienced by defective NAND chips where the normal current average prior to defect insertion is 2.4 mA whereas it shot to 14 mA after defect induction.

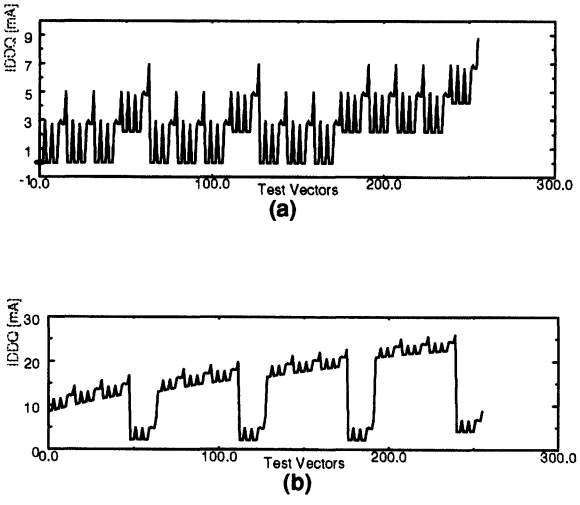

FIGURE 12 Another example of a NAND chip before/after defect insertion.

SRAM Results

The current test yielded four sets of current measurements in the following order, write-zero cycle (w0), read-zero (r0), write-one (w1), and read-one (r1). The I_{DDQ} test failures were either with the current readings exceeding a high or a low current limit—not to be confused with the absolute minimum or maximum current—or with the measurements falling within the range but being inconsistent with the expected normal reading. The golden chips average-I_{DDQ} current ranges for the four cycles were as follows (herein, a 7 volt supply was used):

I_{w0} (quiescent current resulting from w0): 2.9–3.4 milliamperes

I_{r0} (quiescent current resulting from r0): 3.0–3.5 milliamperes

I_{w1} (quiescent current resulting from w1): 3.9–4.6 milliamperes

I_{r1} (quiescent current resulting from r1): 3.0–3.5 milliamperes

The following relations were shown experimentally to hold true for a good SRAM chip:

$$I_{w0} < I_{r0},\ I_{w1} > I_{r1},\ I_{w1} \cong I_{w0} + 1mA,\ and\ I_{r1} \cong I_{r0}$$

The above current ranges may be considered high for a CMOS chip and it can be argued that such high current may in fact mask out small current variations that may be indicative of a defect. This "high" quiescent current was ascribed to the sense amplifiers and other non-CMOS circuitry that inherently consume more current. To magnify the effect of a fault, new data was generated by finding the difference between some measurement cycles. The new data consists of:

$(I_{r0} - I_{w0})$ with a mean around 0.1 mA; $(I_{w1} - I_{w0})$ with a mean around 1 mA;

$(I_{r1} - I_{r0})$ with a mean around zero; and $(I_{w1} - I_{r1})$ with a mean around 1mA.

This new data amplifies I_{DDQ} anomalies in some cases wherein a spike (dip) may be interpreted as an abnormal current value indicating a faulty chip. However, it should be noted that this approach may mask the effects of some faults. Nonetheless, this method can help in cases where the absolute current signature alone reveals no peculiarities. In this study, we considered both the absolute current value and the above difference method. In a production environment, this difference method requires test equipment that can perform simple mathematical operations such as subtraction and can detect maximum or minimum limits on measurements. A summary of the results is found in Table IX. All chips failed one type of test and the majority failed both logic and current tests. One chip failed the voltage but passed the current test. Alternatively, one chip failed the current test and passed the voltage test. Some defects that were not detected at the nominal supply voltage of 5 volts were exposed when the supply was increased to 7 volts (the maximum allowed level).

It was found that many SRAM cells (i.e. addresses) failed the I_{DDQ} test but passed the logic test. However, the comparison did not reveal a case where addresses passed I_{DDQ} test and failed the logic test. All SRAMs were tested at 5 volts and also at 7 volts.

TABLE IX SRAM results

Func P/F	Iddq P/F	Test (2 ptrn) Remarks
F	F	high Iddq
F	F	high Iddq
F	F	high Iddq
F	F	diff. spike
P	F	ladrss spike
F	F	high Iddq
F	F	high Iddq
F	F	high Iddq
F	P	----------
F	F	high Iddq
F	F	high Iddq
P	F	diff. spikes
F	F	high Iddq
F	F	high Iddq
F	F	high Iddq

It was noticed that in two cases, the 7 volts test detected more failing addresses than the 5 volts test. In one case, the 5 volts test detected only 32 faulty addresses while 2000 bad addresses were detected by the 7 volts test. Incidently, those bad addresses were detected through the current response in both cases. An overall summary of the logic and current results of both NAND/SRAM chips is found in Table X.

The signature of a SRAM chip consists of the four main measurement cycles: write-0, read-0, write-1, read-1 which are superimposed on each other, and another four cycles that were generated by taking the difference of two main cycles. In several cases, abnormal current values where discovered only when the difference between two main cycles was found, even though the mean of every cycle was within normal range. Examples of SRAM I_{DDQ} response are presented in figures 13 and 14. Figure 13 clearly depicts many current spikes in the difference r0-w0 cycles peaking at 25 mA. Also, figure 14 demonstrates similar properties where the faulty response is distinctly different from the fault-free response. As a reminder, each plot consists of 8192 current measurements per cycle as described earlier.

Burn-in results

As discussed earlier, a special card was designed and an environmental stress chamber was programmed to thermally stress the chips. In addition, extra circuitry provided stimuli to the chips. After this stressing effort, both the logic and current tests were repeated. In this study, the effect of burn-in on I_{DDQ} response was examined. The current response recorded before and after burn-in, performed on fault free SRAM/NAND chips, showed burn-in stress to have a minimal effect on I_{DDQ} response. The current response appeared to be shifted upwards or downwards within 10 microamperes but still preserved its normal pre-burn-in response. An exception to the above observation was the case with one NAND. Initially this chip failed the logic test and I_{DDQ} test. After burn-in, the chip seemed to have recovered and passed the logic test but still failed the current test although it was noticed

TABLE X Summary of results

TEST TYPE	NAND	% Detected	SRAM	% Detected	Totals NAND and SRAM	% Detected
failed Iddq only	3	19%	2	13%	5	16%
failed logic only	0	0%	1	6.7%	1	3%
Failed Iddq	16	100%	14	93%	30	96.7%
Failed logic	13	81%	13	87%	26	83.8%
Total tested	16	—	15	—	31	—

that its I_{DDQ} average dropped to 50% of its initial value. This healing phenomenon was also observed with SRAMs when the logic test (at 5 volts) was conducted after a current test (at 7 volts). Bake-recoverable IC failures are caused by charge instabilities and parasitic capacitance that lead to inconsistent logic values which propagate as erroneous logic outputs. It is theorized that the induced defects have created defective p-n junctions and parasitic leakages which may have led to the "healing" phenomena. This behavior was also reported by Sandia laboratory and other IC fabrication facilities [22].

V. CONCLUSIONS

In this paper, the results of two studies were presented. The first study involved an assessment of I_{DDQ} testing for different types of logic design styles including pseudo-NMOS and precharge logic. The study involved the design, simulation, fabrication, and testing of ICs with built-in defects. The results show that many faults that escaped logic stuck-at testing were detected by I_{DDQ} testing for each of the design styles that were considered. The second study involved the use of ICs in a production environment.

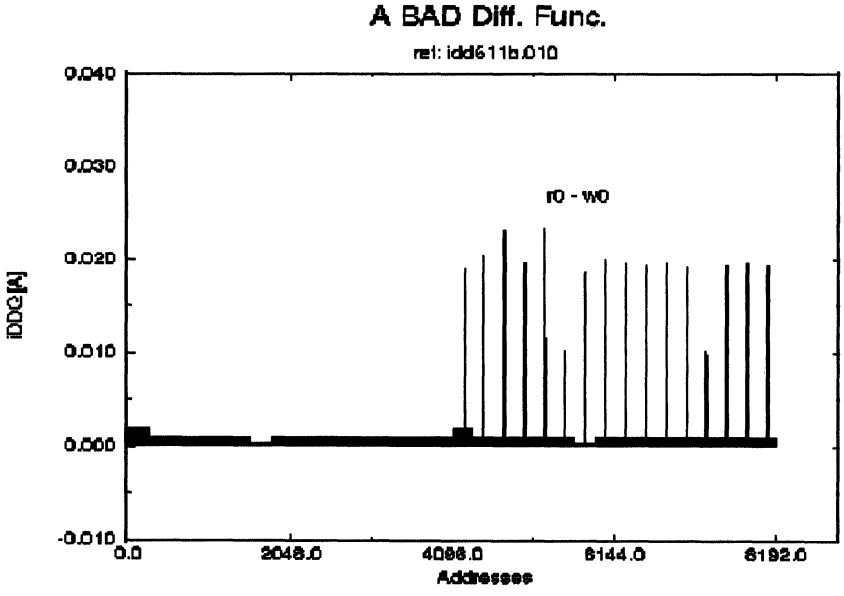

FIGURE 13 An example of a faulty SRAM chip detected from the difference of ($I_{r0} - I_{w0}$) data.

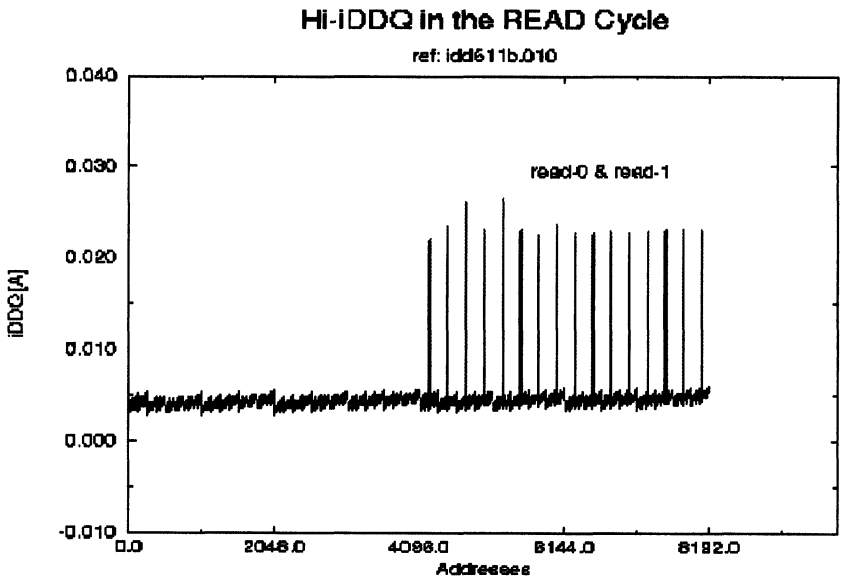

FIGURE 14 An example of a faulty SRAM chip detected from the Ir0 and Ir1 data.

It was shown (see Table X) that 96.7% of all induced defects in this second study were detected by I_{DDQ} testing while 83.8% were detected by stuck-at testing.

At face value alone, the above results would seem rather encouraging as far as the applicability of I_{DDQ} in non-FCMOS structures such as pseudo-NMOS. Unfortunately, in order for this test method to be practical in non-FCMOS structures, extensive partitioning may have to be performed. For example in the case of detecting opens in pseudo-NMOS circuits, a test pattern must be found that establishes a Vdd to GND path (turn on the pull-down network) only in the gate under test and cut off I_{DDQ} contributions from other gates in the circuit. Finding such a pattern is not always possible, and thus circuit partitioning may have to be deployed. The resulting circuit overhead may be unacceptable depending on the circuit size and function.

Experimentation with the effect of burn-in stressing showed no significant effect on the current signature. However, it did affect the consistency of the test results where some chips experienced bake-recovery and seemed to pass the logic test while failing the current test. The aim of this study was to simply assess the effect of burn-in on current signatures. Due to the relatively small sample of chips used, this study cannot be used to establish I_{DDQ}'s ability in replacing burn-in as a screen of latent defects. Furthermore, such studies would have to include latent-type defects that are usually detected by burn-in. It is postulated, however, that with a bigger sample size and latent defect induction, I_{DDQ} testing can assess, and may in special cases substitute for, burn-in for detecting reliability defects.

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