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Design of CMOS PSCD Circuits and Checkers for Stuck-At and Stuck-On Faults

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We present in this paper an approach to designing partially strongly code-disjoint (PSCD) CMOS circuits and checkers, considering transistor stuck-on faults in addition to gate-level stuck-at faults. Our design-for-testability (DFT) technique requires only a small number of extra transistors for monitoring abnormal static currents, coupled with a simple clocking scheme, to detect the stuck-on faults concurrently. The DFT circuitry not only can detect the faults in the functional circuit but also can detect or tolerate faults in itself, making it a good candidate for checker design. Switch and circuit level simulations were performed on a sample circuit, and a sample 4-out-of-8 code checker chip using the proposed technique has been designed, fabricated, and tested, showing the correctness of the method. Performance penalty is reduced by a novel BiCMOS checker circuit.

Keywords: Bridging fault, Built-in current sensor, Built-in testing, CMOS integrated circuit, Concurrent error detection, Integrated circuit testing, Strongly code-disjoint checker, Stuck-at fault, Stuck-on fault, Totally self-checking checker

1. INTRODUCTION

Investigation of totally self-checking (TSC) checkers dates back at least as far as 1968[1]. Classical gate-level single stuck-at fault model has been adopted by most researchers ever since. Because the CMOS technology has become the major VLSI technology, it is necessary to revise the theory (assumptions and conditions) on totally self-checking; circuits and checkers in order to facilitate reliable computing[2]. Fault models especially are among the targets. For example, a combinational CMOS circuit may be turned into a sequential one by a stuck-open fault, which apparently cannot be modeled by a stuck-at fault. Results have been presented on the design of CMOS circuits in which single stuck-open faults are detectable by robust tests[3]. Study of various on-line checkers for switch-level circuits also has been raised due to the prevalence of the CMOS technology (see, e.g.,[4–10]), with stuck-on faults on fully complementary gates still relatively untouched[11].

Methods have been proposed towards realizing reliable checkers in CMOS circuits. If the checkers are realized using only CMOS domino gates, then they will remain self-testing for all single stuck-at and stuck-open faults, and most stuck-on faults[4]. It also was claimed that test invalidation due to

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circuit delays can be avoided in CMOS domino logic circuits[4]. In the case of dynamic domino CMOS circuits, detecting a stuck-on fault in the nMOS portion of any CMOS logic gate does not require current monitoring, but clocked transistors and inverters still need current monitoring for transistor stuck-on faults. In[10], a new technique for designing totally self-checking FCMOS circuits is presented. The technique also is based on domino logic. A procedure for multilevel CMOS TSC circuit design for Berger Code inputs is presented, but stuck-on faults are still not discussed[5]. The standard method of applying test inputs and observing outputs may not be applicable to detecting transistor stuck-on faults in full CMOS, and to measure steady-state currents under proper test vectors to detect these faults is currently considered the best way. Detecting stuck-on faults in CMOS circuits by I_{DDQ} monitoring has been widely reported (see, e.g.,[12–17]). However, in a system where self-checking circuits and checkers are implemented for concurrent error detection, off-chip current monitoring is not practical.

A strongly code-disjoint (SCD) built-in current sensor for CMOS self-checking circuits have been proposed recently[18]. In this paper, we also discuss concurrent detection of CMOS stuck-on and bridging faults which induce steady current flow. We first review a novel scheme of detecting transistor stuck-on faults which was proposed by Favalli, *et al.*[19]. Then the circuit is modified to fulfill the requirement of concurrent error detection, and is called the *analog fault detection* (AFD) circuit. We apply this AFD circuit to an m-out-of-$2m$ TSC checker, and show that the combined m-out-of-$2m$ checker is two-fault tolerant partially strongly code disjoint (2-FT PSCD). A simple inverter chain and a 4-out-of-8 code checker using the proposed technique are presented to justify our concurrent detection approach. Switch and circuit level simulations were performed and discussed. The 4-out-of-8 code checker chip has been designed, fabricated, and tested, showing the correctness of our method. Performance penalty reduction by the BiCMOS technology also has been proposed.

2. BASIC DEFINITIONS

Totally self-checking (TSC) checkers are checking circuits capable of detecting errors in the functional circuit as well as in the checker itself during normal operation. We denote the input code space as X, and the output code space as Y. Let $C(x)$ stand for the fault-free circuit/checker function with input x, and $C_f(x)$ for the faulty circuit/checker function at the presence of fault f which belongs to a given fault set F. The effectiveness of TSC circuits is based on two fundamental fault assumptions[20]:

1. each failure can be modeled as a member of a given fault set F;
2. faults occur one at a time, and between any two faults a sufficient time elapses so that all input codewords are applied to the circuit.

DEFINITION 1: A circuit C is *fault-secure* (FS) for a set of faults F if $\forall f \in F$, $\forall x \in X$, either $C_f(x) \notin Y$ or $C_f(x) = C(x)$.

DEFINITION 2: A circuit C is *self-testing* (ST) for a set of faults F if $\forall f \in F$, $\exists\, x \in X \ni C_f(x) \notin Y$.

DEFINITION 3: A circuit is *totally self-checking* (TSC) if it is both FS and ST.

DEFINITION 4: A circuit C is *code-disjoint* (CD) if $\forall x \in X$, $C(x) \in Y$, and $\forall \hat{x} \notin X$, $C(\hat{x}) \notin Y$.

DEFINITION 5: A circuit is a *TSC checker* if it is both TSC and CD.

Since there is no redundant fault allowed, the TSC conditions are quite stringent. It is difficult for a circuit to satisfy the TSC checker conditions, especially when we consider fault models at the switch or transistor level. An alternative condition called the *TSC goal* therefore is proposed[20]. It states that *given the fault assumptions, a TSC functional circuit under test (CUT) always produces a noncodeword (not an incorrect codeword) as the first erroneous output due to a fault in the CUT, and the fault(s) in the circuit must either be detected or*

not interfere with its capability to produce a noncode output for a noncode input from the CUT. Accordingly, a new concept was presented for functional circuits[20]:

DEFINITION 6: A circuit C is said to be *strongly fault-secure* (SFS) for a set of faults F if for every fault $f \in F$, either

a) the circuit is ST and FS (i.e., TSC), or
b) the circuit is FS, and if a new fault in F occurs, for the resulting multiple fault a) or b) is true.

It is clear that any SFS circuit achieves the TSC goal under the two fundamental fault assumptions given above. Naturally, SFS circuits are the largest class of functional circuits, with which a system may achieve the TSC goal, with respect to combinational faults. In[21], a similar definition is created for designing a checker, which is a companion of the SFS definition.

DEFINITION 7: A circuit (usually a checker) C is *strongly code-disjoint* (SCD) for a set of faults F if before the occurrence of any fault, C is CD. Furthermore, for every fault f in F, either

a) the circuit is ST, or
b) the faulty circuit always maps noncode inputs to noncode outputs, and if a new fault in F occurs, for the resulting multiple fault a) or b) is true.

SCD checkers seem to be the largest class of checkers which may achieve the TSC goal so far as combinational circuits and faults are concerned. However, in[22], an example is given where a network of SCD checkers do not achieve the TSC goal. Therefore, the largest class of checkers that achieve the TSC goal in fact is the class of *strongly self-checking checkers*[22]:

DEFINITION 8: A circuit C is *strongly self-checking* (SSC) for a set of fault F if before the occurrence of any fault, C is CD. Furthermore, for every fault f in F, either

a) the circuit is ST and FS (i.e., TSC), or
b) the circuit is FS and the faulty circuit always maps noncode inputs to noncode outputs, and if a new fault in F occurs, for the resulting multiple fault a) or b) is true.

A weaker set of conditions (i.e., partially SCD conditions) which is useful for many practical situations also was proposed[7]:

DEFINITION 8: Let k be the smallest integer such that there exists a fault sequence $f = \langle f_1, f_2, \ldots, f_k \rangle$ which makes $C_f(x)$ lose the SCD property, and no codeword can detect the multiple fault f. If C is CD and for any integer m, $1 \leq m \leq k-1$, and any fault sequence $f = \langle f_1, f_2, \ldots, f_m \rangle$, either $C_f(x)$ is CD or the fault sequence f is detectable by code inputs, then C is k-fault-tolerant partially SCD (k-FT PSCD).

3. CONCURRENT ANALOG FAULT DETECTION

Analog faults cover all types of failures giving rise to degraded electrical signals, such as voltages, under static conditions. Such a degradation may be caused by the presence of faulty conducting paths from Vdd to GND. Transistor stuck-on and bridging faults, exemplified in Fig. 1(a) and (b), respectively, are among those hard-to-detect analog faults. In Fig. 1(a), if the vector $(x_1, x_2) = (0, 1)$ is applied to the circuit, then there will be a conducting path from Vdd to GND due to the transistor stuck-on fault, indicated by a circle. This conducting path is highlighted in the figure. Consider the circuit shown in Fig. 1(b), and assume there is a bridging fault between nodes f_1 and f_2. If the vector $(x_1, x_2, x_3) = (0, 1, 1)$ is applied, then $f_1 = 1$ and $f_2 = 0$ in the fault free case. However, if the bridging fault is present, there is a conducting path (highlighted in the figure) from Vdd to GND through the pMOS network of function f_1 and the nMOS network of function f_2. Any of these conducting paths from Vdd to GND may cause the output value to be undetermined, i.e., to fall into the range (V_{OL}, V_{OH}). Therefore, detecting the analog faults concurrently will be critical to a reliable self-checking systems.

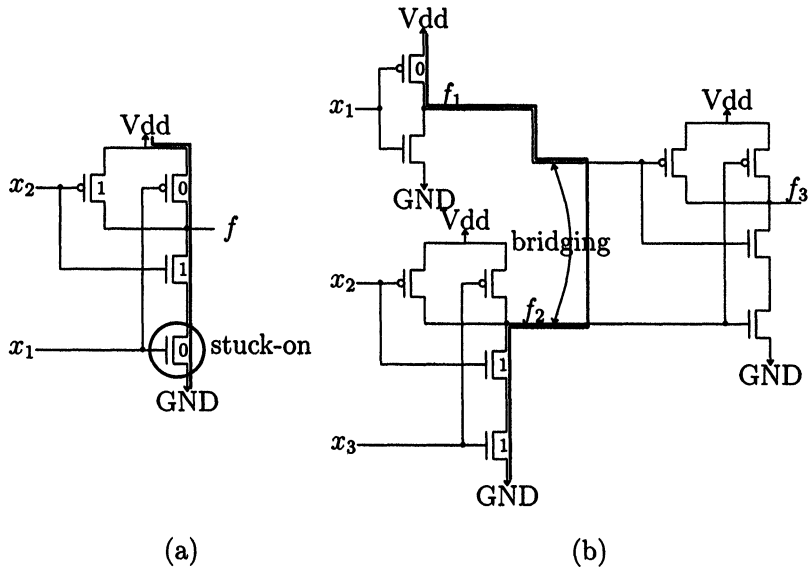


FIGURE 1 (a) A stuck-on fault example. (b) A bridging fault example.

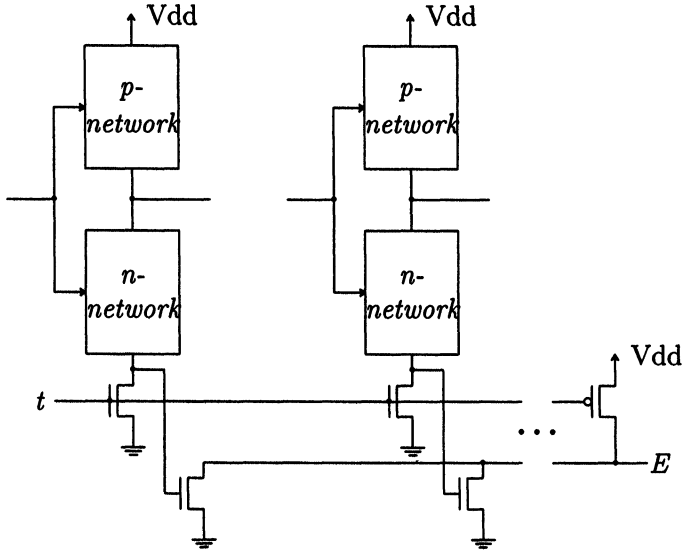


FIGURE 2 Analog fault detection circuit proposed in[19].

A design-for-testability (DFT) approach for CMOS analog fault detection is depicted in Fig. 2[19], which needs a few extra transistors to detect analog faults without using current monitoring. A revised DFT scheme for detecting analog faults for CMOS circuits was also proposed recently[23], which requires less hardware overhead.

When the control signal t is at logic 1, the circuit is in normal operation mode; when t is at logic 0 (test mode), the error signal E will indicate whether there is a fault (logic 0) or not (logic 1). Our first thought is that this DFT technique might be applied to on-line self-checking systems. However, for such a system, this scheme should be modified

to satisfy the on-line detection criterion. Fig. 3 depicts our *analog fault detection* (AFD) circuit which will be shown to satisfy the concurrent error detection requirement.

By definition, the output of a simplest TSC checker must be (1, 0) or (0, 1) in the fault-free case. The error indication signal E in the AFD circuit (Fig. 3) takes the possible values of 0 and 1 through the switches M_1 and M_4, respectively, which are controlled by a signal c_{12} (to be explained later). In fact, transistors M_1 and M_4 form an inverter in the fault-free case. When $c_{12}=1$, the AFD circuit is in normal operation mode; when $c_{12}=0$, it is in test mode (and the AFD circuit indicates whether there is an analog fault or not). Apart from the inclusion of M_4 (as compared with Fig. 2), transistors M_1, M_3, and M_4 are designed to have appropriate aspect (W/L) ratios such that the signal E will be 0 ($\sim$0 V) when one of the Vdd-GND paths (i.e., M_1–M_3 and M_1–M_4) is conducting. The influence of transistor stuck-on and stuck-open faults occurring in the AFD circuit of a TSC checker is listed in Table I. Even if M_1 is stuck on, the functional circuit will still work normally, and the AFD circuit can still detect a subsequent fault. However, there does exists a side-effect—with the signal c_{12} high, M_4 is on and the path M_1–M_4 would produce large current. There are only two faults which can not be detected by the TSC checker, and whose presence do prevent the AFD circuit from detecting faults in the functional circuit: one is the stuck-on fault in M_2, and the other is the stuck-open fault in M_3.

TABLE I Influence of faults on the AFD circuit itself

	Stuck-on	Stuck-open
M_1	undetected; no influence on checker function	E always 0 ($\sim$ 0 V)
M_2	undetected	detected by checker
M_3	E always 0 ($\sim$ 0 V)	undetected
M_4	E always 0 ($\sim$ 0 V)	E always 1 ($\sim$ 5 V)

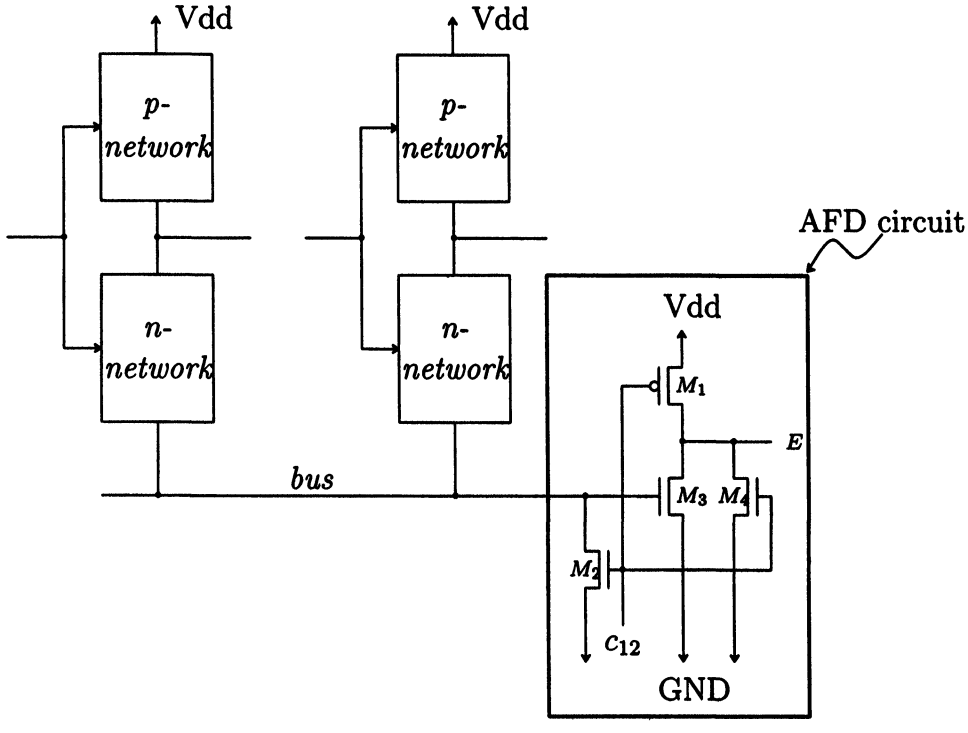


FIGURE 3 Steady-state current-detection AFD circuit.

Though the checker can not expose these faults, the presence of any of these faults does not cause the original circuit to malfunction. The checker may only lose the ability of detecting the steady-state current of the circuits which connect to the AFD circuit. Consider the situation that M_2 is stuck on (see Fig. 3), and then a subsequent stuck-on fault or bridging fault in the functional circuit occurs. This fault consequently induces a static current which can not be detected by the AFD circuit because this AFD circuit has lost its ability of detecting the steady-state current. Therefore, this checker will lose the SCD ability but still satisfy the 2-FT PSCD condition.

We can add n parallel M_3 transistors and n serial M_2 transistors to increase the fault tolerance ability, which makes the checker $(n+1)$-FT PSCD. However, the circuit area overhead will increase and the circuit performance will degrade. The above two transistors should be laid out carefully to improve the reliability of the whole system. Except for these faults, all other faults can be detected on-line by the TSC checker. If the transistor M_2 is stuck-open, this fault is equivalent to the GND line being floating, which will be detected by the checker. The error signal $E=0$ if M_3 or M_4 is stuck on, because of the ratioed transistor pairs (M_1, M_3) and (M_1, M_4). This is true even if subsequently M_1 is stuck on or stuck open. There is no conducting path from Vdd to E when transistor M_1 is stuck open, so E gets no chance to be charged, and will discharge toward 0 V. In any of these cases, the fault is equivalent to E being stuck at 0, which obviously can be detected by the checker. Finally, when transistor M_4 is stuck open, the fault is equivalent to E being stuck at 1 (unless there is a second fault—a stuck-on fault in the functional circuit—turning M_3 on), which also can be detected by the checker. This result is guaranteed under appropriate control of the periodic signal c_{12}, which is designed to fulfill the concurrent (on-line) fault detection capability of our approach. Signal c_{12} is functionally the ORed output of ϕ_1 and ϕ_2 (nonoverlapping two-phase clock). The half cycle when $c_{12}=1$ is for normal operation mode of the system; while the other half cycle is for test mode. This is illustrated in Fig. 4. In Fig. 5, we show the DFT approach for concurrent analog fault detection, which mixes the test phases and the normal-operation phases using c_{12}, in a pipelined system with a two-phase clock.

The functional circuit in Fig. 5 is structured in the form of an iterative pipelined array (e.g., a systolic array) of simple cells. In the figure, there are two AFD modules which are complementary to each other. The upper AFD module is for detecting stuck-on faults in even-numbered cells, while the lower AFD module is for detecting stuck-on faults in odd-numbered cells. The two error indication signals E_1 and E_2 produce 1-out-of-2 code outputs in the fault-free case (the reason that a checker requires at least two outputs is that a single-output checker cannot detect one of the output line stuck-at faults). A stuck-on fault in M_3 of the lower AFD module turns (E_1, E_2) from (1, 0) into (0, 0) during the test phase, which has the same effect when there is some stuck-on fault in the odd-numbered cells causing the gate of M_3 to be charged high. The (0, 0)

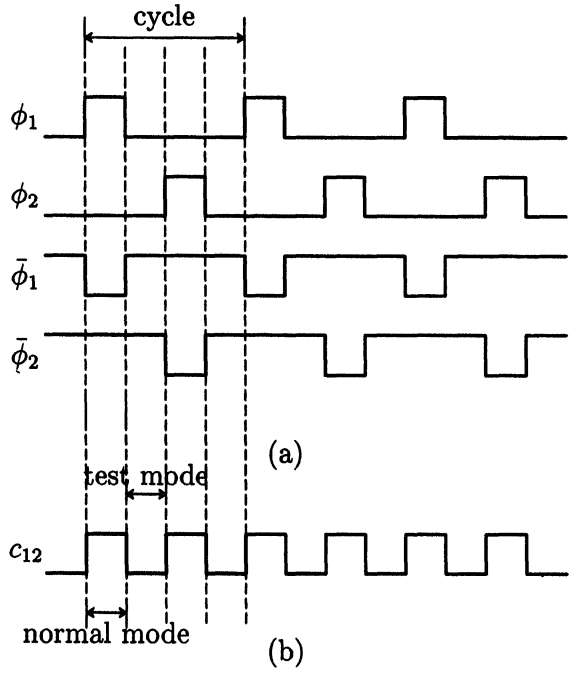


FIGURE 4 (a) Nonoverlapping two-phase clock. (b) Signal c_{12}.

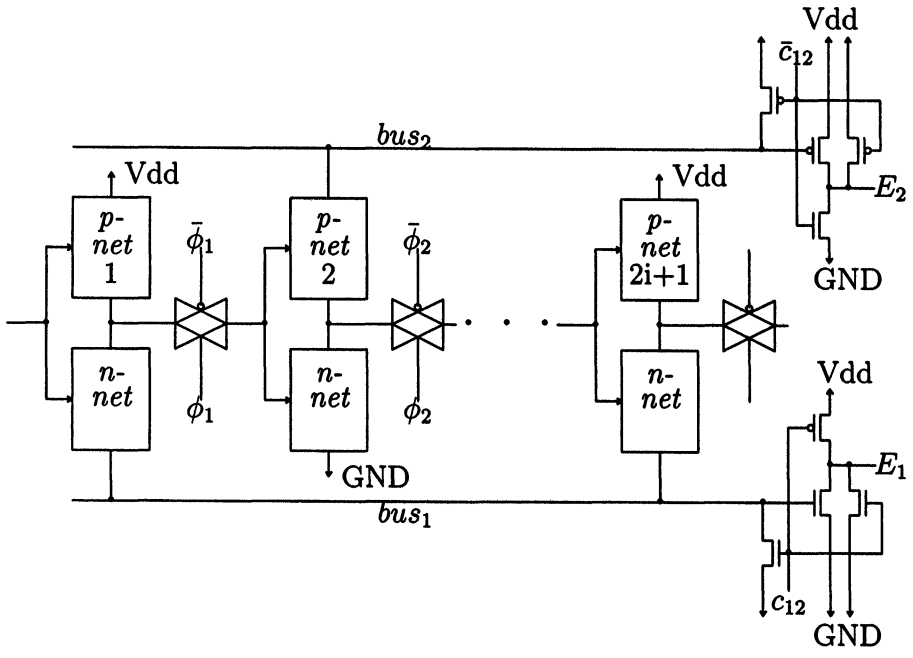


FIGURE 5 A DFT approach for concurrent CMOS analog fault detection.

output therefore indicates that there is a fault in the odd-numbered cells or the lower AFD module. Similarly, the (1, 1) output indicates that there is a fault in the even-numbered cells or the upper AFD module. Note that we consider only single faults. The correct timing of c_{12} is shown in Fig. 4(b). Because of cascading transistor M_2 (see Fig. 3) with the original circuit, the computation time may be increased and noise margin may be narrowed. To alleviate these problems, it is necessary to give an appropriate aspect ratio to transistor M_2.

4. CMOS AND BiCMOS PSCD CHECKER DESIGN

Modularity and regularity are vital circuit design criteria known to every VLSI designer. Many TSC checkers designed with modular structures have been proposed in the past[24–27]. In this section, we apply our analog fault concurrent detection technique to the unordered-code TSC checkers proposed by Smith[24]. Fig. 6 shows the structure of Smith's m-out-of-$2m$ TSC checker, which has been proved to be totally self-checking (with respect to single stuck-at faults, of course). Since the m-out-of-$2m$ TSC checkers are constructed by elementary *sorter* cells (Fig. 6), the m-out-of-$2m$ TSC checkers are modular and regular. This TSC checker can detect all single stuck-at faults at the gate level. However, when the fault model is extended to include switch-level faults, this checker will no longer satisfy the self-testing condition[6]. Kundu and Reddy therefore proposed a design procedure for two-level or multilevel (but with an even number of levels) circuits, which meet the TSC condition even if the transistor stuck-open faults are considered[24]. However, the stuck-on faults are not discussed in their paper.

The m-out-of-$2m$ PSCD checker is pipelined by adding transmission gates in between every two stages (or more, if desired) as shown in Fig. 7. To also detect the stuck-on faults concurrently, the AFD circuit can be used jointly with this pipelined checker. A two-variable *two-rail checker* (TRC) is then cascaded to form the final m-out-of-$2m$ PSCD

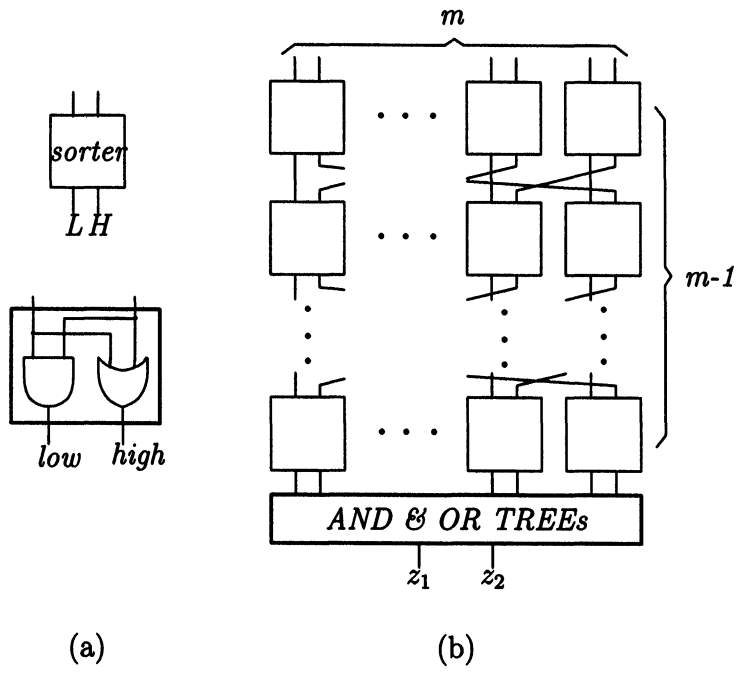


FIGURE 6 Smith's unordered-code TSC checker: (a) Schematic diagram of the elementary cell, which is a 2-bit sorter. (b) m-out-of-$2m$ code TSC checker by an array of $m \times (m-1)$ elementary cells.

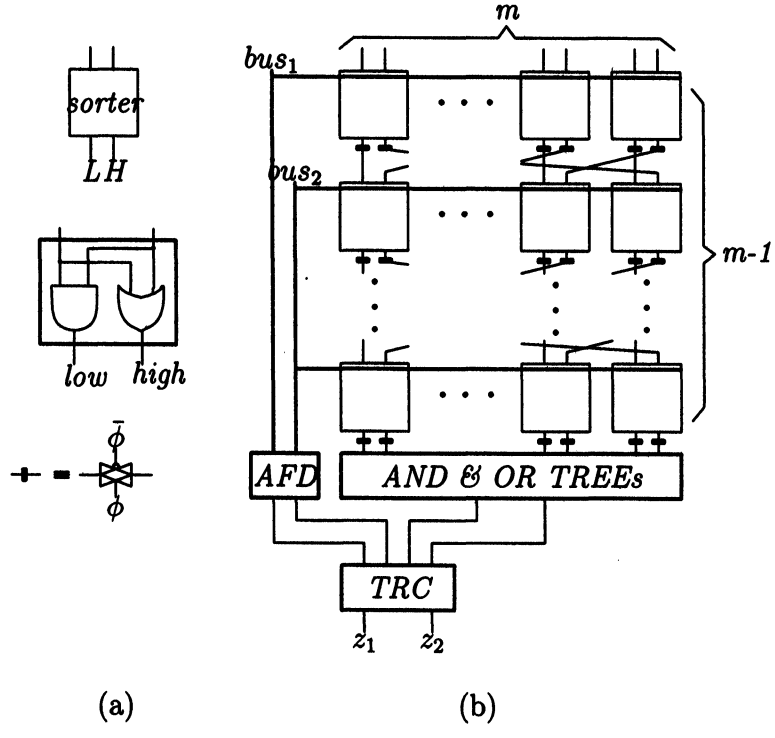


FIGURE 7 An m-out-of-$2m$ PSCD checker which can detect transistor stuck-on faults.

checker, as indicated in the figure. If there is a stuck-on fault in this checker, and an input pattern that sensitizes a power-ground path, then the AFD circuit takes on the value (0, 0) or (1, 1) instead of (0, 1) or (1, 0), which violates the normal input requirement of the TRC, causing its output (z_1, z_2) to display this error. Therefore, the stuck-on fault is detected.

Shown in Fig. 8(a) is one possible small system design. Since the AFD circuit can not be separated from the functional circuit, slight performance penalty is unavoidable. This effect however can be reduced by a careful design of transistor M_2 (see the next section). Another design is shown in Fig. 8(b), which is good for larger CMOS circuits. In the figure, there are $(n-1)$ AFD circuits: $(n-2)$ of them are for the functional circuit (which is partitioned into $(n-2)$ blocks), and the last one is for the original checker circuit. This design improves on the performance of large circuits by reducing stray capacitance on each bus. More AFD circuit modules can be used in a similar way to detect analog faults in a larger system. For example, we can use another AFD circuit to detect stuck-on faults in the TRC_n circuit (see Fig. 8(c)). Stuck-on faults on the TRC circuit is undetected, but since it is simple in circuit complexity, we can design it carefully to avoid analog faults. Without this assumption, the checker conditions would be hard, if not impossible, to satisfy.

To justify the proposed concurrent analog fault detection approach, an example circuit is designed, laid out, and simulated. Its schematic diagram and mask layout are shown in Figs. 9 and 10, respectively. The functional circuit is a pipelined inverter chain, which can be consider as a dynamic

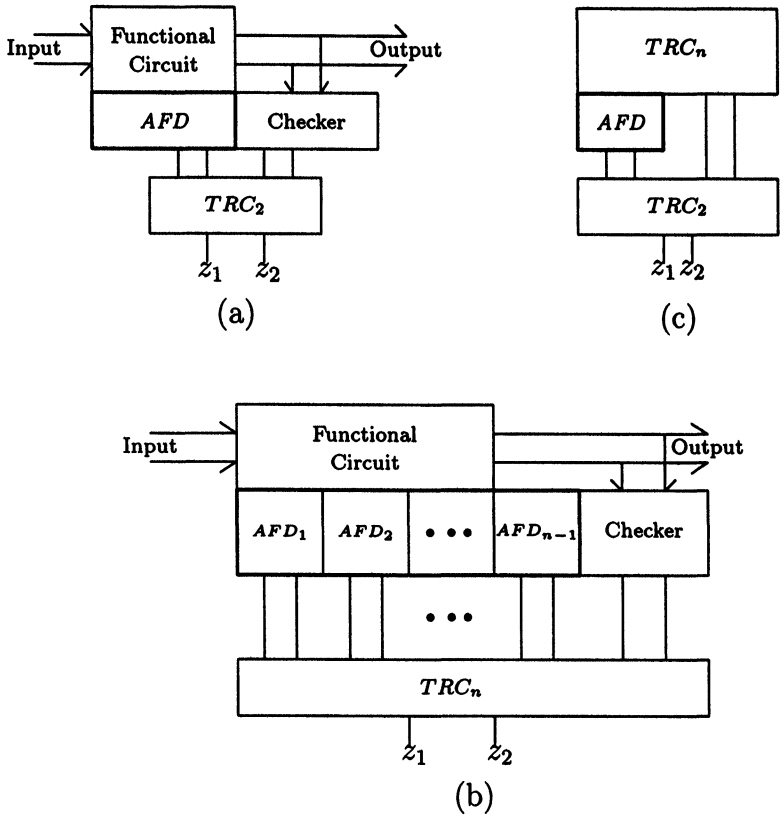


FIGURE 8 CMOS PSCD system designs: (a) For a small circuit. (b) For a large circuit. (c) With the AFD circuit embedded in TRC_n.

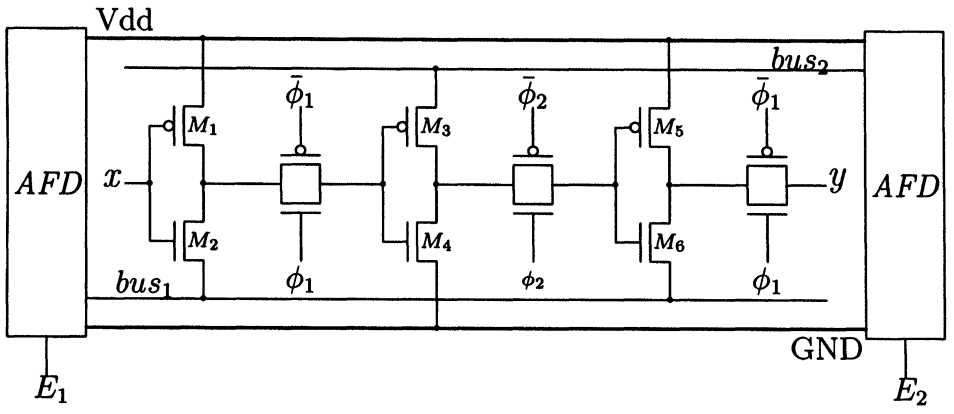


FIGURE 9 An inverter chain with the proposed AFD circuit.

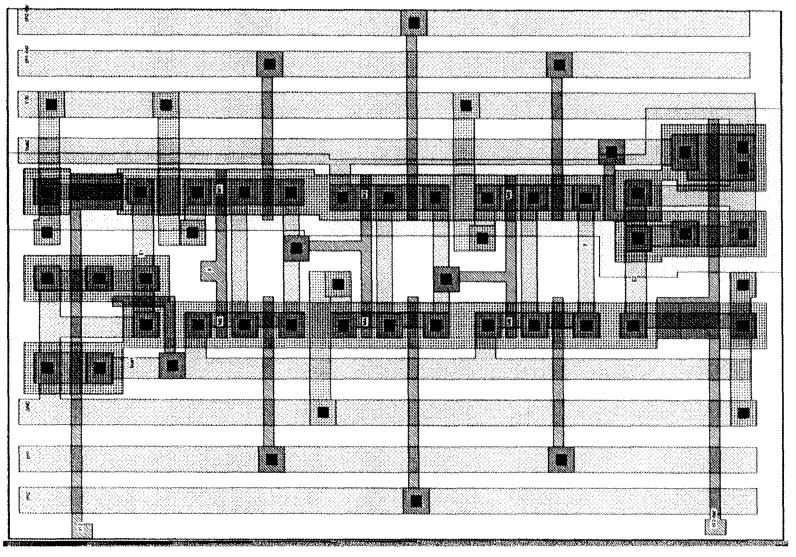
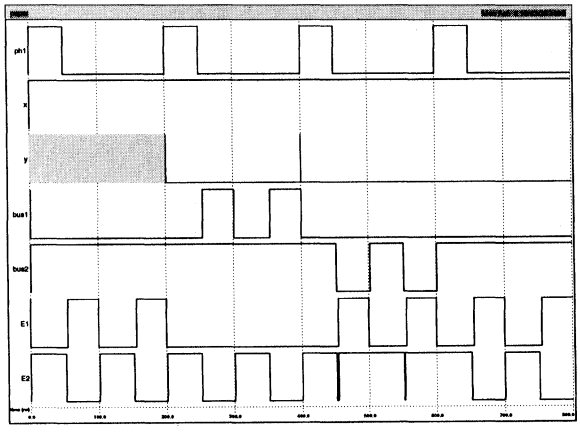


FIGURE 10 The mask layout of Fig. 9.

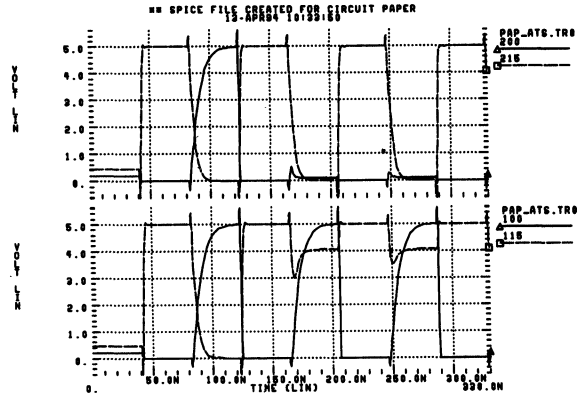
shift register—a frequently used circuit module in CMOS. The layout is based on a 3 μm CMOS technology, and the circuit is extracted from the layout and simulated. The aspect ratio (W/L) of M_1, M_3, and M_4 are 3/10, 4/2, and 4/2, respectively. Switch-level (Irsim) and circuit-level (Spice) simulation results are shown in Fig. 11, which are just as predicted. In Fig. 11(a), signals x and y are the input and output of the CUT, respectively. We apply $x = 1$ and monitor its output y, which does not change even if there are two consecutive faults in the circuit, i.e., we can not tell whether the circuit is faulty or not just by observing primary output y. However, we are able to know that the circuit is faulty (there are analog faults) by observing the error indication signals E_1 and E_2, which alternate back and forth between (0, 1) and (1, 0) in the fault free case (before 200 ns). If there is a stuck-on fault in transistor M_1 (of Fig. 9), then the signals (E_1, E_2) will take on the values (0, 0) to indicate this analog fault (from 250 ns to 300 ns and 350 ns to 400 ns). If there is a stuck-on fault in transistor M_4 (of Fig. 9), then the signals (E_1, E_2) will take on the values (1, 1) to indicate this analog fault (from 450 ns to 500 ns

and 550 ns to 600 ns). From 600 ns to 800 ns, this circuit is fault free again. Fig. 11(b) shows the Spice simulation result corresponding to Fig. 11(a), in which the upper half shows the result for 0 ns to 400 ns, while the lower half shows that for 400 ns to 800 ns. It should be noted that stuck-at faults in the inverter chain cannot be detected at (E_1, E_2), however, they will be exposed at (Z_1, Z_2) as shown in Fig. 8.

A 4-out-of-8 code checker chip employing the proposed scheme has been designed, simulated, fabricated, and tested. The 2062-transistor chip is fabricated by an inexpensive 3 μm CMOS technology, which runs at about 1.7 MHz, and occupies an area of about 25 mm^2. We received 20 parts from CIC (Chip Implementation Center, a service organization in Taiwan similar to MOSIS in the US), among which 85% worked as predicted by the simulation results. The failed parts are due to fabrication defects (there is no test service performed by CIC or the foundry). Fig. 12 shows the layout plot of the PSCD checker chip, in which there are eight 4-out-of-8 code PSCD checkers. The process we used for the experiment is slow, but our purpose was to justify the functionality of our checker scheme and to see how much performance penalty we will suffer from the extra nMOS transistor appended to the pull-down path. Our measurement result is consistent with the Spice simulation as shown in Fig. 13, in which we trace the rising and falling transitions of the original circuit (in solid line) and the circuit with the AFD scheme (in dashed line). There is no difference in rising transition as expected, but in falling transition there is an extra 10% delay time when the AFD circuitry is included. This penalty obviously is unavoidable. It however can be reduced by using the BiCMOS technology. Fig. 14 shows this new circuit.



(a)



(b)

FIGURE 11 Simulation results: (a) Switch level. (b) Circuit level.

Although the performance degradation also can be reduced by a careful layout of transistor M_2 (in Fig. 3), it has many side-effects. Owing to the speed degradation, the functional and checker circuits may need a number of AFD circuits to detect steady-state current produced by a stuck-on transistor. Maly and Patyra pointed out that a *bipolar junction transistor* (BJT) device, rather than a MOS device, should be used as a voltage drop element in a current sensor[16], since BJTs have high switching speed and low voltage drop (in the saturation mode). In our design, the transistor M_2 can be replaced by an *npn* BJT (see Fig. 14). The circuit performs the same logic function, and the system speed is improved. We also can replace the MOS transistor M_3 (in Fig. 3) with a BJT (see Fig. 14), which reduces the testing time. Fault models for

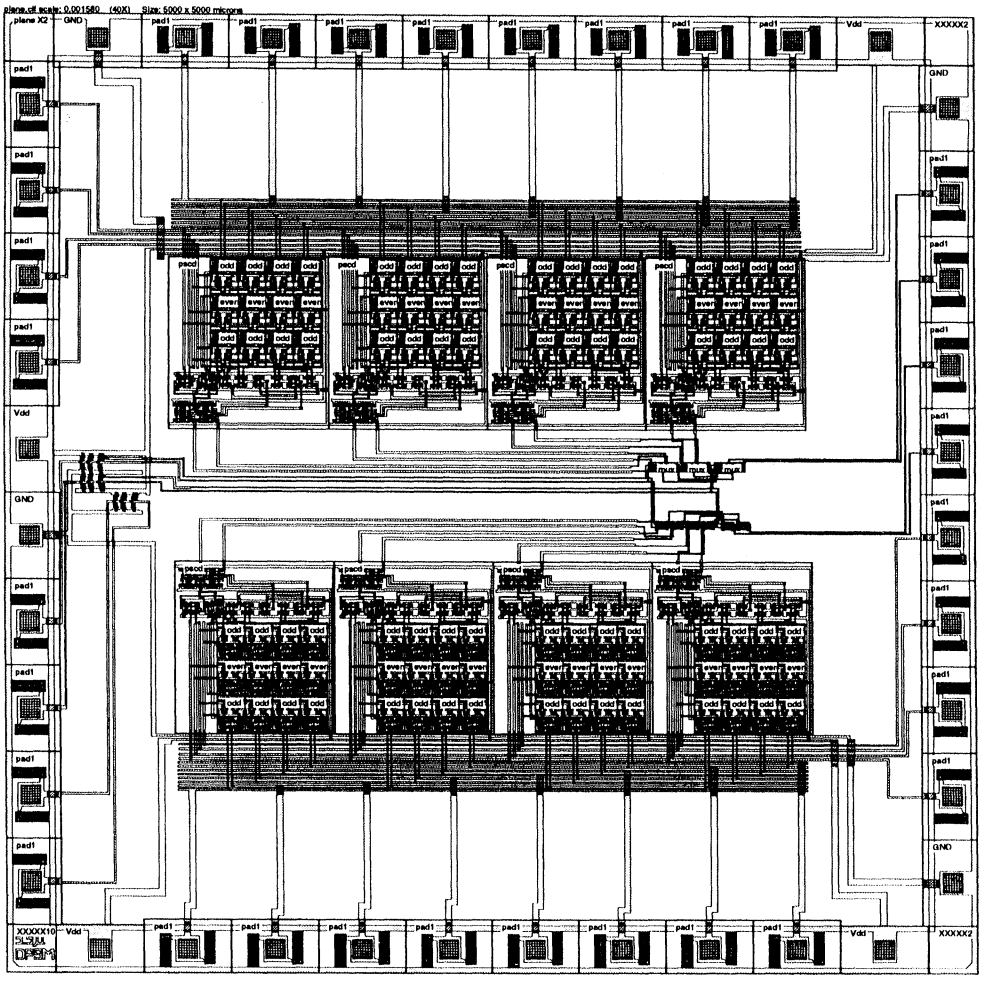


FIGURE 12 Chip layout of the fabricated 4-out-of-8 code PSCD checker.

BJTs are assumed to be transistor stuck-on and stuck-open faults, which are similar to those for MOS transistors. Therefore, the AFD circuits in Fig. 14 preserves the PSCD property.

To evaluate our new scheme, both the circuit with AFD and the circuit without AFD (the original circuit) are simulated. Spice simulation results are shown in Fig. 15, in which the solid line is for the circuit without AFD, and the dashed line is for the circuits with AFD. The upper half of the figure shows that the difference between the circuit with AFD and the original circuit is very small (as compared with Fig. 13). Though the circuit performance is greatly improved, the power consumption also increases. Static power is consumed during the time period when the control signal c_{12} is high (see the lower half of the figure, which shows the current levels). Therefore, if the resistance of R is low (e.g., 4.3 KΩ), the circuit will consume large power. The power consumption can be reduced to approximately the power consumption of the original circuit, shown in Fig. 16, if the resistance R is increased (e.g., 86 KΩ). The resistance needs not be linear, so we can use a MOSFET for this purpose. There is a trade-off between power consumption and area overhead.

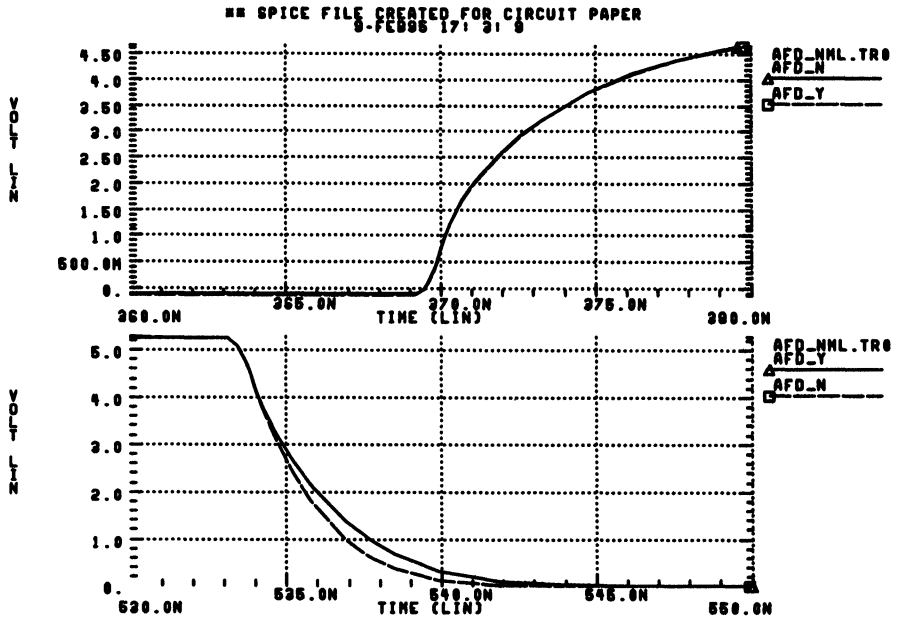


FIGURE 13 Delay comparison between the original circuit and that with the AFD scheme.

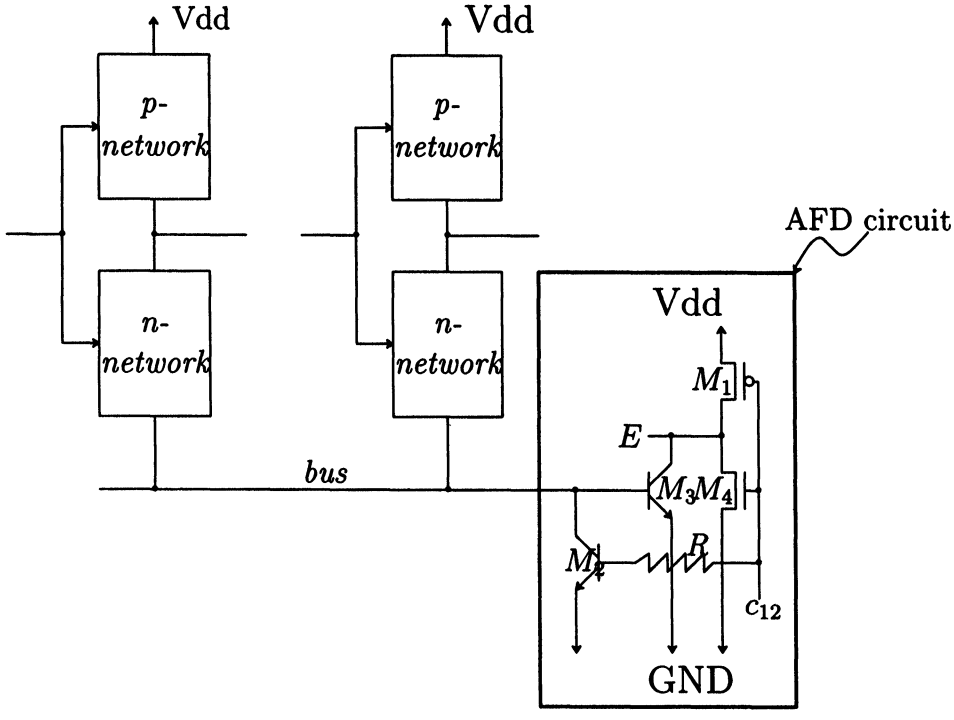


FIGURE 14 Steady-state current detection circuit using BiCMOS technology.

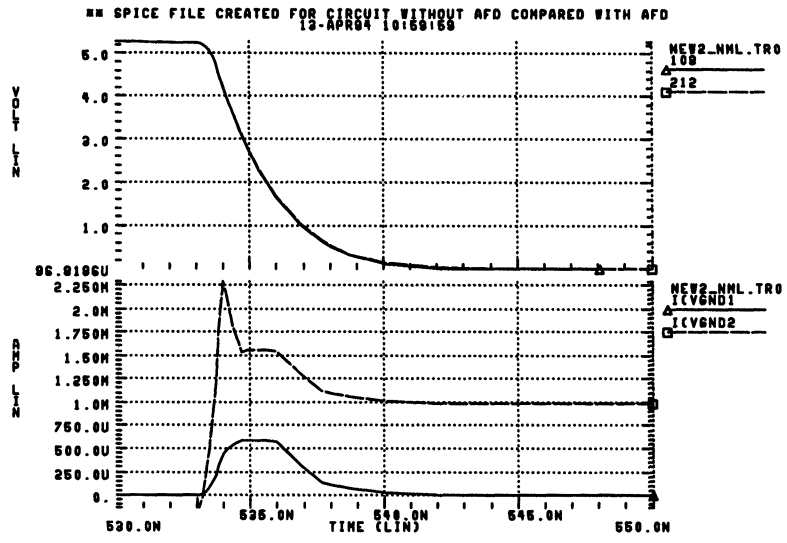


FIGURE 15 Simulation result: $R = 4.3\,\mathrm{K}\Omega$.

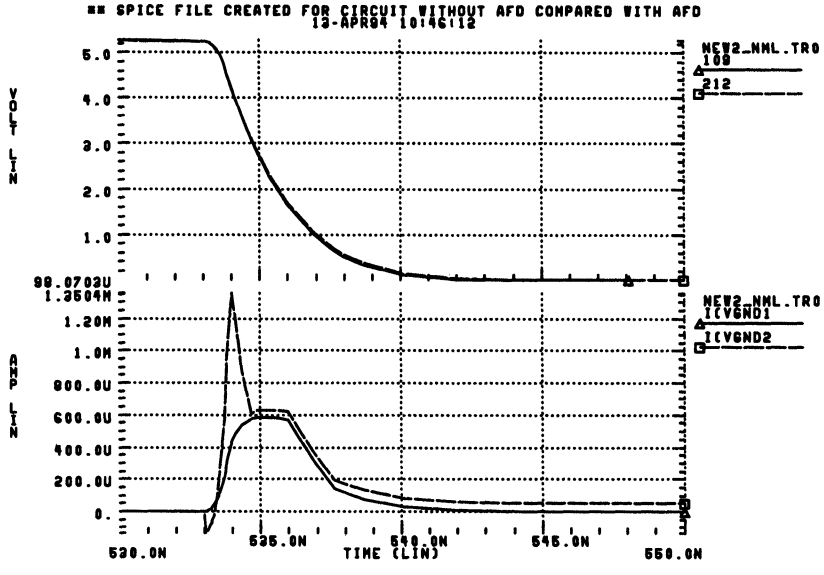


FIGURE 16 Simulation result: $R = 86\,\mathrm{K}\Omega$.

5. CONCLUDING REMARKS

We discuss concurrent detection of CMOS stuck-on and bridging faults which induce steady current flow. We first review a novel scheme of detecting transistor stuck-on faults which was proposed by Favalli, *et al.*[19]. Then the circuit is modified to fulfill the requirement of concurrent error detection, and is applied to an m-out-of-$2m$ TSC checker. We show that the combined m-out-of-$2m$ checker is two-fault tolerant partially strongly code disjoint (2-FT PSCD). A simple inverter chain is presented to justify our concurrent detection approach. Switch and circuit level simulations are

performed, and chips are fabricated and tested, which shows the correctness of the method, and also shows that performance penalty can not be avoided.

An important factor that affect the performance is that the parasitic capacitance from the virtual ground (*bus* in Fig. 3) and true ground is large due to the diffusion-substrate capacitances of all the pull-down nMOS transistors. If the circuit speed is untolerable due to this effect, the functional circuit has to be further divided into smaller subcircuits, i.e., with separate shorter busses and multiple AFD circuits. This becomes a tradeoff between clock period and chip area.

In a similar work[18], performance degradation is reduced by connecting in parallel with the current sensor a large diode. We propose an alternative solution—BiCMOS circuits are used to reduce performance degradation. Although this method can be used only with the BiCMOS process (which have become common in the industry), the checker circuit is simpler. The current sensor in[18] is SCD, while ours is PSCD. Both methods require specific clocking schemes.

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