VLSI DESIGN
1998, Vol. 8, Nos. (1–4), pp. 325–330
Reprints available directly from the publisher
Photocopying permitted by license only

RF Performance of Si/SiGe MODFETs: A Simulation Study

S. ROY, A. ASENOV*, S. BABIKER , J. R. BARKER and S. P. BEAUMONT

Nanoelectronics Research Centre, Department of Electronics and Electrical Engineering, Glasgow University, Glasgow G12 8LT, Scotland, UK

The microwave performance potential of Si/SiGe pseudomorphic MODFETs are studied, in comparison to state of the art InGaAs pseudomorphic HEMTs. Both devices have equivalent structures corresponding to a physical HEMT used for calibration. We use an RF analysis technique based on transient Monte Carlo simulations to estimate the intrinsic noise figures, the RF figures of merit f_T and f_{max}, and the effect of contact and gate resistances. Both devices exhibit velocity overshoot below the gate region. It is shown that the difference in noise figures and f_T values can be mainly attributed to differences in device channel velocity. f_{max} exhibits a strong dependence on device contact resistance, eroding some of the performance advantage of the pseudomorphic HEMT.

Keywords: Si/SiGe, heterostructures, Monte Carlo, microwave performance, RF analysis

INTRODUCTION

Recent theoretical and experimental studies show that low field mobility and velocity overshoot are enhanced in Si layers grown pseudomorphically on relaxed SiGe substrates. Induced strain breaks the six-fold degeneracy of the Si conduction band, resulting in an improved band offset for the two conduction valleys whose transverse effective mass is in the plane of the heterojunction. This increases the in plane effective mobility and reduces inter-valley scattering in the Si layer [1]. Modulation doped field effect transistors (MODFETs) based on this material system have been demonstrated, and show significant potential for RF applications [2, 3]. Although measured mobilities are lower than those reported in optimal III–V based devices, the compatibility between SiGe and conventional Si processing technology makes such MODFETs attractive for Si MMICs design and microwave signal processing applications integrated on conventional Si chips. Therefore, comparison of strained Si channel devices with well established members of the III–V family will

* Corresponding author. Tel.: ++44 141 330 5233, Fax: ++44 141 330 4907, e-mail: A. Asenov@elec.gla.ac.uk.

provide greater insight into their potential performance and limitations.

As part of this goal, we here study the microwave performance potential of a Si/SiGe pseudomorphic MODFET in comparison with a state of the art InGaAs channel pseudomorphic HEMT, using an RF analysis technique based on transient Monte Carlo simulations.

DEVICE STRUCTURES AND PERFORMANCE ANALYSIS

To allow a fair comparison similar device layer structures are considered (Figs. 1a,b). Both devices have δ-doping separated by a 2.5 nm spacer from the channel, a T shape recess gate with 50 nm recess offset and heavily doped (n-type $10^{18}\,cm^{-3}$) cap layers. An effective δ-doping of $5\times10^{12}\,cm^{-2}$ is considered in the both cases. Total gate-to-channel separation is 22 nm and the gate length is 0.12 μm. p-type background substrate doping of $10^{14}\,cm^{-3}$ is considered. This corresponds to the dimensions of real pseudomorphic HEMT fabricated at the Glasgow Nanoelectronics Research Centre and used for validation and calibration of the RF Monte Carlo analysis technique (described in an accompanying paper [4]). We realise that for the Si/SiGe MODFET this may pose unresolved growth problems. Specifically we conjecture improvements in growth technology and low temperature processing to allow formation of a well defined As δ-doping supply layer. For simplicity of Monte Carlo modelling a uniform SiGe substrate is assumed, instead of a 'virtual substrate' with graded Ge concentration. The 'etch stop' region of the Si/SiGe device is also considered as (undoped) SiGe. Simple 1-D Poisson calculations indicate that if a strained Si 'etch stop' region is included, it will exhibit negligible parallel conductance at a d.c. bias of $V_G = -0.25$ V.

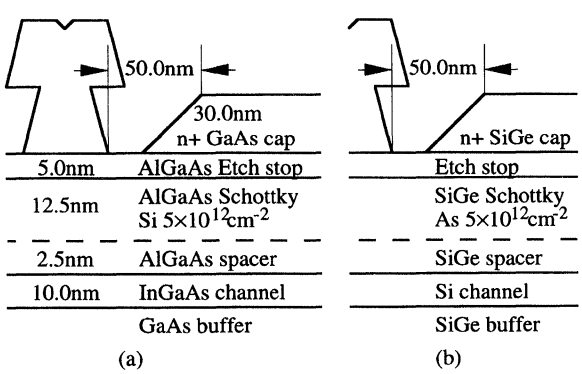

FIGURE 1 Vertical layer structure of (a) a 0.12 μm pseudomorphic HEMT and (b) a 0.12 μm pseudomorphic MODFET. Both devices have the same vertical dimensions.

RF analysis of HEMT and MODFET performance is based on Monte Carlo simulation of device transient response. We follow Yamada's [1] treatment of the effect of the strain on the Si channel band structure, with conduction band splitting of $\Delta E_c = 0.67x$ (eV) and band gap $E_g = 1.11 - 0.74x$ (eV). However the six phonon scattering model of Jacoboni [5] is implemented, instead of the four phonon model in [1]. Acoustic and ionised impurity scattering modes are also included, with ionised impurity scattering calculated from the Brooks-Herring model [6]. Bulk velocity-field characteristics obtained from the model are in agreement with experimental unstrained Si data at 77 K and 300 K and previous results for strained Si [1, 7]. The transient Monte Carlo simulations begin by following 5×10^4 superparticles for 2 ps settling time at d.c. bias, then a further 2.0→2.6 ps during which device statistics are recorded at 1 fs intervals. A step change $\Delta V_G = 0.2$ V, or $\Delta V_D = 0.3$ V is then consecutively applied, and the transient response measured for a further 2 ps. It is found that structure and doping dependant THz oscillations in device drain current (possibly due to plasma oscillations in the channel, or in the heavily doped cap layer) may mask the detailed form of the transients, and so a number of traces are averaged to define the response. Complex y-parameters are derived by Fourier transforming these terminal current transients, and used to extract the small signal equivalent circuit, intrinsic noise figures, and estimate the RF performance figures of merit f_T (cutoff frequency) and f_{max} (maximum frequency of oscillation). Finally, the small signal equivalent

circuit is augmented by the addition of external impedance, and thus the effect of contact and gate resistance on the 'real' device operation estimated. A detailed description of the analysis process is given in [4].

RESULTS AND DISCUSSION

The average velocity in the channel of both devices is compared in Figure 2 for a d.c bias of $V_D = 1.5$ V and $V_G = -0.25$ V. In the pseudomorphic HEMT this corresponds to the region of maximum transconductance, while in the pseudomorphic MODFET it is the region of maximum transconductance achieved while constraining parallel conduction in the δ-doped region to less than 10% of total conduction. The gate extends from $x = -0.12 \rightarrow 0.0\,\mu$m. Both devices show distinct overshoot below the gate region. Peak velocity in the pseudomorphic MODFET, at the drain end of the strained Si channel, approaches twice the saturation velocity of bulk unstrained Si. The ratio between peak velocity in the MODFET compared to that of the pseudomorphic HEMT InGaAs channel is 2.8.

Figures 3–5 and Table I characterise the RF performance of the two devices. The intrinsic noise figures NF (in decibels) are shown in Figure 3. From the definition of NF we postulate that the significant difference between the devices will be in their transconductance $g_{mo} = Y_{21}$. All other terms - y-parameters and current fluctuations $<\delta I^2>$ – we therefore represent by an approximate constant C.

$$NF = 1 + \left[\frac{Y_{11}}{Y_{21}}\right]^2 \frac{<\delta I_d^2>}{<\delta I_g^2>} \approx 1 + \left(\frac{C}{g_{mo}}\right)^2 \quad (1)$$

From Figure 3 and equation (1) the ratio of transconductances g_{HEMT}/g_{MODFET} is indeed found to be approximately constant below 60 GHz, with value 2.6. The transconductance values directly obtained from the Monte Carlo simulations are $g_{HEMT} = 87$ and $g_{MODFET} = 31$, with ratio 2.8. It can be concluded that the bulk of the

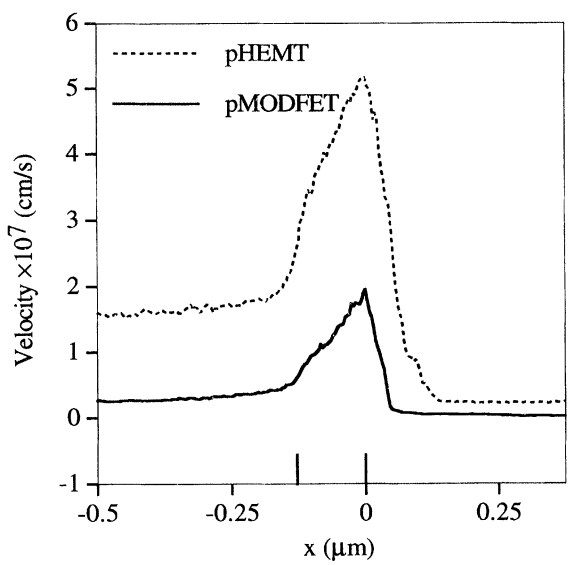

FIGURE 2 Comparison between average velocity in the channel of 0.12 μm pseudomorphic HEMT and MODFET. $V_D = 1.5$ V, with $V_G = -0.25$ V corresponding to maximum transconductance.

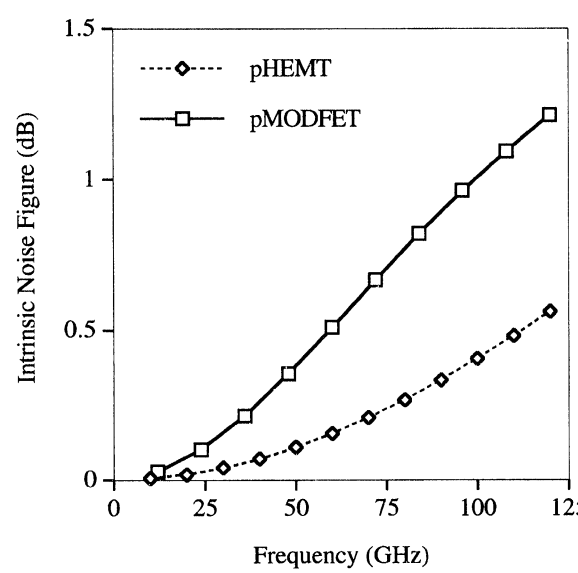

FIGURE 3 Comparison between minimum intrinsic noise figures for pseudomorphic HEMT and MODFET as a function of frequency. $V_D = 1.5$ V, with $V_G = -0.25$ V.

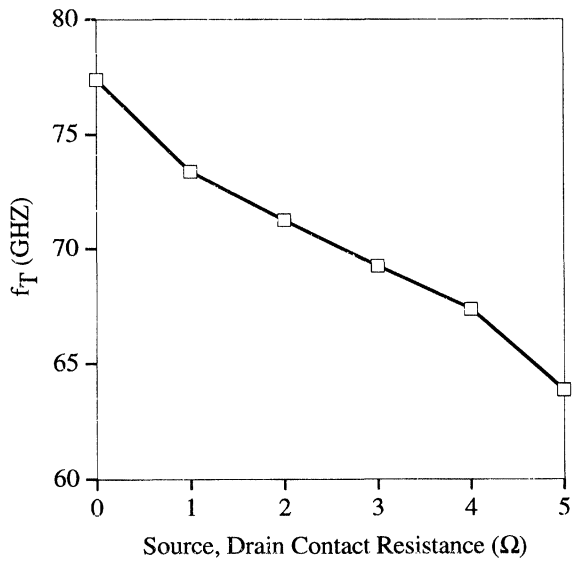

FIGURE 4 Variation of f_T in a pseudomorphic MODFET as a function of source and drain contact resistance (f_T invariant to changes in gate resistance).

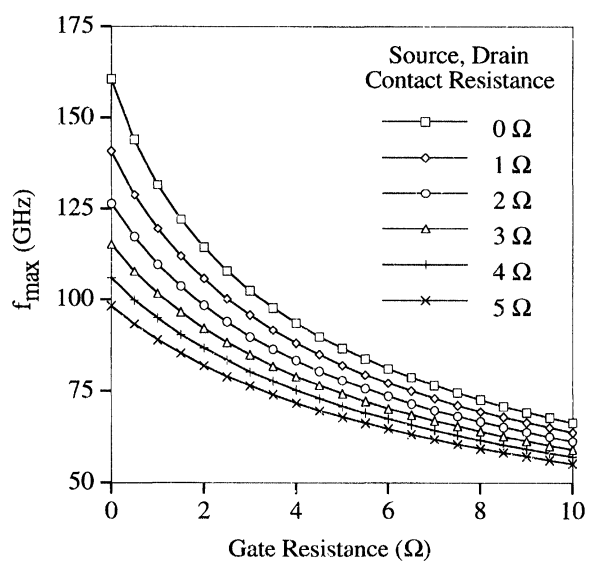

FIGURE 5 Variation of f_{max} in a pseudomorphic MODFET as a function of gate and contact resistances.

difference in noise figures between the two devices can be attributed to the differences in transconductance – and thus to differences in channel velocity.

TABLE I Calculated RF figures of merit for pseudomorphic HEMT and MODFET at bias $V_D = 1.5$ V, $V_G = -0.25$ V. Device width of 100 μm is assumed. f_T, f_{max} calculated for both negligible external gate and drain contact resistance, and for more realistic contact resistances of 5Ω

RF figure of merit (GHz)	Pseudomorphic HEMT	Pseudomorphic MODFET
with negligible contact resistance		
f_T	192	77.4
f_{max}	634	161
gate, source & drain resistances all of 5 Ω		
f_T	156	63.9
f_{max}	169	68.0

Table I lists the RF figures of merit extracted from the transient response of each device. The ratio of cut-off frequencies f_T for the pseudomorphic HEMT and MODFET is approximately 2.5 and independent of external resistance. This implies that the value of f_T is primarily governed by the channel velocity of the respective device. However, the ratio of f_{max} for the pseudomorphic HEMT and MODFET is 3.9 for intrinsic devices, and drops to 2.5 when external contact resistances of 5Ω are applied. A more realistic inclusion of device parasitics in this case reduces the advantages of the pseudomorphic HEMT. Finally, Figures 4 and 5 detail the effect of varying contact resistance on both figures of merit for the pseudomorphic MODFET, and show clearly the strong dependence of f_{max} on device parasitics.

CONCLUSIONS

The microwave performance potential of a Si/SiGe pseudomorphic MODFET was studied, in comparison to a state of the art InGaAs channel pseudomorphic HEMT. We used an RF analysis technique based on transient Monte Carlo simulations, calibrated to a physical HEMT. The difference in device noise figures was attributed mainly to differences in device transconductance, and thus to differences in channel velocity. The cut-off frequency f_T was also shown to be governed by channel velocity. However the max-

imum frequency of oscillation f_{max} was seen to exhibit a strong dependence on device contact resistance, eroding some of the advantage of the pseudomorphic HEMT over the Si/SiGe MODFET.

References

[1] Yamada, T., Zhou, J., Miyata, H. and Ferry, D. K. (1994). "In-Plane Transport Properties of $Si/Si_{1-x}Ge_x$ Structure and its FET Performance by Computer Simulation", *IEEE Trans. Elec. Devices*, **41**(9), 1513.

[2] Ismail, K., Rishton, S., Chu, J., Chan, K. and Meyerson, B. (1993). "High-performance Si/SiGe *n*-type modulation-doped transistors", *IEEE Electron Device Letters*, **14**(7), 348–350.

[3] Welser, J., Hoyt, J. L. and Gibbons, J. F. (1994). "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors", *IEEE Electron Device Letters*, **15**(3), 100.

[4] Babiker, S., Asenov, A., Cameron, N., Beaumont, S. P. and Barker, J. R. "Complete RF analysis of compound FETs based on transient Monte Carlo simulation", *this issue*.

[5] Jacoboni, C. and Lugli, P. (1989). *The Monte Carlo Method for Semiconductor Device Simulation*, Wein, Springer-Verlag.

[6] Brooks, H. (1951). "Scattering by Ionized Impurities in Semiconductors", *Phys. Rev.*, **83**, 879.

[7] Roldén, J. B., Gámiz, F., López-Villanueva, J. A. and Carceller, J. E. (1996). "A Monte Carlo study on the electron-transport properties of high-performance strained-Si on relaxed SiGe channel MOSFETs", *J. Appl. Phys.*, **80**(9), 5121.

Authors' Biographies

Scott Roy is a researcher in the Department of Electronics and Electrical Engineering at the University of Glasgow, from where he received a Ph.D. in 1994 for investigations into the engineering and architectural aspects of extended single electronic systems. His interests include high performance computing (he represented Glasgow University in ESPRIT Project ZEUS; Zentren Europáischen Supercomputings) and its application to device modelling. He is presently developing codes to simulate and optimise *n*-channel SiGe FETs for VLSI and RF applications – and designing, in collaboration with Motorola UK, multiprocessor systems on which they will run.

Sherief Babiker studied Electrical Engineering in Khartoum University Sudan (1979–1984). During the period 1985–90 he worked at the Electrical Engineering Department of Khartoum University. In 1994 he was awarded a Ph.D. degree for work on the theory and modelling of single-electronic devices and systems. His current research interests concentrate on the simulation and modelling of FETs with emphasis on submicron gate length InGaAs channel pHEMTs for RF applications.

Asen Asenov had 10 years industrial experience as a head of the Process and Device Modelling Group in IME – Sofia, developing one of the first integrated process and device CMOS simulators IMPEDANCE. He was visiting professor at the Physics Department of TU Munich, and is currently a Reader in the Department of Electronics and Electrical Engineering, Glasgow University. As a leader of the Device Modelling Group he has contributed to the development of 2D and 3D device simulators and their application in the design of FETs, SiGe MOSFETs and IGBTs. He also investigates the design of parallel algorithms.

John Barker is Professor of Electronics in the Department of Electronics and Electrical Engineering. He has a long standing interest in computational methods, device modelling and transport theory. From 1970–85 he was a member of the Theory group in the Dept. of Physics, University of Warwick, aside from 1978–79 when he worked at IBM T.J. Watson Laboratory, North Texas State University and Colorado State University. From 1987–89 he was academic director of the IBM UK/Glasgow University Kelvin Project on Numerically Intensive Parallel Computing. He is academic director of the Parallel Processing Centre at the University of Glasgow.

Steve Beaumont was educated at the University of Cambridge and has been with the Department of Electronics and Electrical Engineering at the University of Glasgow since 1978. He became Head of Department in 1995 and he convenes the Nanoelectronics Research Centre's management committee. His research interests lie in the field of

nanometre-scale fabrication and its application to electronic and optoelectronic devices. He has over 100 publications on electron beam nanolithography, dry etching, short-gate III – V based transistors, quantum transport devices, the optical properties of quantum dots, and single electron devices. Latterly he has become involved with the issue of manufacturability of mm-wave circuits and the use of nanometre-scale fabrication techniques coupled with technology-based device simulations to forecast performance and yield with the minimum of process iterations.