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Single-Electron Memories

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One of the most promising applications of single-electronics is a single-electron memory chip. Such a chip would have orders of magnitude lower power consumption compared to state-of-the-art dynamic memories, and would allow integration densities beyond the tera bit chip.We studied various single-electron memory designs. Additionally we are proposing a new memory cell which we call the *T*-memory cell. This cell can be manufactured with state-of-the-art lithography, it operates at room temperature and shows a strong resistance against random background charge.

Keywords: Memory, single-electron tunneling, simulation, random background charge

1. INTRODUCTION

Over the last years many applications of the Coulomb blockade and of Coulomb oscillations, so called single-electron devices, have been proposed. The most fundamental device is the single-electron transistor [1] which was soon followed by pumps, turnstiles, supersensitive electro-meters, memories and logic gates (see for example [2]). Many of these devices have been fabricated as laboratory prototypes with various manufacturing processes, and have been operated usually at temperatures at or below liquid Helium (4.2 K). Some effects could be seen and some prototypes could be operated up to liquid nitrogen temperature (77 K) [3] and only very few functioned at room temperature (300 K) [4]. But almost all of these prototypes suffer from the extraordinary charge sensitivity of single-electron devices which makes them strongly vulnerable to uncontrollable impurities, traps and charge transport in other parts of the circuit. Additionally all employed manufacturing processes have not been proven to be applicable for mass production. That is, the challenge for the next years is to find reliable and reproducible mass production methods for robust room temperature single-electron devices.

All results and conclusions are based on computer simulations which have been performed with our single-electron device and circuit simulator SIMON. For more information about SIMON please refer to [5, 6].

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2. DIFFERENT SINGLE-ELECTRON MEMORY CELLS

In the following we are describing briefly the function of different single-electron memory cells. Some of them have already been extensively treated in other publications.

2.1. Flip-Flop

One design possibility is to mimic conventional CMOS architecture with single-electron devices. A static single-electron memory cell design or flip-flop, based on this approach was proposed by A. Korotkov *et al.* [7].

2.2. Electron Trap

Nakazato and Ahmed [8] proposed a dynamic memory cell pushed to its extreme limit. A small number of electrons is stored on a single quantum dot. The central island of a single-electron transistor which is extremely charge sensitive, may be used as sensor for the logic states. However exactly this charge sensitivity makes these devices prone to random background charge. The more tunnel junctions are used the less likely it is that electrons are co-tunneling to ground. That is why this memory is a dynamic memory, since the charges can not be trapped infinitely. Nevertheless, the refresh rate can easily extend to the second or minute range.

2.3. Ring Memory

Another idea which is a generalization of the bistable quantum cell for cellular automata by Lent *et al.* [9] is the ring memory cell. An even number n of tunnel junctions are connected to a ring, and $n/2$ electrons are inserted into the ring. These electrons will repel each other and can form two stable configurations. Applying voltage pulses will switch the state of the ring to either one of the stable configurations.

2.4. Q_0 -Independent Memory

The first random background charge or Q_0-independent memory was proposed by Likharev and Korotkov [10]. The basic idea is the following. Electrons are stored on an island or floating gate. A single-electron transistor which is very charge sensitive on its gate, is used to sense the changes of charge on the floating gate. The trick to achieve the Q_0-independence is not to sense any absolute charges, but to sense the current oscillations in the single-electron transistor, which are caused by changes in the charge on the gate. In other words, the charge change on the floating gate induces current oscillations. These oscillations occur at any background charge. Only the phase, not the amplitude is background charge dependent. The cell can only be read destructively by discharging the floating gate. If current oscillations are detected, the floating gate was charged with electrons. If no oscillations are detected, no charge was stored on the floating gate.

2.5. Discussion of Simulation Results

We simulated the above memory cells and especially studied their operation temperature, complexity and random background charge dependence. Due to lack of space we can not discuss the details of our simulation results. But all of the above designs have at least one flaw. Many are random background charge dependent (flip-flop, electron trap, ring memory). Some are quite complex and show a relative low operation temperature compared to other designs with the same tunnel junction parameters (flip-flop, ring memory).

3. THE THREE CHALLENGES

Thus we can name three challenges that have to be addressed:

- Room temperature operation,
- Industrial mass production,

- Random background charge independence for reliable operation.

Coulomb blockade effects are only observed if the charging energy associated with the tunneling of a single electron is bigger than the thermal energy kT, with k the Boltzmann-constant, and T the absolute temperature. To produce devices which operate at room temperature a resolution limit of < 10 nm is necessary. This means, that for industrial mass production only naturally formed tunnel junctions (poly-silicon, granular films) are feasible today. It is not possible with todays industrial lithography to produce a single tunnel junction with dimensions smaller 10 nm. The resolution limit of optical lithography is more than a magnitude larger than 10 nm. Clearly, the next decade will see new high resolution lithography methods (X-ray, e-beam, near-field, nano-imprint, STM, AFM, ...), but until they are not available for industrial mass production only naturally formed tunnel junctions in granular films can reach resolutions in the nano-meter regime and thus allow room temperature operation.

4. A NEW MEMORY CELL

Combining todays lithography with granular film processes one can manufacture what we call a T-memory cell. Two granular film batches are arranged in a T-shape (see Fig. 1). It is a combination of a multi-electron trap with a multi-island transistor for read-out. The cross-bar of the T is the multi-island transistor which is controlled by a gate electrode which stores either a number of electrons or a number of holes. Writing a '1' or '0' is done by applying a positive or negative voltage pulse at the word-line. This will charge the gate electrode which has a similar function as the floating gate in a flash memory cell. Thus in our example a positive write pulse on the word-line will store some holes on the gate electrode representing '1' and a negative write pulse will store some electrons on the gate electrode representing '0'. Destructively reading the memory cell is done by applying for example a negative voltage pulse at the word-line and sensing current oscillations of I_{out}. If I_{out} oscillates then the cell held a '1'. If no oscillations are picked up then the cell held a '0'. Accordingly the contents of the cell has to be restored.

The T-cell can be viewed as a combination of the electron trap [11] and the Q_0-independent memory cell [10], with the change that we use tunnel junction arrays for both elements, the trap and the read-out transistor. This change makes the T-memory cell much easier to manufacture. In fact,

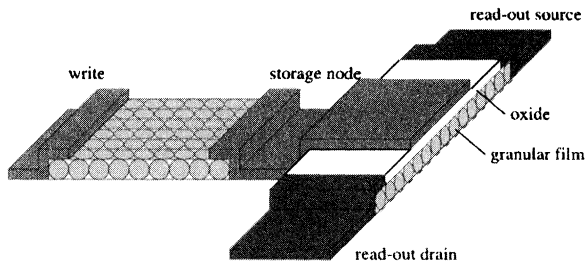

FIGURE 1 T-memory cell.

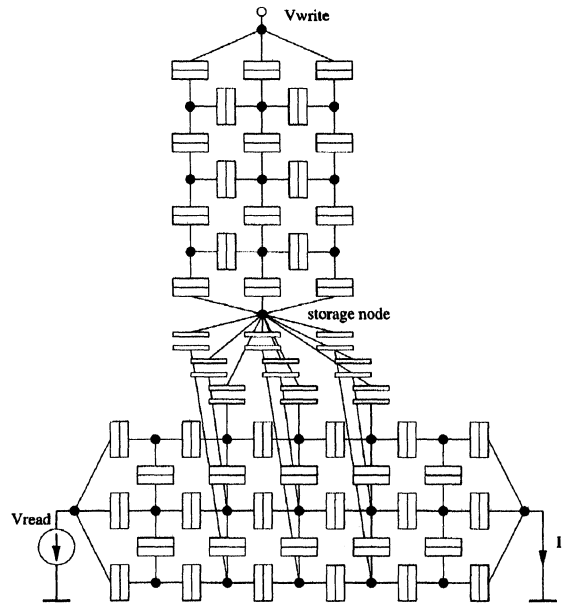

FIGURE 2 T-memory cell circuit.

since the granular film batches can have dimensions in the 100 nm regime, state-of-the-art optical lithography is sufficient to produce such memory cells.

Yano *et al.* [12] manufactured memory cells where the storage dots and read-out circuit are located in the same granular film, a poly-silicon film. The disadvantage of this design is, that it is much more difficult or even impossible to tune process parameters in order to change the characteristics of storing and reading separately. In our design, the granular films for the storing part and the read-out part could be produced with entirely different process parameters, thus optimizing each performance characteristics.

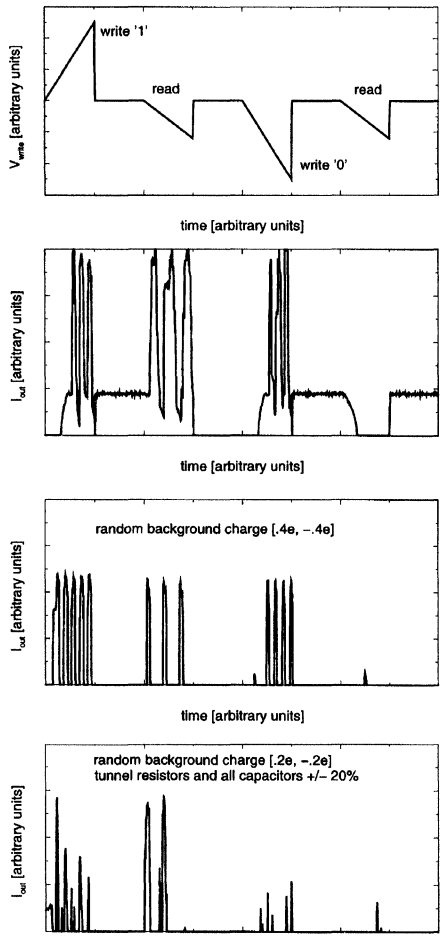

FIGURE 3 Writing and reading the *T*-memory cell.

We simulated the cell of Figure 2 and similar ones. In Figure 3 we give a typical write-read cycle for a '1' and a '0'. We simulated the same write-read cycle for different random background charges (Q_0 = 0, [0.2*e*, −0.2*e*], [0.4*e*, −0.4*e*]) and randomly changed tunnel resistors and capacitors. As can be clearly seen, the Coulomb oscillations are only present when a '1' was stored in the memory, independent of background charge.

5. CONCLUSION

We simulated and studied various single-electron memory designs. By analyzing proposed memories (flip-flop, electron trap, Q_0-independent memory, ...) we came up with a new memory cell, our so called *T*-memory cell. It is manufacturable with todays production methods, operates at room temperature, shows a strong background charge resistance, and is down-scalable to atomic dimensions.

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Author's Biography

Christoph Wasshuber received the *Diplomingenieur* and the Ph.D. degrees in micro-electronics and semiconductor-electronics from the Vienna University of Technology, Austria, in 1993 and 1997, respectively. He was for one and a half years with the *Asada Laboratory at the Tokyo University, Japan* studying single-electronics, and joined then the *Institut für Mikroelektronik* at the Vienna University of Technology. His current interests include modeling and simulation of single-electron devices, quantum effects in semiconductor devices, and computer aided engineering in VLSI technology in general.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the *Diplomingenieur* and the Ph.D. degrees in electrical engineering from the Vienna University of Technology in 1987 and 1992, respectively. He was one year with the *Institut für flexible Automation* and joined then in 1988 the *Institut für Mikroelektronik* at the Vienna University of Technology. Currently he is employed as an assistant professor heading the device modeling group.

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Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of *Diplomaingenieur* in Control Theory and Industrial Electronics from the Vienna University of Technology in 1978. Since that time he joined the *Institut für Allgemeine Elektrotechnik und Elektronik*, previously called the *Institut für Physikalische Elektronik*, at the Vienna University of Technology. He finished his thesis on "Two Dimensional MOS Transistor Modeling" in 1981. Dr. Selberherr has been holding the *venia docendi* on computer-aided design since 1984. He is the head of the *Institut fur Mikroelektronik* since 1988. Hiscurrent topics are modeling and simulation of problems for microelectronics engineering. He authored and coauthored more than 200 publications in journals and conference proceedings. Furthermore, he wrote a book *Analysis and Simulation of Semiconductor Devices*. Dr. Selberherr is member of the *Association for Computing Machinery* (1979), the *Society of Industrial and Applied Mathematics* (1980) and the *Verband deutscher Elektrotechniker*.