VLSI DESIGN
1998, Vol. 8, Nos. (1–4), pp. 111–115
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Cellular Automata Studies of Vertical Silicon Devices

M. SARANITI [a], G. ZANDLER [b], G. FORMICONE [a] and S. GOODNICK [a,*]

[a] *Electrical Engineering Department, Arizona State University, Tempe (AZ) 85287-6206;*
[b] *Physik Department and Walter Schottky Institut, TU-München, Garching, Germany*

We present systematic theoretical Cellular Automata (CA) studies of a novel nanometer scale Si device, namely vertically grown Metal Oxide Field Effect Transistors (MOSFET) with channel lengths between 65 and 120 nm. The CA simulations predict drain characteristics and output conductance as a function of gate length. The excellent agreement with available experimental data indicates a high quality oxide/semiconductor interface. Impact ionization is shown to be of minor importance. For inhomogeneous *p*-doping profiles along the channel, significantly improved drain current saturation is predicted.

Keywords: Cellular automaton, submicron MOSFET, Silicon, simulation, semiconductor device

1 INTRODUCTION

As a numerically very efficient discrete variant of the Monte Carlo (MC) technique [1], the CA [2] method significantly reduces the gap in computational speed between simulation techniques based on solving the full Boltzmann equation, and moment-based approaches such as the hydrodynamic method. The CA method is therefore particularly suited to simulate highly nonlinear charge transport, typical for the ultra-short devices described in this paper.

2 VERTICAL MOSFET

Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD) allow the realization of vertical devices with characteristic channel lengths well below 0.1 μm. Recently, CVD epitaxy was utilized to grow vertical MOSFET's with ultra short channels (see [3,4]). The epitaxially grown layer structures are selectively etched to a depth of 0.8 μm and thermally oxidized to grow the SiO_2 gate dielectric with a thickness of 5 nm. The quality of the oxide is comparable to planar structures. Figure 1 shows the cross section of such a vertical MOS [4]. The simulated geometry is shown on the left side of the figure, and corresponds to one half of the real device.

Devices with different doping levels and channel length were fabricated. The doping concentration in the source and drain n^+ regions are in the range $10^{18}\,cm^{-3} \div 2 \times 10^{19}\,cm^{-3}$, while the *p*-buffer layer contains an acceptor concentration of

* Corresponding author: Tel.: (602)965 2030, Fax: (602)965 8118 e-mail: saraniti@asu.edu.

$2 \times 10^{18}\,cm^{-3}$. These devices were grown with an effective channel length varying from 65 to 170 nm.

To investigate the influence of nonlinear transport on the electrical characteristics of such ultra short devices, we performed systematic calculations for all the realized structures and compare our results to experimental data. We further explore the influence of inhomogeneous *p*-doping along the channel in improving the drain current saturation behavior.

2.1 Current-Voltage Curves

As a critical test for the nominal geometry settings like oxide thickness and *p*-doping level, we have compared the experimental and calculated sub-threshold behavior of the devices described above. Excellent agreement was obtained for several devices with different geometries and doping concentrations, which indicates that the nominal and technologically realized values of the geometry agree well with each other. This is exemplified in Figure 2 for the 65 nm CVD vertical MOSFET structure. There, the applied drain voltage is 0.5 V.

Based on these geometries, we investigated the drain current saturation behavior of the vertical MOSFET for different channel lengths. Figure 3 shows the output current versus drain voltage for three different channel lengths of 170 nm, 120 nm and 65 nm, respectively. The bias of the gate was fixed to the value of 2 V. Clear drain current saturation behavior is found even for the ultra-short, 65 nm device. The increasing output current

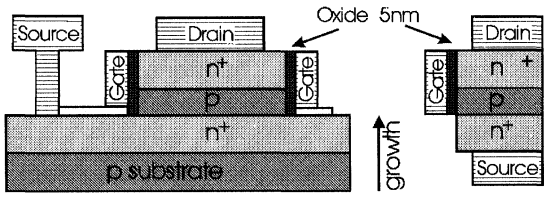

FIGURE 1 Layout of the vertical CVD-EPI MOS. The growth direction is shown, while the equivalent simulated region is on the right side.

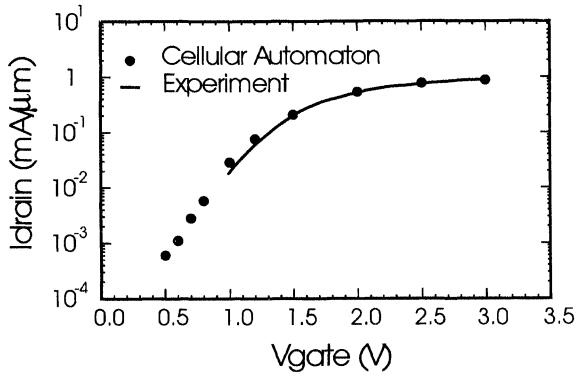

FIGURE 2 Sub-threshold output current of the simulated device versus gate voltage when a low ($V_D = 0.5$ V) drain bias is applied.

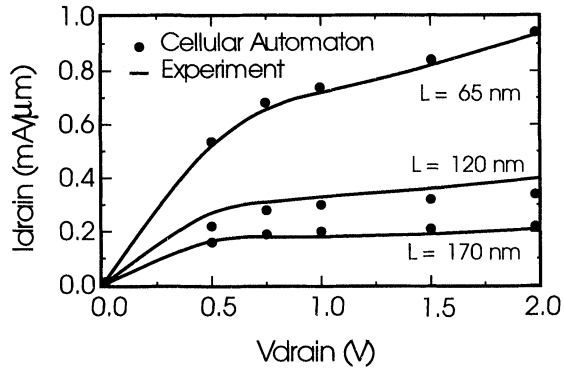

FIGURE 3 Computed (points) and experimental (full lines) current-voltage characteristics with decreasing channel length at $V_G = 2$ V gate bias.

and output conductance with decreasing channel length reflect a strong barrier reduction at the source junction. Nevertheless, even for high bias condition, no parasitic charge transport occurs in the bulk parallel to the conduction channel. The increase of drain current and output conductance due to the electrostatic effects mentioned above are further enhanced by velocity overshoot in the shorter channels. This velocity overshoot is driven by a high, inhomogeneous electric field along the channel. For the 65 nm *n-p-n*$^+$ structure biased at $V_D = V_G = 2$ V, we find a peak value of 800 kV/cm at the n^+p drain junction.

For this bias condition, the average electron velocity in the conduction channel of the 65 nm device is shown in Figure 4. Pronounced velocity overshoot is evident all along the conduction channel, the maximum velocity being reached at the drain end of the *p*-buffer, where it peaks to a value of three times the saturation velocity in homogeneous Si.

The overall agreement for the complete current–voltage characteristics between the CA results and experimental data is exemplified for the 70 nm device in Figure 5. For this device, simulations were performed up to a bias value of $V_D = 2.5$ V, to investigate the occurrence of impact ionization at higher bias. Up to the highest bias point shown, negligible contributions due to impact ionization were found. However, this process becomes important at higher drain bias. Analogous results were found for the 65 nm device.

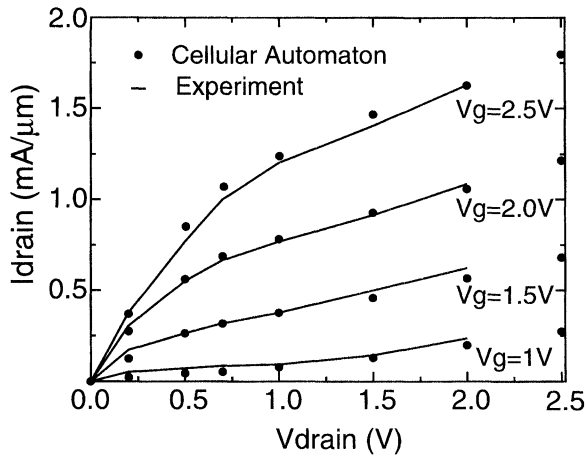

FIGURE 5 Computed (points) and experimental (full lines) current–voltage characteristics of the 70 nm vertical MOSFET.

2.2 Bulk Effects

The potential barriers due to the *np* (source) and *pn* (drain) junctions prevent a parasitic bulk current from flowing parallel to the channel inversion layer. At the same time, the electric field due to these junctions can reach high values, giving rise to impact ionization or even field breakdown. Optimization of such devices must account for the electrostatic behavior of the bulk region in order to improve saturation and avoid impact ionization at a given operating bias. Figure 6 (left) shows the concentration of carriers in the bulk 65 nm n^+pn system when a bias of 2 V is applied between the *n* and n^+ regions corresponding to the source and drain of the device shown in Figure 1. The fact that the potential barrier due to the *npn* junction (Fig. 6) is still intact at this drain bias ensures that no parasitic bulk current is flowing.

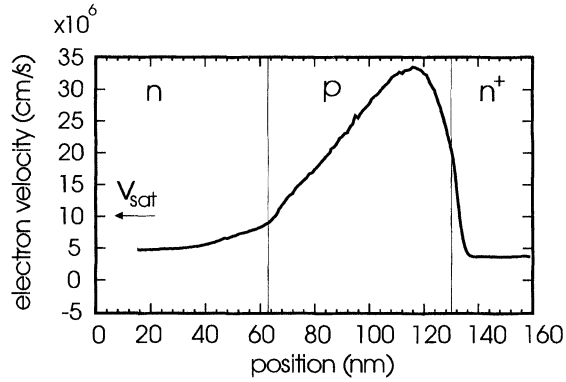

FIGURE 4 Average drift-velocity of electrons in the CVD-EPI MOSFET of Figure 1; a pronounced velocity overshoot is evident in the *p*-buffer.

2.3 Design Optimization

In order to improve the saturation behavior of the vertical MOSFET, an additional 20 nm p^+-buffer was introduced in the central *p*-region. The chosen

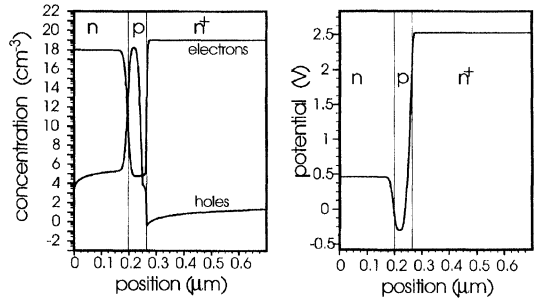

FIGURE 6 Carrier concentration (left) and potential profile (right) in the bulk *n-p-n* structure present in the vertical 65 nm MOSFET.

doping concentration in this p^+-buffer is $3\times10^{18}\,cm^{-3}$. The buffer was placed 10 nm from the *n-p* source junction. The buffer extension and position were optimized to reduce the influence of the drain potential on the output current, thus improving the saturation behavior. Its separation from the *n-p* source junction keeps the value of the junction field low enough to avoid impact ionization. Additionally, punch-through action is reduced due to the higher doping, which is crucial for devices with shorter channels. The drain current reduction due to the presence of the buffer was compensated by reducing the oxide thickness to 4 nm.

Simulation results for the device with the p^+-buffer are compared in Figure 8 with measurements made on a transistor with a homogeneously doped channel. The saturation behavior is remarkably improved compared to the characteristics shwon in Figure 5, and the reduced oxide thickness completely compensates the current reduction due to the p^+-buffer.

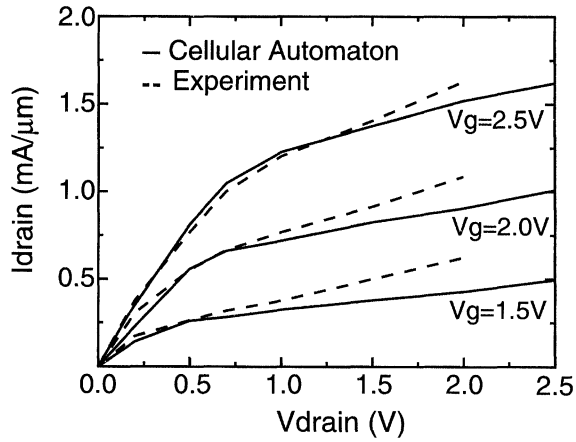

FIGURE 8 Improved saturation behavior of the simulated MOSFET after adding an additional 20 nm p^+ buffer. The simulation results (full lines) are compared with experimental data of Figure 5.

3 CONCLUSIONS

The capability of the CA approach to accurately predict highly nonlinear transport behavior and the resulting electrical characteristics in real nanostructured semiconductor devices was demonstrated. A novel family of vertical MOSFET's was investigated, giving results which are in excellent agreement with the experiments. The crucial role of the bulk parasitic conduction was stressed, and an optimized device design was proposed which improves the overall performance of the device.

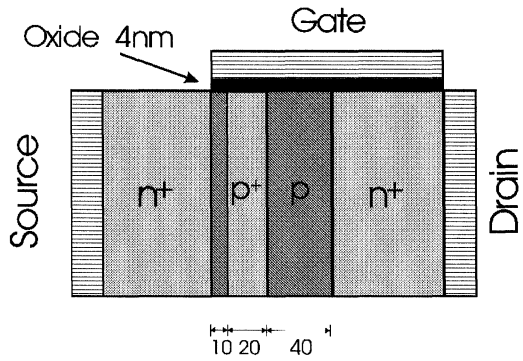

FIGURE 7 Cross-section of the saturation optimizing geometry. A $3\times10^{18}\,cm^{-3}$ p^+-buffer is included within the central *p* region.

Acknowledgements

The authors would like to thank Peter Vogl for his valuable suggestions. This work was partially supported by the NSF, grant ECS-9312240, and by the Siemens project SFE.

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Authors' Biographies

Macro Saraniti received on April 1991 the Laurea degree in Physics from the University of Modena (Italy). In 1996 he received his Ph.D. in Physics from the Technical University of München (Germany) with a thesis on "Development of efficient numerical techniques for semiconductor device simulations". He is currently Faculty research associate of the Electrical Engineering Department of Arizona State University. His research interests are related to the numeric aspects of semiconductor devices simulation, as well as to the analysis and design of Si and GaAs ultra-short devices.

Günther Zandler received his Ph.D. from the University of Innsbruck, Austria, in 1989. In 1988, he became research associate at the Institute for Experimental Physics at the University of Innsbruck. In 1989 he joined the Physics Department of the Technical University of Munich as research associate for theoretical semiconductor physics. His research interests focuse on the simulation of electron devices, high field transport and ultrafast phenomena in bulk and nano-structured semiconductors.

Gabriele Formicone received the Laurea in Physics from the University of Roma (Italy) "La Sapienza" in June 1994, and the M.S. Degree in Electrical Engineering from Arizona State University in December 1996. He is also enrolled in the Ph.D. Degree at ASU, where he has been Graduate Research Assistant from June '94 to June '97. Currently he is Simulation Engineer at the Communication Products Laboratories, Motorola. His interests are devoted to the many aspects of physics and transport in submicron Si/SiGe devices and heterojunctions.

Stephen Goodnick received his B.S. degree in Engineering Science from Trinity University in 1977, and his M.S. and Ph.D. in Electrical Engineering from Colorado State University in 1979 and 1983 respectively. He was an Alexander von Humboldt Fellow at the Technical University of Munich, Germany and the University of Modena, Italy in 1985 and 1986. He was the Melchor visiting chair at the University of Notre Dame in 1991. He was a faculty member from 1986 to 1997 in the Department of Electrical and Computer Engineering at Oregon State University, Corvallis, Oregon, where he held the rank of Professor. He is presently Chair and Professor of Electrical Engineering at Arizona State University. Dr. Goodnick is a senior member of IEEE, a member of the American Physical Society, Sigma Xi, Eta Kappa Nu and Blue Key National Honor Society. He has co-authored over 70 journal articles and book chapters related to transport in semiconductor devices and microstructures.