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Preface

This special issue of the VLSI DESIGN: an International Journal of Custom-chip Design, Simulation and Testing is devoted to the special issue of "Physical Design in Deep-Submicron".

The goal of this special issue is to explore physical level solutions to the deep submicron (0.25 micron meter or below) problems.

In deep submicron designs, physical interconnections delay will overtake gate delays as a design concern by the year 2000, mandating a shift in the physical design flow for deep-submicron. In a typical deep submicron process, approximately 70% of the signal delay is due to interconnect and only 30% due to the gate driving the interconnect. Therefore, we predict that iterations between synthesis and layout increase dramatically due to timing and routability problems.

The key to solving this problem is knowing more about the physical design, *i.e.*, placement and estimated interconnect, early in the design cycle. The RTL is being defined to accurately predict size, timing and power, early in the design cycle and avoid downstream iterations. This means the design engineer needs to get back to the fundamentals of physical designs.

In this special issue, this kind of problems arisen in VLSI deep-submicron interconnection designs are described and their state-of-the-art techniques are demonstrated in the following 8 papers.

Performance improvement of VLSI fabricated in deep submicron technology depends on the delay of interconnects. As the amount of interconnects between devices grows super linearly with the number of transistors, the chip area is dominated by interconnects. The challenging approach is to develop synthesis methods integrating logic and layout synthesis steps. The first paper by Malgorzata Chrzanowska-Jeske, Yang Xu, and Marek Perkowski addresses "Logic Synthesis for a Regular Layout". The paper presents very interesting ideas which lead to new practical approaches to merging logic synthesis and layout.

The second paper by Dirk Stroobandt, Jan Van Campenhout addresses "Accurate Interconnection Length Estimations for Predictions Early in the Design Cycle". They improved the Donath's method for before-placement-estimation of average length of wires, to be used in applications in physical design of large Standard Cell or Gate array circuits. This is a very important topic in practice. The empirical error in the Donath's method is almost completely corrected in their experiments.

In the physical implementation of deep-submicron IC's, placement solution quality is a major determinant of whether timing correctness and routing completion will be achieved. The third paper by Maogang Wang, Prithviraj Banerjee and Majid Sarrafzadeh addresses "Placement with Incomplete Data". The paper addresses a new problem in a placement that will arise along with the increasing complexity of current deep submicron designs. Such a complicated design will typically take 2 to 3 years to complete. In the first 2 years, a detailed net list is not available. The paper addresses a layout estimation methodology for the incomplete netlists.

The fourth paper by C. J. Albert, A. E. Caldwell, T. F. Chan, D. J.-H. Huang, A. B. Kahng, I. L. Markov and M. S. Moroz addresses "Analytic Engines are Unnecessary in Top-Down Partitioning-Based Placement". Due to its speed and "global" perspective, the quadratic placement methodology has been widely adopted in industry. The paper revisit the quadratic placement methodology and develop insights into its effective implementation.

Placements of blocks on a 2 dimensional surface minimizing chip area and wirelength is one critical process in VLSI layout design. The fifth paper by Jun Xu, Pei-Ning Guo and Chung-Kuan Cheng addresses "Empirical Study of Block Placement by Cluster Refinement". The algorithm improves the previously known algorithms.

In ultra-deep submicron design (*i.e.*, 0.25 um and below), parasitic capacitance and resistance effects begin to dominate. Thus, recently deep submicron designs require routing methodologies to reduce coupling-capacitances (called crosstalk). As CMOS technology advances, intrinsic gate delay decreases and interconnect wire delay increases with respect to overall circuit delay. The coupling capacitance between minimum pitch wires on a 0.25 um CMOS IC can account for over 80% of the total capacitance of a wire. This makes interconnect crosstalk noise one of the biggest challenges in VLSI design today. The sixth paper by Su-Hyun Nam, Jun-Dong Cho and Dorothea Wagner addresses "Lower-Power and Min-Crosstalk Channel Routing for Deep-Submicron Layout Design" that discusses the noise problem from a layout designer's point of view.

With technology scaling, the selection of line thicknesses, widths and spacings in multi-layer interconnect to simultaneously optimize signal distribution, signal performance, signal integrity, and interconnect reliability is increasingly critical.

The seventh paper by Andrew Kahng, Sudhakar Muddu and Egino Sarto addresses "Tuning Strategies for Global Interconnects in High-Performance Deep-Submicron ICs". The paper center on global wiring layers and interconnect tuning issues related bus routing, repeater selection, and choice of shielding/spacing rules for signal integrity and performance.

Steadily shrinking process technologies and ever-increasing design sizes require new verification tools to address the complexities of ultra-deep submicron design. The eighth paper by Wonjong Kim and Hyunchul Shin addresses "Hierarchical Restructuring for Hierarchical LVS (Layout vs schematic) Comparison". The paper addresses a new hierarchical comparison method with less time and less storage for computing.

In conclusion, the above commissioned papers in this special issue are intended of current issues and future applications of deep submicron VLSI interconnections.

The trend helps to further improve the high performance systems, but much work may remain to be done to improve such techniques to be more practical.

The editor is most grateful to the authors of the papers cited above, especially Prof. Malgorzata Chrzanowska-Jeske, Dr. Dirk Stroobandt, Prof. Majid Sarrafzadeh, Prof. Andrew B. Kahng, Prof. Chung-Kuan Cheng, and Prof. Hyunchul Shin, each of who is willing to contribute the paper to the special issue and who is one of leaders in their respective fields of expertise.

Especially, I would like to announce that Prof. Andrew B. Kahng and Dr. Dirk Stroobandt are now initiating a workshop on System-Level Interconnect Prediction which will take place in April 10 and 11, 1999 in Monterey (the weekend before the International Symposium on Physical Design). This workshop is a new forum for the exchange of ideas related to estimation of interconnect design parameters in VLSI CAD applications (http://www.elis.rug.ac.be/~dstr/SLIP.html).

I would also like to thank DR. George W. Zobrist, the Editor-in-Chief of VLSI DESIGN, and Prof. Majid Sarrafzadeh, the associate Editor of IEEE Transactions on CAD of Integrated Circuits, for their enthusiasm, encouragement, and support of this special issue.

My thanks are due as well to those people behind the success, those anonymous reviewers, whose selfless, dedicated, and fairly professional comments to authors contributed to this special issue.

Guest Editor's Biography

Prof. Jun-Dong Cho was born in Seoul, Korea. He received the B.S. degree in electronics from Sung Kyun Kwan University, Seoul, Korea, in 1980, the M.S. degree from Polytechnic University, Brooklyn, NY, in 1989, and the Ph.D. degree from Northwestern University, Evanston, IL, in 1993, both in computer science.

He was a Senior CAD Engineer at Samsung Electronics, Co., Ltd., Buchun, Korea. Since 1995, he has been Assistant Professor of Electronic Engineering, Sung Kyun Kwan University, Suwon, Korea.

His research interests are in the area of VLSI CAD algorithms, low power digital designs.

He has been a guest editor of VLSI DESIGN: An International Journal of Custom-Chip Design, Simulation, and Testing for the special issue in High performance Design Automation for VLSI Interconnects, 1998. He has also been serving on a guest-editor of an International Journal of High-Speed Electronics and Systems for the special issue in High Performance Design Automation of MCMs and Packages, 1996.

He received the Best paper award at the 1993 Design Automation Conference in the area of physical design.

He has a book "High-Performance Design Automation of MCMs and Packages", World Scientific, 1996, and the co-author of an invited chapter in Encyclopedia of Electrical and Electronics Engineering in the area of VLSI Circuit Layout, published on April, 1999.

He serves on the technical committee of the Ninth International Conference on VLSI Design, 1996 and 1997, and Ninth International Conference on VLSI Design, 1996 and 1997, and IEEE MultiChip-Module Conference, 1996 and 1997.

He has also chaired a session in International Symposium on Physical Design, Nappa Valley, April, 1997, and International Conference on VLSI and CAD, Seoul, Sep. 1997, respectively.

He is currently serving as an associate editor of Institute of Electronic Engineer of Korea, and Journal of Electrical Engineering and Information Science. He is now organizing for Korean CAD and VLSI Design Workshop, May '99 and serving as a technical committee member of International Conference on VLSI and CAD, Seoul, Nov. 1999.

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