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Accurate Interconnection Length Estimations for Predictions Early in the Design Cycle

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Important layout properties of electronic circuits include space requirements and interconnection lengths. In the process of designing these circuits, a reliable pre-layout interconnection length estimation is essential for improving placement and routing techniques. Donath found an upper bound for the average interconnection length that follows the trends of experimentally observed average lengths. Yet, this upper bound deviates from the experimental value by a factor $\delta \approx 2$, which is not sufficiently accurate for some applications. We show that we obtain a significantly more accurate estimate by taking into account the inherent features of the optimal placement process.

Keywords: Interconnection length estimates, Donath's hierarchical placement, Rent's rule, occupancy probability

1. INTRODUCTION

The production of VLSI and ULSI computer chips requires the layout (placement and routing) of the (logical) chip design onto a physical carrier. With the advent of high level description languages such as VHDL, with the extensive use of component libraries, and with the standardization of production parameters, more and more steps in the design cycle are being automated. In the early days of chip design, designing a chip manually was still feasible. Nowadays, computer aided design (CAD) tools are indispensable to cope with the complexity and the limited time resources. For the placement and routing phases, the quality requirements are particularly stringent. For the results of these phases to be good enough, accurate predictions of relevant post-layout circuit properties are an absolute necessity to limit the search in the vast solution space. Hence, CAD tools use estimator tools [1–4], usually based on partitioning methodologies [5].

The main circuit parameters that have to be estimated are the interconnection length in the placed design, area occupancy, attainable clock frequency, power dissipation, and (especially for

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some types of gate arrays) channel densities. The estimation is intended to be performed before the circuit is actually placed (*a priori* estimation) and is then used to obtain better layouts [3]. The estimates also provide deeper insight in the placement properties of circuits on different carriers, *e.g.*, three-dimensional architectures, where optical channels could be used for the third dimension interconnections [6–8]. The possibilities of such architectures can be explored without the need to actually build the systems.

With physical feature sizes decreasing rapidly, the time delay of electrical signals travelling in the inter-connect between active devices and gates is approaching and even surpassing the delay through the devices and gates. The estimation of the interconnection length early in the design cycle therefore gains importance as an aid for floorplanning, placement, and routing tools. The accuracy of the estimates is of crucial importance to the final design result. *A priori* interconnection length estimation will become an essential step in designing systems that have to meet stringent performance criteria.

There have been a few attempts to predict interconnection lengths. A first upper bound for interconnection lengths has been found by Sutherland and Oestreicher [9]. Since it is based on a random placement, it yields excessively large estimates. Donath [1,10] found that a hierarchical placement technique gives much better interconnection length estimates and his results have been used by several other researchers [3, 11–15]. Recently, Van Marck and Stroobandt have extended Donath's technique to three-dimensional and anisotropic architectures [7, 8], Stroobandt and Kurdahi have included models for multi-terminal nets [16, 17], and Stroobandt has added the estimation of external interconnection lengths [18]. Comparable work has been done by Ozaktas [19], who investigates optical architectures, based on interconnection models. Independently from Donath, Masaki and Yamada [20] derived the same interconnection length distributions and added three-dimensional extensions. Davis *et al.* [15] calculated Donath's wire length distribution in somewhat more detail.

Almost all recent papers on wire length estimates are based on Donath's pioneering research. They produce the same valuable results but they also have the same deficiencies. Donath estimates the average interconnection length using a model for the interconnection complexity of the circuit, known as Rent's rule [21]. Experimentally measured average interconnection lengths vary with the number of logic gates in a circuit and with the interconnection complexity of the circuit. Donath found that his theoretically obtained average interconnection length values appeared to follow these variations [1]. However, Donath's calculated average interconnection length and the actual one still differ by a factor $\delta \approx 2$. His method indeed results in an upper bound for the average interconnection length. We would like to estimate the average interconnection length more accurately. Therefore, it is important to understand the underlying mechanisms that cause the overestimation in Donath's calculation.

In this paper, we show that the discrepancy between the theoretical estimates and the experimentally measured values is primarily due to the lack of accuracy in the placement model used by Donath. We consider this issue in Section 4, and in Section 5, we present a way to introduce a new placement model efficiently. This leads to a better estimation for the average interconnection length (Section 6), as will be verified experimentally in Section 7. But first, we explain the circuit model and the key issues of Donath's placement technique.

2. MODEL FOR THE CIRCUIT, THE PARTITIONING PROCESS, AND THE PHYSICAL ARCHITECTURE

A circuit can be represented by a set of interconnected blocks as in Figure 1 (the blocks can be the representation of transistors, gates, or even entire circuits). An interconnection between blocks

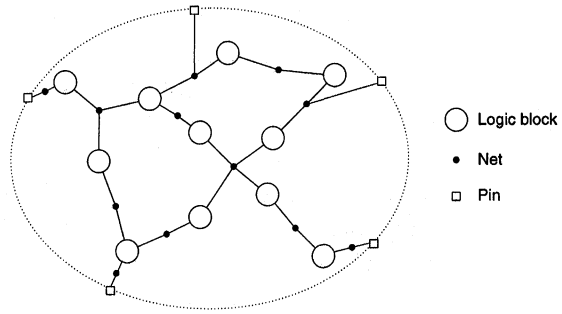

FIGURE 1 Model of a circuit.

is called a *net*. A net that is connected to more than two blocks is called a *multi-terminal net*. Some of the nets are also connected to the outside of the circuit. These are called *external nets* (as opposed to *internal nets* which only connect to blocks within the circuit). In order to model these external nets properly, we introduce a new kind of block and call it a *pin*. A pin models the external terminal for the net. The other (internal) blocks are called *logic blocks*. Every external net is connected to exactly one pin. Note that the number of pins thus equals the number of external nets.

Partitioning a circuit means dividing this circuit into disjoint subcircuits (called *modules*), each containing a subset of the blocks (Fig. 2). This partitioning is guided by some kind of criterion. Generally, the criterion is to minimize the number of nets crossing the borders of modules in the partition. Nets that are cut by module boundaries are shared between two or more modules and are said to be external to the modules. Therefore, the net is split into a number of subnets, one for each module that shares the net. A new pin is assigned to each subnet. Each module can then itself be seen as a circuit and can be partitioned further. A partitioning process where the modules themselves are recursively partitioned is called a *hierarchical partitioning method.*

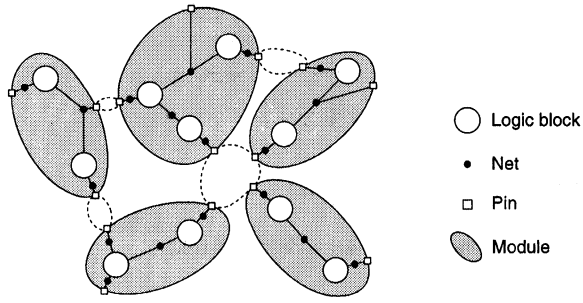

FIGURE 2 Partitioning the circuit of Figure 1 into modules.

In partitioned circuits, a relationship exists between the number of elementary blocks B in a module and the number of the module's external connections (pins) P. It is known as Rent's rule [21]:

$$P = T_b B^r \quad (0 < r < 1), \tag{1}$$

where T_b is the average number of terminals per elementary block and r is called the Rent exponent. This exponent is a measure of the interconnection complexity of the circuit [19]. Its value increases for increasing interconnection complexity. Generally, r varies from around 0.5 for simple regular circuits (such as Random Access Memories), up to 0.75 for complex circuits (such as fast full custom VLSI circuits) [22]. The validity of Rent's rule is related to the fact that designers tend to build their circuits hierarchically, roughly exhibiting the same complexity at each level of hierarchy. Rent's rule seems to apply to nearly all circuits. Figure 3 shows the results of a circuit

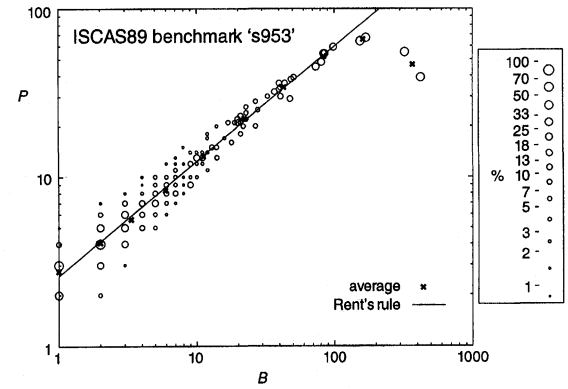

FIGURE 3 Number of pins P versus number of blocks B for every partition during the 'ratiocut' partitioning of the ISCAS89 benchmark circuit 's953', compared to Rent's rule. The size of the circles corresponds to the percentage of modules that has P pins and B blocks in a pool of modules around an average number of blocks.

partitioning according to the 'ratiocut' partitioning method [23]. Rent's rule can be observed easily (especially when considering the average values) and the Rent exponent is found to be 0.68.[1]

The model for the circuit alone does not enable us to estimate interconnection lengths since these only get their meaning after the placement of the circuit in a physical architecture or carrier. The physical architecture often is a regular structure (in gate arrays and standard cell layout) or can be modelled as one (as a first order approximation). We therefore model it as a square (part of a) Manhattan grid (Fig. 4(b)). In this grid, each gridpoint (*cell*) corresponds to a location where one logic block of the circuit can be placed. The gridlines correspond to the *channels* in which the connections between the gates can be routed. All lengths are thus measured using a Manhattan metric.

3. DONATH'S TECHNIQUE

3.1. Hierarchical Placement

Donath's technique to estimate the average interconnection length is based on a hierarchical placement of the circuit into a square Manhattan grid [1]. The circuit is partitioned hierarchically into subcircuits. Each subcircuit at a hierarchical level consists of four subcircuits (of equal size) at the next (lower) level of hierarchy (Fig. 4(a)). We thus assume that the number of gates in the circuit is a power of 4 (there are 4^K gates, with K the number of hierarchical levels). The circuit is placed in a square Manhattan grid, which is also partitioned into four subsquares of equal size (Fig. 4(b)).

In Donath's partitioning and placement scheme, each subcircuit is assigned recursively to a subsquare until all gates are assigned to exactly one grid location. The recursion levels will be numbered $K-1$ (four subcircuits that constitute the entire circuit) down to 0 (four subcircuits consisting of only one logic gate). Note that external interconnections are not included in the estimations (these interconnections belong to level K and are considered in [18]).

The partitioning of the circuit into four subcircuits of equal size should be done in such a way that the partition satisfies Rent's rule. That is, we want to keep the number of interconnections between the subcircuits as small as possible. This is a necessary condition if we want our placement scheme to be a good model for the *optimal*

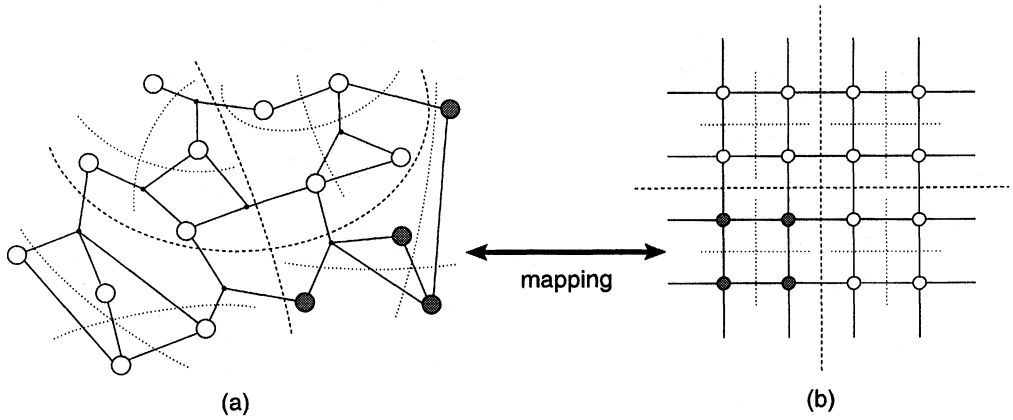

FIGURE 4 Recursive partitioning scheme of the circuit (a) and the physical architecture (b).

[1]The deviation from Rent's rule at the partitioning levels with very large module sizes is explained in [21, 24]. In this paper, we will not elaborate on this issue.

placement of the circuit. We define an optimal placement as one that minimizes the total interconnection length. It is indeed obvious that such a placement tries to place densely interconnected logic gates as close as possible, resulting in clusters of such gates. Among clusters, there are fewer interconnections. A placement scheme that keeps the number of interconnections between the subcircuits as low as possible thus leads to many short interconnections and few long ones. This behaviour is modelled accurately by the module pin numbers following from Rent's rule.

3.2. Average Interconnection Length

Given the above model for the circuit, the physical architecture and Donath's placement, we want to find the average interconnection length. We can do this by calculating the average number of interconnections N_k and the average length of the interconnections l_k at every hierarchical level k ($0 \leq k \leq K-1$). The average interconnection length L (in number of cell pitches), computed over all hierarchical levels, is then given by

$$L = \frac{\sum_{k=0}^{K-1} N_k l_k}{\sum_{k=0}^{K-1} N_k}. \tag{2}$$

The computations of N_k and l_k are performed for point-to-point interconnections only (as in [1]). This simplification is based on the knowledge that these nets outnumber all other nets in circuits and that multi-terminal nets can be modelled as a collection of point-to-point nets by pairwise connecting some of the net terminals until a path exists between every pair of terminals (possibly *via* other terminals). This simplification somewhat shortens the average wire length but it does not have too much influence on the average values computed in this section. In [16, 17], Stroobandt and Kurdahi present a possible way of including multi-terminal nets into the calculations. In order to keep the reasoning clear, we will not consider this extension in this paper.

The expected number of interconnections at each level of the hierarchy can be calculated using Rent's rule and can be seen to be [1]

$$N_k = \alpha T_b 4^K (1 - 4^{r-1}) 4^{k(r-1)}, \tag{3}$$

where, according to Donath, $\alpha \approx 1/2$ more or less models the presence of multi-terminal nets.

We now seek to find the average interconnection length l_k for point-to-point interconnections at hierarchical level k. The interconnections belonging to hierarchical level k are those interconnections between logic blocks belonging to the same $(k+1)$-th level hierarchical subcircuit, but to different k-th level hierarchical subcircuits. Those interconnections thus connect two gates placed in different squares at hierarchical level k. Only two different combinations are possible: either the squares are adjacent or they are diagonally opposed (Fig. 5). We will call the first combination an A-*combination*, the second one a D-*combination*. For each of these combinations, we compute the average interconnection length (denoted as $l_{k,a}$ for A-combinations, $l_{k,d}$ for D-combinations). For this, it is assumed that the starting points and the endpoints of the interconnections between two squares are uniformly distributed over those squares (from now on, we indicate starting points and endpoints of interconnections as *interconnection points*). The enumeration of all possible lengths (distances between interconnection points) for the two combinations on every hierarchical level k, is straightforward. The distributions are given by [14]

$$S_{k,a}(l) = \begin{cases} \frac{-l^3+3\lambda l^2+l}{3\lambda^4} & (0 \leq l < \lambda) \\ \frac{2l^3-12\lambda l^2+(21\lambda^2-2)l-9\lambda^3+3\lambda}{3\lambda^4} & (\lambda \leq l < 2\lambda) \\ \frac{-l^3+9\lambda l^2-(27\lambda^2-1)l+27\lambda^3-3\lambda}{3\lambda^4} & (2\lambda \leq l < 3\lambda) \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

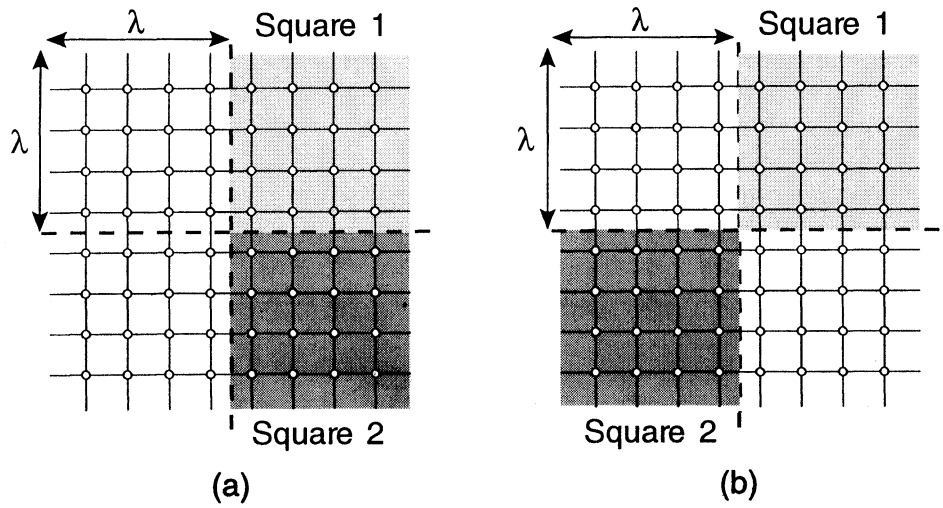

FIGURE 5 Two possible combinations at a hierarchical level k: an A-combination (a) and a D-combination (b).

for an A-combination, and

$$S_{k,d}(l) = \begin{cases} \frac{l^3-l}{6\lambda^4} & (0 \le l < \lambda) \\ \frac{-3l^3+12\lambda l^2-(12\lambda^2-3)l+4\lambda^3-4\lambda}{6\lambda^4} & (\lambda \le l < 2\lambda) \\ \frac{3l^3-24\lambda l^2+(60\lambda^2-3)l-44\lambda^3+8\lambda}{6\lambda^4} & (2\lambda \le l < 3\lambda) \\ \frac{-l^3+12\lambda l^2-(48\lambda^2-1)l+64\lambda^3-4\lambda}{6\lambda^4} & (3\lambda \le l < 4\lambda) \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

for a D-combination. In these equations, the squares have size λ^2 (Fig. 5) with $\lambda = 2^k$.

The expected value for the average length in a certain combination at a hierarchical level k then equals (with $C \in \{a, d\}$)

$$l_{k,C} = \frac{\sum_{l=0}^{4\lambda} l\, S_{k,C}(l)}{\sum_{l=0}^{4\lambda} S_{k,C}(l)} \tag{6}$$

and results in

$$l_{k,a} = \frac{4\lambda}{3} - \frac{1}{3\lambda} \tag{7}$$

$$l_{k,d} = 2\lambda, \tag{8}$$

with $\lambda = 2^k$. A more efficient way of calculating these average wire lengths makes use of *generating polynomials* and is presented in [25].

Since there are four A-combinations and two D-combinations, the total average interconnection length l_k at the hierarchical level k is given by

$$l_k = \frac{4l_{k,a} + 2l_{k,d}}{6}. \tag{9}$$

Combining Eq. (2) through 9 yields

$$L = \frac{14H(K,r,1) - 2H(K,r,3)}{9H(K,r,2)}, \tag{10}$$

with

$$H(K,r,x) = \frac{2^{K(2r-x)} - 1}{2^{2r-x} - 1}. \tag{11}$$

Note that this function should be extended continuously in the singular point $r = x/2$.

3.3. Asymptotic Behaviour

The calculations from the previous section show a different scaling behaviour for different Rent

exponents. With the total number of logic blocks (or gates) G equalling 4^K, the scaling behaviour is given by

$$\begin{cases} L \sim G^{r-\frac{1}{2}}, & r > 0.5 \\ L \sim \log(G), & r = 0.5 \\ L \sim f(r), & r < 0.5 \end{cases} \tag{12}$$

where $f(r)$ is independent of the number of blocks G. The Rent exponent thus plays an important role. For complex circuits ($r > 0.5$), the average length increases with the size of the circuit, whereas it is independent of circuit size for circuits of modest complexity ($r < 0.5$).

4. A CRITIQUE OF DONATH'S APPROACH

Donath reported a good resemblance between theoretical and experimental scaling behaviour but a more or less constant deviation between theory and experimental results of a factor of approximately 2 [1] (see Fig. 6). In order to be able to predict interconnection lengths more accurately, it is important to understand the underlying reasons for this.

Donath's estimation technique is primarily based on his hierarchical placement scheme. Every hierarchical level is treated separately without any knowledge on the length of interconnections from other levels of hierarchy. Donath simply assumes that the interconnection points are uniformly distributed over the gates of the square grid. It is nevertheless clear that an optimal placement strategy will place interconnected logic gates as close as possible, regardless of the hierarchical level the interconnection belongs to. This means that an optimal placement procedure will place gates that are interconnected to a gate of another square (at level k) preferably near the (common) border of the two squares (as shown in Figs. 7 and 8 for the two combinations; the darker the zone, the higher the number of interconnection points). Consequently, the interconnections at lower levels (*e.g.*, $k-1$) will be placed at the center of the square at level k which is, again, the border of a square at level $k-1$. This clearly represents the optimal placement behaviour. Donath's technique does not take full account of this information. On the contrary, the assumption of a uniform distribution of interconnection points models a random placement at each level. The average interconnection length found by Donath therefore remains an upper bound for the real value.

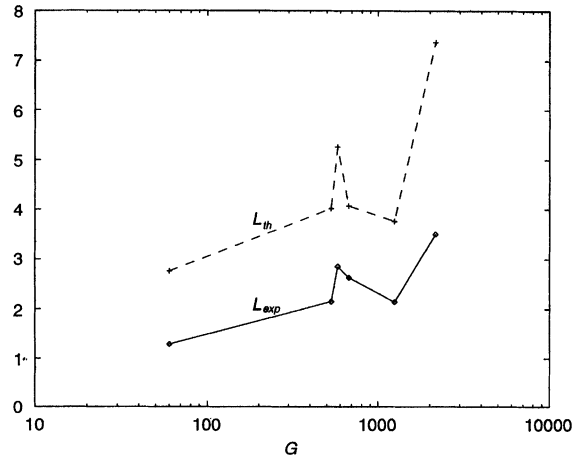

FIGURE 6 Comparison between Donath's average wire length L_{th} and experimentally measured average wire lengths L_{exp} for circuits of varying size (according to the data provided by Donath in [1]).

5. REFINING DONATH'S MODEL

5.1. Definitions

We define an *interconnection length distribution* as a collection of values, indicating, for each length l, how many interconnections have this length. The sum of these values over all lengths l equals the total number of interconnections. The *normalized distribution* denotes, for each length l, the fraction of interconnections that has length l. The *global distribution* is defined as the interconnection length distribution of the entire circuit. The global distribution contains information about all interconnections considered together. At each hierarchical level, we can also define a *local distribution*. Such a distribution only contains information about interconnections at a specified hierarchical level.

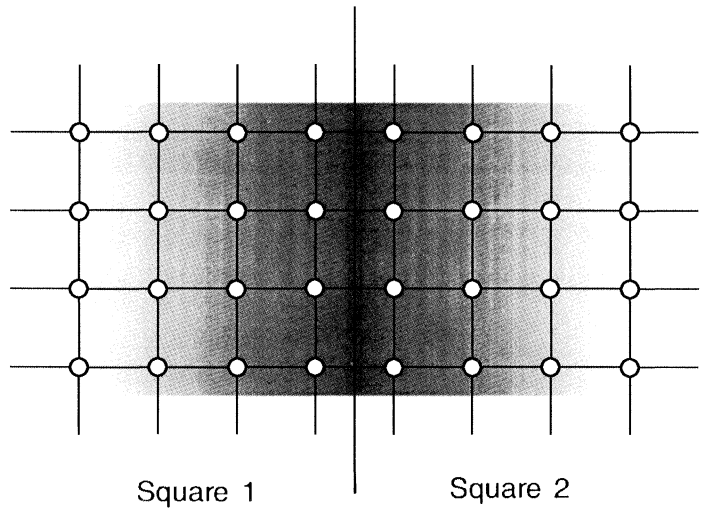

FIGURE 7 The placement of interconnection points in an A-combination (darker zones contain more points).

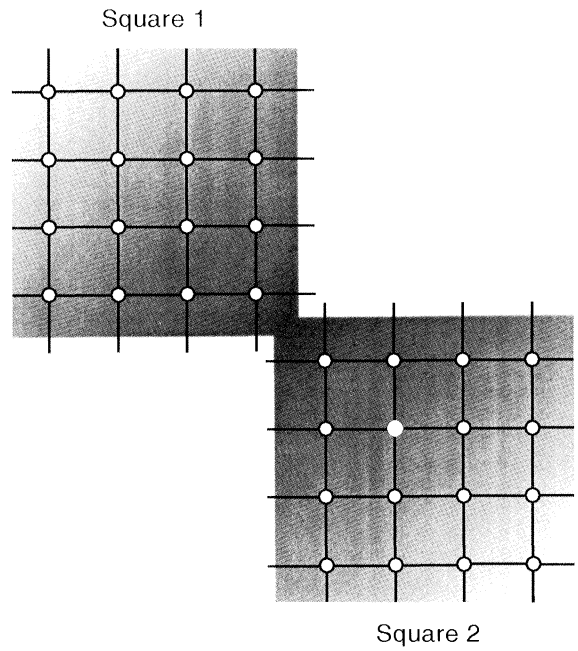

FIGURE 8 The placement of interconnection points in a D-combination (darker zones contain more points).

5.2. Stochastic Model of the Placement Process

A physical placement of a netlist[2] is a list of N pairs of points $\mathcal{P}_N = ((P_1, Q_1), \ldots, (P_N, Q_N))$ in the physical architecture (Manhattan grid). Each pair represents a connection to be routed. Both the number of pairs N and the exact value of their coordinates (P_i, Q_i) can be considered random

[2]Again, we only consider point-to-point nets.

variables; $\mathcal{P}_N$ is a stochastic process. The joint distribution of N and $\mathcal{P}_N$ follows from the choice of a circuit out of the pool of all "meaningful" circuits and an optimal (possibly randomized) placement into the physical architecture.

Once the list $\mathcal{P}_N$ is known, both the wire lengths and the hierarchical level in Donath's partitioning model are fixed: they are functions of $\mathcal{P}_N$ through the length distribution of the architecture. We can thus write the length of a connection (P_i, Q_i) as $L(P_i, Q_i) \triangleq L_i$. The hierarchical level $K(P_i, Q_i) \triangleq K_i$ also follows from the actual places of P_i and Q_i in the Manhattan grid.

We assume that the precise order of the elements of $\mathcal{P}_N$ is not important and we limit our scope to circuits with a preset number of connections N. On the basis of this assumption, we can assume that the distribution of the first connection (P_1, Q_1) characterizes the other interconnections (this does, however, not imply statistical independence between pairs). Finally, we implicitly assume that the process $\mathcal{P}_N = ((P_1, Q_1), \ldots, (P_N, Q_N))$ possesses certain ergodic properties so that, for instance, the distribution of $L(P_1, Q_1)$ can be estimated from the statistics of $(L(P_1, Q_1), L(P_2, Q_2), \ldots, L(P_N, Q_N))$ of a "typical" circuit, valid for the entire population. For N large enough, the expected values of the observed statistics for the interconnection length distributions are good estimates for the interconnection length distributions themselves.

The global normalized wire length distribution $\mathcal{E}_l$ of a circuit, placed in a Manhattan grid, can then be estimated by the probability distribution of L_1

$$\mathcal{E}_l = P\{L(P_1, Q_1) = l\} \tag{13}$$

and the global wire length distribution $\mathcal{D}_l$ by

$$\mathcal{D}_l = N\mathcal{E}_l = NP\{L(P_1, Q_1) = l\}. \tag{14}$$

The local normalized wire length distribution (denoted by $\mathcal{M}_{k,l}$) is the conditional distribution

$$\mathcal{M}_{k,l} = P\{L(P_1, Q_1) = l | K(P_1, Q_1) = k\} \tag{15}$$

and the local wire length distribution $\mathcal{L}_{k,l}$ at level k can be calculated by multiplying the normalized distribution by the expected value of the total number of interconnections at level k (denoted as N_k). This expected value is given by

$$E[N_k] = NE\left[\frac{N_k}{N}\right] = NP\{K_1 = k\}, \tag{16}$$

which results in

$$\begin{aligned} \mathcal{L}_{k,l} &= E[N_k]\mathcal{M}_{k,l} \\ &= NP\{L(P_1, Q_1) = l, K(P_1, Q_1) = k\} \end{aligned} \tag{17}$$

5.3. Structural Distribution and Occupancy Probability

Donath's method for wire length estimations [1] is based on the enumeration of all possible interconnections (pairs of points) in each adjacent combination and each diagonal combination and on all hierarchical levels. This way, one obtains a wire length distribution that only depends on the physical architecture the circuit will be placed in. We will call this distribution the *structural distribution* [26]. The distributions $\mathcal{S}_{k,a}$ and $\mathcal{S}_{k,d}$, calculated in Donath's method (Section 3), are the normalized structural distributions for a square Manhattan grid.

We can also assign to each pair of points the probability that an interconnection between the two points will be effectively laid out in an optimal placement of the circuit with preset Rent exponent. This is what we call the *occupancy probability*.

Let $\mathcal{A}$ be the set of all points in a square (finite) subregion of the Manhattan grid. The *structural distribution* $\mathcal{S}(l)$ is then determined by the enumeration of all pairs (p, q) in the Manhattan grid, a distance $L(p, q) = l$ apart. If we call this set of pairs $\mathcal{N}(l)$, then the structural distribution is given by the number of elements in that set

$$\mathcal{S}(l) = |\mathcal{N}(l)| \tag{18}$$

with

$$\mathcal{N}(l) = \{(p,q) \in \mathcal{A} \times \mathcal{A} : L(p,q) = l\}. \quad (19)$$

The *occupancy probability* of a pair of points (p, q) is the probability that the pair will effectively be connected by a wire in an optimal placement of the circuit in the physical architecture, and this probability is given by

$$P_{p,q} = P\{(P_1, Q_1) = (p,q)\}. \quad (20)$$

We can now write the global wire length distribution $\mathcal{D}_l$, normalized on the total number of interconnections N, as

$$\frac{\mathcal{D}_l}{N} = P\{L_1 = l\} = P\{(P_1, Q_1) \in \mathcal{N}(l)\} = \sum_{L(p,q)=l} P\{(P_1, Q_1) = (p,q)\}.$$

Since we only consider the wire length as criterion for an optimal placement, we can assume that $P\{(P_1, Q_1) = (p,q)\}$ only depends on the length $L(p,q)$ but not on the precise location of the points p and q. If we denote an arbitrary pair (p,q) with $L(p,q) = l$ as $(p,q)_l$, then follows

$$\frac{\mathcal{D}_l}{N} = P\{(P_1, Q_1) = (p,q)_l\} \sum_{L(p,q)=l} 1$$

The factor $P\{(P_1, Q_1) = (p,q)_l\}$ is the *occupancy probability* of the pair $(p,q)_l$. As it only depends on the length, we denote it as $f(l)$. The second factor on the RHS of the equation is the number of pairs with length l, available in the physical architecture. This factor thus equals the structural distribution $\mathcal{S}(l)$. Therefore we can write

$$\mathcal{E}_l = \frac{\mathcal{D}_l}{N} = f(l)\,S(l). \quad (21)$$

By changing the distribution function of the interconnection points we actually change the occupancy probability $f(l)$ for pairs of points, *i.e.*, the probability that a pair of points in the Manhattan grid would be connected in a real placement procedure. We know that an optimal placement prefers shorter interconnections over longer ones. It thus seems acceptable to assume that most point pairs at the shortest distance will be *occupied* and less at longer distances. Intuitively, we expect the occupancy probability to be a monotonically decreasing function of the wire length. On the other hand, we should also consider the fact that the interconnection complexity of the circuit restricts the possible choices so that not all interconnections can have the shortest length. It is not possible to place interconnected logic blocks close to each other if other blocks have already taken those positions. These restrictions increase for circuits of higher complexity. The occupancy probability therefore should depend on the Rent exponent in such a way that it decreases less (more) rapidly when the Rent exponent is larger (smaller). In the next section, we will suggest a possible expression for the occupancy probability.

5.4. Global Occupancy Probability

In [10] and [14], simple theoretical considerations are used to indicate that the normalized distribution $\mathcal{E}_l$ of interconnection lengths for a good two-dimensional placement in a square Manhattan grid should be of the form

$$\begin{aligned} \mathcal{E}_l &\approx C\, l^{2r-3} \quad (1 \le l \le l_{\max}) \\ &\approx 0 \quad (1 > l_{\max}). \end{aligned} \quad (22)$$

In this equation, C is a normalisation constant and $l_{\max}$ is a constant related to the size of the square grid. In [3], Stroobandt *et al.*, showed that the trend of $\mathcal{E}_l$ (Eq. (22)) mainly depends on the number of interconnections N_k (given by Eq. (3)) at each hierarchical level and not on the way these interconnections are distributed locally (*i.e.*, per hierarchical level).

Using Eqs. (21) and (22), we can derive an approximated equation for the occupancy probability. Note that the approximation must be most accurate for small values of l since these occur most frequently and dominate the distribution. The structural distribution $S(l)$ can be found by

the enumeration of all possible point pairs of length l and is given by [4]

$$\mathcal{S}(l)=\begin{cases}\lambda^2 & (l=0)\\ \frac{2}{3}l(6\lambda^2-6l\lambda+l^2-1) & (0<l\leq\lambda)\\ \frac{2}{3}(2\lambda-l-1)(2\lambda-l)(2\lambda-l+1) & (\lambda<l\leq 2\lambda)\\ 0 & \text{otherwise}\end{cases} \tag{23}$$

It can be seen that the structural distribution increases linearly with l for small values of l. This can also be verified from Figure 9. We thus approximate the structural distribution by a distribution proportional to l. Therefore, the occupancy probability can be approximated by

$$f(l)=\frac{\mathcal{D}_l}{N\mathcal{S}(l)}\approx C\frac{l^{2r-3}}{l}=Cl^{2r-4} \tag{24}$$

with C a normalization constant. This occupancy probability obeys the requirement of a monotonically decreasing function of the wire length. It also takes into account the restrictions imposed by Rent's rule: the occupancy probability decreases less rapidly for higher values of r. Indeed, finding the placement of a complex circuit is a lot more difficult than finding the placement for a circuit that is less complex. The placement results in longer wires in the first case than in the second.

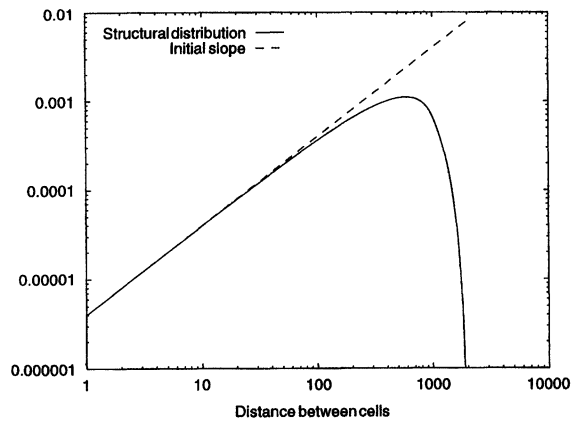

FIGURE 9 The normalized structural distribution of a Manhattan grid of 1000 × 1000 cells in a log–log plot.

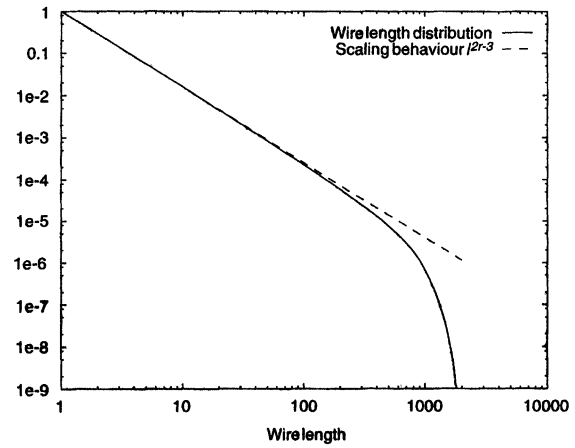

FIGURE 10 The global wire length distribution as a result of weighing the structural distribution by the occupancy probability for a Manhattan grid of 1000 × 1000 cells.

The approximation of the structural distribution (proportional to l) introduces a huge overestimation of the number of wires with length $l > \lambda/2$ (with λ the side of the Manhattan grid). The result of this overestimation is an underestimation of the occupancy probability for these wire lengths. Yet, we should note that

1. the number of wires with such lengths is negligible compared to the total number of wires;
2. the global wire length distribution only follows l^{2r-3} until a certain value l, smaller than the maximum distance in the grid; for greater lengths, the distribution decreases much more rapidly (see Eq. (22)).

Figure 10 shows that, conversely, the global distribution, found as the product of the (approximated) occupancy probability with the structural distribution, follows the behaviour observed by Donath (Eq. (22)), even for large values of l.

5.5. Local Occupancy Probability

The local wire length distribution on each hierarchical level can also be expressed as the product of the structural distribution at that level and an

occupancy probability. We can write the local wire length distribution $\mathcal{L}_{k,l}$ (normalized on N) as

$$\frac{\mathcal{L}_{k,l}}{N} = P\{L(P_1,Q_1)=l, K(P_1,Q_1)=k\} = \sum_{\substack{L(p,q)=l \\ K(p,q)=k}} P\{(P_1,Q_1)=(p,q)\}. \tag{25}$$

Also within one level, the wire length remains the only criterion for an optimal placement, so we can still assume $P\{(P_1,Q_1)=(p,q)\}$ to only depend on the length $L(p,q)$, and not on the precise location of p and q. We now denote an arbitrary pair (p,q) with length $L(p,q)=l$ at level $K(p,q)=k$ as $(p,q)_{l,k}$ and we denote the set of all pairs at level k that have length l as $\mathcal{N}_k(l)$. This then leads to

$$\frac{\mathcal{L}_{k,l}}{N} = P\{(P_1,Q_1)=(p,q)_{l,k}\}|\mathcal{N}_k(l)| = f(l)\mathcal{S}_k(l). \tag{26}$$

The factor $P\{(P_1,Q_1)=(p,q)_{l,k}\}$ is the occupancy probability of a pair $(p,q)_{l,k}$. Since we assumed that it only depends on the length of the interconnection, it is also given by $f(l)$. The second factor is the number of pairs (connections) at level k with length l and thus equals the local structural distribution $\mathcal{S}_k(l)$.

Donath implicitly assumes a uniform occupancy probability (all pairs have equal probability of being 'occupied'): $P\{(P_1,Q_1)=(p,q)_{l,k}\}$ is independent of p and q (and thereby also independent of the length and the level). For the local normalized distribution $\mathcal{M}^D_{k,l}$ this means, according to Donath,

$$\begin{aligned}\mathcal{M}^D_{k,l} &= P\{L(P_1,Q_1)=l|K(P_1,Q_1)=k\} \\ &= \frac{P\{L_1=l,K_1=k\}}{P\{K_1=k\}} \\ &= \frac{\sum_{\substack{L(p,q)=l \\ K(p,q)=k}} P\{(P_1,Q_1)=(p,q)\}}{\sum_{K(p,q)=k} P\{(P_1,Q_1)=(p,q)\}} \\ &= \frac{P\{(P_1,Q_1)=(p,q)\}|\mathcal{N}_k(l)|}{P\{(P_1,Q_1)=(p,q)\}\sum_l |\mathcal{N}_k(l)|} \\ &= \frac{\mathcal{S}_k(l)}{\sum_l \mathcal{S}_k(l)}.\end{aligned} \tag{27}$$

The normalized local wire length distribution in Donath's method thus equals (as we already know from Section 3) the normalized structural distribution.

We already observed Donath's model not to be a good model for an optimal placement within one hierarchical level. Therefore we introduce, at each hierarchical level, our non-uniform occupancy probability $f(l) = C l^{2r-4}$ for each separate pair of points $(p,q)_{l,k}$. In the next section, we calculate the average wire length by making use of this occupancy probability $f(l)$.

6. NEW AVERAGE WIRE LENGTH

We assume that all local occupancy probabilities are given by $f(l) = C l^{2r-4}$ (Eq. (24)). That way, we introduce information on the optimal placement of the entire circuit in each hierarchical level.

The local distribution at hierarchical level k is to be found by weighing the structural distribution $S_{k,C}$ ($C \in \{a,d\}$ Eqs. (4) and (5)) with the occupancy probability $f(l) = C l^{2r-4}$ (Eq. (24)). The expected value for the average length in a certain combination at a hierarchical level k then equals (with $C \in \{a,d\}$)

$$l_{k,C} = \frac{\sum_{l=0}^{4\lambda} l S_{k,C}(l) f(l)}{\sum_{l=0}^{4\lambda} S_{k,C}(l) f(l)} \tag{28}$$

$$= \frac{\sum_{l=0}^{4\lambda} S_{k,C}(l) l^{2r-3}}{\sum_{l=0}^{4\lambda} S_{k,C}(l) l^{2r-4}}. \tag{29}$$

The average interconnection length at hierarchical level k is then given by Eq. (9):

$$l_k = \frac{4 l_{k,a} + 2 l_{k,d}}{6}.$$

The sums in Eq. (29) can not be computed analytically without knowing the value for $\lambda = 2^k$. Yet, if we want to compare our results with those of Donath, both numerically and theoretically, an analytical form of the average interconnection

length is needed. A way around this problem is to approximate the discrete distributions by continuous ones. One can easily verify that the continuous form of the Eqs. (4) and (5) is given by

$$S^c_{k,a}(l) = \begin{cases} \frac{-l^3+3\lambda l^2}{3\lambda^4} & (0 \le l \le \lambda) \\ \frac{2l^3-12\lambda l^2+21\lambda^2 l-9\lambda^3}{3\lambda^4} & (\lambda \le l \le 2\lambda) \\ \frac{-l^3+9\lambda l^2-27\lambda^2 l+27\lambda^3}{3\lambda^4} & (2\lambda \le l \le 3\lambda) \\ 0 & \text{otherwise,} \end{cases} \tag{30}$$

and

$$S^c_{k,d}(l) = \begin{cases} \frac{l^3}{6\lambda^4} & (0 \le l \le \lambda) \\ \frac{-3l^3+12\lambda l^2-12\lambda^2 l+4\lambda^3}{6\lambda^4} & (\lambda \le l \le 2\lambda) \\ \frac{3l^3-24\lambda l^2+60\lambda^2 l-44\lambda^3}{6\lambda^4} & (2\lambda \le l \le 3\lambda) \\ \frac{-l^3+12\lambda l^2-48\lambda^2 l+64\lambda^3}{6\lambda^4} & (3\lambda \le l \le 4\lambda) \\ 0 & \text{otherwise.} \end{cases} \tag{31}$$

A substitution of the sums in Eq. (29) by integrals, for a Manhattan grid with an infinite number of points in each dimension and size $\lambda \times \lambda$ for each submodule at hierarchical level k, yields

$$l_{k,C} = \frac{\int_0^{4\lambda} S^c_{k,C}(l) l^{2r-3} dl}{\int_0^{4\lambda} S^c_{k,C}(l) l^{2r-4} dl}. \tag{32}$$

For $r > 0.5$, this results in

$$l_{k,a} = \lambda R_a(r) \tag{33}$$

$$l_{k,d} = \lambda R_d(r), \tag{34}$$

with

$$R_a(r) = \frac{(2r-3)}{(2r+1)} \frac{3^{2r+1} - (2r+7)2^{2r} + (4r+5)}{3^{2r} - (r+3)2^{2r} + (4r+3)}, \tag{35}$$

$$R_d(r) = \frac{(2r-3)}{(2r+1)} \frac{4^{2r} - 3^{2r+1} + 32^{2r} - 1}{4^{2r-1} - 3^{2r} + 32^{2r-1} - 1}, \tag{36}$$

and

$$l_k = \lambda R(r), \tag{37}$$

with

$$R(r) = \frac{4R_a(r) + 2R_d(r)}{6}. \tag{38}$$

The sum over all hierarchical levels (Eq. (2)) then yields

$$L = R(r) \frac{H(K,r,1)}{H(K,r,2)}, \tag{39}$$

with

$$H(K,r,x) = \frac{2^{K(2r-x)} - 1}{2^{2r-x} - 1}.$$

The integral in the denominator of Eq. (32) does not converge at the lower bound for $r < 0.5$. This means that it is fully dominated by the values around $l = 0$, an area where the value should be zero in the discrete case (sums). The error introduced by the continuous approximation then becomes extremely high but the divergence of the integral shows that the average length no longer scales with λ, but remains constant. We will not elaborate on the details here. Since the convergence still exists for the diagonal combination, the average length will be fully dominated by it and it follows that

$$L = \frac{R_d(r)}{3} \frac{H(K,r,1)}{H(K,r,2)} \quad (r < 1/2). \tag{40}$$

7. DISCUSSION AND RESULTS

7.1. Scaling Behaviour

The scaling behaviour is the same as in Donath's technique (compare Eq. (39) with Eq. (10)). This results from the use of the same hierarchical

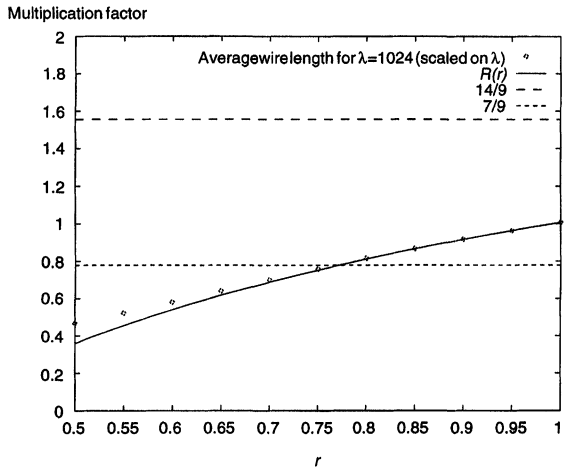

FIGURE 11 $R(r)$ (Eq. (38)) against Donath's factor 14/9 for $0.5 \leq r \leq 1$. Also a numerical result based on Eq. (29) is shown.

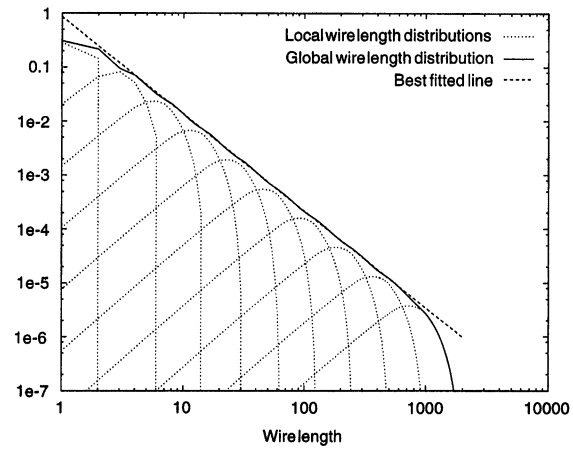

FIGURE 12 The normalized global wire length distribution, composed of local wire length distributions, calculated with Donath's method.

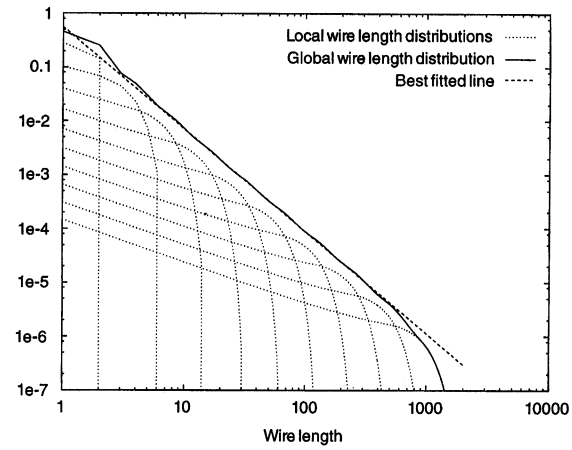

FIGURE 13 The normalized global wire length distribution, composed of local wire length distributions, calculated with our method.

placement model with the number of interconnections at each hierarchical level estimated by Rent's rule.

The main difference between our estimates and Donath's estimates lies in the multiplicative constant ($R(r)$ *versus* 14/9) (Fig. 11). The factor $R(r)$ increases with increasing r, corresponding to the fact that more complex circuits (with a higher r) tend to have longer interconnections. The value of $R(r)$ is approximately 7/9, which is half the value found by Donath, for rather complex circuits with $r < 0.8$. This corresponds to our knowledge that Donath's estimates differ from experimental values in a factor $\delta \approx 2$. In all cases ($0 < r < 1$), our estimation of the average interconnection length is more accurate than the one found by Donath.

7.2. Comparison of Our Wire Length Distributions with Donath's

Figures 12 and 13 show the global distribution (filled line) as the sum of the various local distributions (point lines), for Donath's method and our method, respectively. They both follow the expected trend l^{2r-3} (dashed line) but our method follows this trend better for the small wire lengths (note that, due to the logarithmic scale, our overestimation of the number of nets with length 2 only seems to be much larger than the underestimation of the number of nets of unit length, but that this is not the case in reality; the order of magnitude is comparable). The improvement in the model for the optimal placement has resulted in boosting the local distributions for low values of l. The fact that, even at higher levels, short interconnections are still abundant indeed coincides with the intuitive notion of an optimal placement.

The difference between our method and Donath's is also shown on Figure 14. Our approximation obviously is much better, especially at unit length. It is only slightly worse than Donath's for lengths 2. The fact that there still exists a deviation in our method (at very small lengths) is the result of the fact that we still treat adjacent and diagonal combinations in the same way, although their average lengths are not the same, especially not at the lowest level (1 compared to 2). A differentiation in the number of interconnections assigned to adjacent or diagonal combinations would require an extension of Rent's rule to a second order equation. This has not been accomplished yet.

Our wire length estimation uses a better model for an optimal placement than Donath's model. This can also be seen from the following thought experiment (Fig. 15): cut the Manhattan grid in two parts by a vertical cut. Next, count the number of interconnections that traverse the cut, assuming that a circuit with a given Rent exponent is placed according to Donath's placement model. Let the cut move from left to right and, for each cut position, count the number of crossing wires. In Figure 15, the interconnections numbered 1 and 2 are counted when the cut takes position 1, the interconnections 3 and 4 when the cut takes position 2. After we have done the same for a placement according to our model, based on the occupancy probability, we observe the results of our count in Figure 16. The number of counted wires (shown in Fig. 16 in % of the total number of wires, as a function of the cut position) is always smaller in our case than with Donath's model. Also the variation of this number over all cut positions is smaller. This implies that our method models an optimal placement better as an optimal placement results in shorter wires and hence a lower chance of a wire being cut.

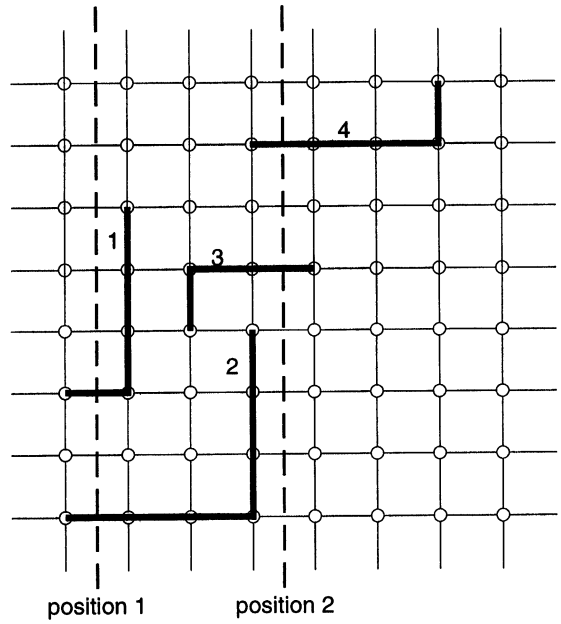

FIGURE 15 Thought experiment: count the number of interconnections crossing a cut in the Manhattan grid.

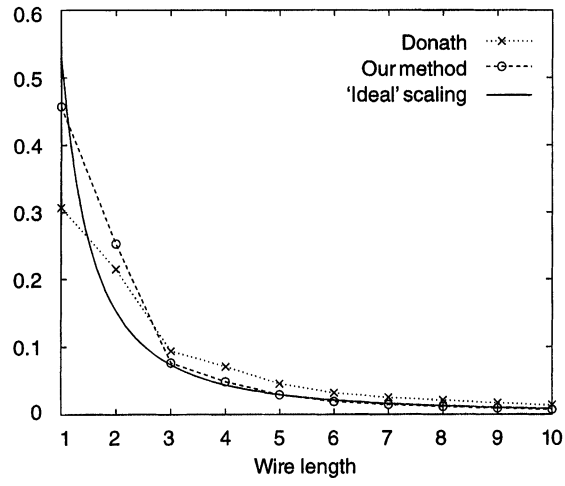

FIGURE 14 The global wire length distributions according to Donath's method and our method, compared to the 'ideal' distribution (normalized on the range [1...1024]). Only the first 10 values are shown.

7.3. Experimental Verification

In order to verify our model for the placement of a circuit in a Manhattan grid, we performed several experiments on benchmark circuits with our own placement program, based on simulated annealing [27]. The resulting wire length distribution for one

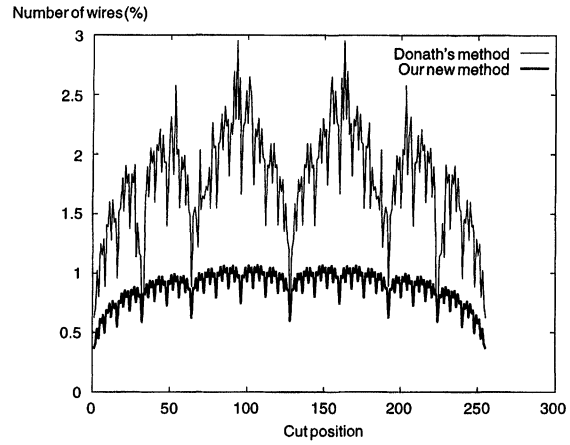

FIGURE 16 The number of interconnections (in % of the total number of interconnections in the circuit) for successive cuts and a circuit with Rent exponent $r = 0.6$ in a Manhattan grid of 256×256 cells. Comparison of Donath's placement model to our extension with a non-uniform occupancy probability.

of the benchmark circuits ('c1908') is shown in Figure 17. Also the theoretical estimates, based on Donath's technique (dashed line) and our own method (filled line), are shown in the figure. Our model, taking into account the occupancy probability, obviously matches the experimental results more closely, especially for wires of lengths 1 and 2 (which are the most important ones for the calculation of the average wire length).

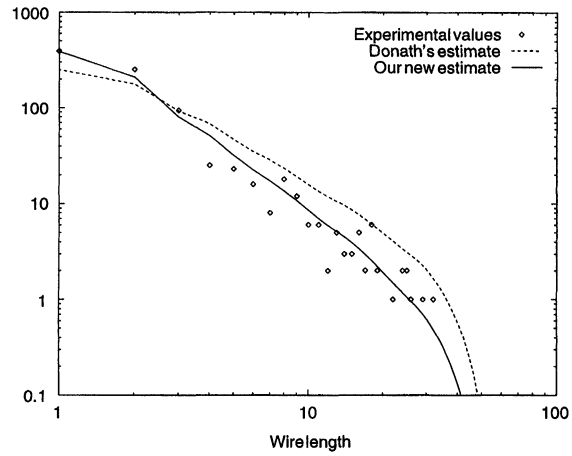

FIGURE 17 The wire length distribution after placement of the ISCAS85 benchmark circuit 'c1908 nr'.

In Tables I, II, and III, the results are shown for all benchmarks. Table I shows the results for the benchmark circuits used by Donath in [1]. In this table, our wire length estimates are much lower than Donath's and are related to the experimental values more closely than Donath's.

Tables II and III show the results of our own experiments with the ISCAS benchmark circuits. These results are also shown in Figures 18 and 19, as a function of the number of logic blocks and the Rent exponent, respectively. In these figures, we have connected the corresponding points for clarity. The rough appearance of the curves is due to the strong dependency of the average length on both the number of logic blocks and the Rent exponent. Only one of these dependencies is shown in the figures.

In Table II, we can again observe that our estimates are much lower than Donath's and that they generally follow the experimental values more closely. In some cases, we appear to underestimate the wire length. This is partly due to the fact that the occupancy probability underestimates the number of long wires at the higher levels. For circuits that are large enough, this has no real influence on the average wire length, because the number of long interconnections is relatively small. For smaller circuits this influence is no longer negligible and for those circuits we should actually change the approximation of the occupancy probability at the higher levels. Yet, it is clear, both from the tables and the figures, that the circuits for which we underestimate the average length, also lead to low estimates with Donath's technique. For these circuits, also Donath's estimates are much lower than we would expect, since we know that Donath overestimates average lengths by a factor of approximately 2 [1]. The experimental value thus appears too high. This could be a consequence of not too good a placement, or it could be the result of a bad estimate of the Rent exponent. The phenomenon is even stronger in Table III and in Figures 18 and 19. Our estimates are almost always too low and even Donath often underestimates the average length (which does not correspond to

TABLE I Average wire length for a placement of Donath's benchmark circuits [1]. Donath's estimates (L_D) and our estimates, based on the occupancy probability (L), compared to experimentally measured values (L_{exp}). G is the number of logic blocks in the circuit, N the number of nets and r the Rent exponent (data copied from [1])

No.	G	N	r	L_{exp}	L_D	L	(L_D/L_{exp})	(L/L_{exp})
1	528	1007	0.59	2.15	4.02	2.44	1.87	1.13
2	576	1111	0.75	2.85	5.26	3.25	1.85	1.14
3	671	1670	0.57	2.63	4.07	2.43	1.55	0.93
4	1239	2687	0.47	2.14	3.76	2.21	1.76	1.03
5	2148	7302	0.75	3.50	7.37	4.29	2.11	1.23

TABLE II Average wire length for a placement of the ISCAS85 benchmark circuits. Donath's estimates (L_D) and our estimates, based on the occupancy probability (L), compared to experimentally measured values (L_{exp}). G is the number of logic blocks in the circuit and r the Rent exponent

Name	G	r	L_{exp}	L_D	L	(L_D/L_{exp})	(L/L_{exp})
c432	160	0.62	2.925	3.304	2.157	1.129	0.737
c499	202	0.62	3.177	3.468	2.237	1.091	0.704
c880	383	0.62	2.764	3.949	2.433	1.428	0.880
c1355	546	0.73	2.804	5.030	3.108	1.793	1.108
c1908	880	0.72	2.865	5.558	3.356	1.939	1.171
c2670	1193	0.73	2.817	6.098	3.643	2.164	1.293
c432nr	157	0.62	2.890	3.291	2.155	1.138	0.745
c499nr	202	0.65	3.157	3.586	2.318	1.135	0.734
c1355nr	546	0.74	2.786	5.110	3.166	1.834	1.136
c1908nr	878	0.71	2.893	5.455	3.288	1.885	1.136
c2670nr	961	0.79	2.482	6.463	3.994	2.603	1.608

TABLE III Average wire length for a placement of the ISCAS89 benchmark circuits. Donath's estimates (L_D) and our estimates, based on the occupancy probability (L), compared to experimentally measured values (L_{exp}). The experimental value L_{10} only takes the first 10 values into account. G is the number of logic blocks in the circuit and r the Rent exponent

Name	G	r	L_{exp}	L_D	L	L_{10}	(L_D/L_{exp})	(L/L_{exp})	(L/L_{10})
s27	13	0.26	1.500	1.710	1.403	1.500	1.140	0.935	0.935
s208.1	112	0.35	1.946	2.444	1.620	1.855	1.256	0.832	0.873
s298	133	0.37	2.598	2.538	1.692	1.694	0.976	0.651	0.998
s386	165	0.51	3.713	2.976	1.937	1.928	0.801	0.521	1.004
s344	175	0.40	2.045	2.699	1.768	1.710	1.319	0.864	1.033
s349	176	0.40	2.045	2.701	1.768	1.796	1.320	0.864	0.984
s382	179	0.35	2.520	2.584	1.712	1.837	1.025	0.679	0.931
s444	202	0.29	2.505	2.478	1.660	1.957	0.989	0.662	0.848
s526	214	0.47	3.187	2.976	1.928	2.174	0.933	0.604	0.886
s526n	215	0.43	3.181	2.856	1.859	2.046	0.897	0.584	0.908
s510	217	0.65	4.036	3.643	2.347	2.505	0.902	0.581	0.936
s420.1	234	0.37	2.089	2.714	1.795	1.843	1.299	0.858	0.973
s832	292	0.51	5.337	3.264	2.065	1.785	0.611	0.386	1.156
s820	294	0.54	5.229	3.389	2.138	1.830	0.648	0.408	1.168
s641	398	0.69	1.882	4.393	2.731	1.608	2.333	1.451	1.698
s713	412	0.71	1.940	4.557	2.845	1.636	2.348	1.465	1.738
s953	424	0.68	4.371	4.393	2.717	2.616	1.004	0.621	1.038
s838.1	478	0.41	2.182	3.078	1.888	1.966	1.410	0.865	0.960
s1238	526	0.66	4.885	4.471	2.722	2.459	0.915	0.557	1.106
s1196	547	0.64	4.330	4.370	2.647	2.218	1.009	0.611	1.193
s1494	653	0.58	5.806	4.112	2.452	1.919	0.708	0.422	1.277
s1488	659	0.59	5.703	4.185	2.500	1.786	0.733	0.438	1.399
s1423	731	0.50	2.552	3.615	2.202	1.882	1.416	0.862	1.170

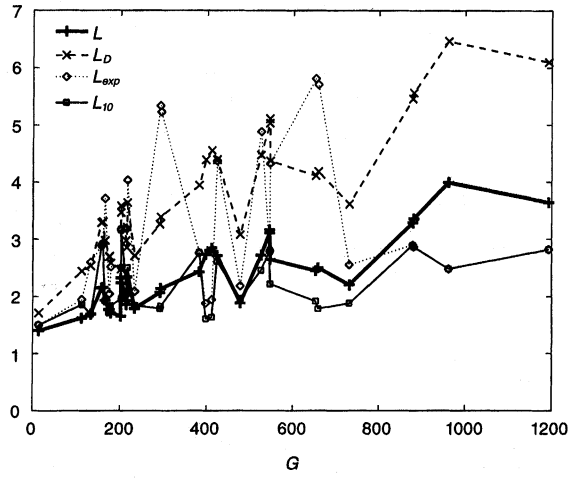

FIGURE 18 Our estimates (L) and Donath's (L_D), compared to the experimental values (L_{exp} and L_{10}): average wire length of the ISCAS benchmark circuits as a function of the number of logic blocks G.

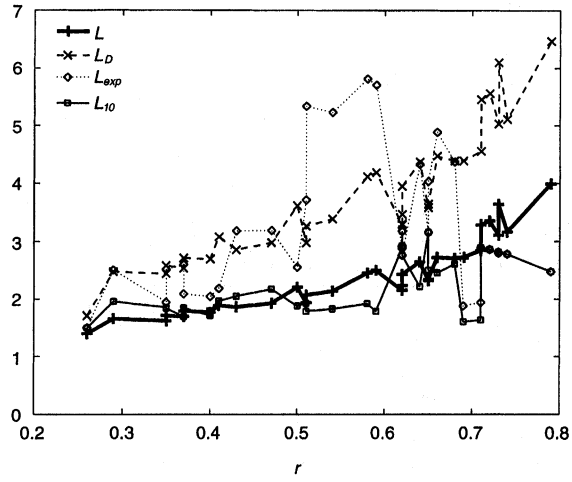

FIGURE 19 Our estimates (L) and Donath's (L_D), compared to the experimental values (L_{exp} and L_{10}): average wire length of the ISCAS benchmark circuits as a function of the Rent exponent r.

Donath's own results [1]). The cause of this more likely is the fact that the ISCAS89 benchmarks contain a lot of nets with very high net degree. Multi-terminal nets are not included in the model yet. In the experimental placements, however, nets with high net degrees are very long. In normal circuits, the number of nets with high net degree is too small to cause a significant deviation in the average length [4]. This is not the case for the ISCAS89 benchmark circuits. Figure 20 shows, for instance, the wire length distribution after placement of the ISCAS89 circuit 's832' (more figures to show this is also true for the other benchmarks, can be found in [28]). The figure clearly shows an excess of long wires compared to the general trend. These wires are all multi-terminal nets with high net degrees. Since the total number of wires is not very large, these nets do have a significant influence on the average wire length. If we do not include these 'exceptional' nets, we find a much better correspondence between the theoretical and the experimental values (for convenience, only the first 10 values of the distribution are taken into account). These experimental values are shown in the column L_{10} of Table III. A comparison between those values and our theoretical estimate L gives a relative difference of less than 20% for 19 circuits out of 24. Figures 18 and 19 show that the experimentally obtained average wire length values, based only on the first 10 values of the distribution, generally are much lower than the original experimental values. Moreover, they are closely related to our theoretical estimates, especially when we also compare both to Donath's estimates. Although omitting the long wires obviously influences the

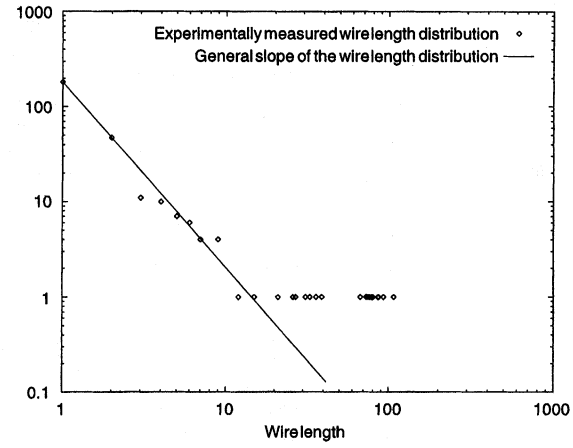

FIGURE 20 Illustration of the existence of exceptionally large interconnections in the placed ISCAS89 benchmark circuits.

whole experiment and the results should be discussed with great care, we can conclude that our model for wire length estimates resembles experimentally measured lengths quite good, but that our model does not take into account specific properties of nets with high net degree. This has been the subject of our latest research work [16, 17].

8. CONCLUSION

In this paper, we have presented a modification of Donath's technique for *a priori* wire length estimation, introducing the occupancy probability as a better model for an optimal placement. This way, we have obtained a new average interconnection length estimation corresponding more closely to the experimental values than the upper bound found by Donath. Our new accurate *a priori* interconnection length estimation technique can have a large impact in future CAD tools for floorplanning and placement, in particular in view of the increasing importance of wires in digital circuits.

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