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A Fast and Accurate Method of Power Estimation for Logic Level Networks*

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A method for estimating the power consumption of multilevel combinational networks is introduced. The proposed method has as inputs the signal probabilities, the data correlations of the primary inputs and the structure of the circuit, and consists of two major steps: (i) the calculation of the switching activity on an individual gate and (ii) the calculation of the switching activity of any node of the network. The foregoing step includes the derivation of novel formulas for calculating the switching activity of basic gates. The latter step includes the development of an algorithm, which propagates the signal probabilities through the network and calculates the switching activity of any logic node. The proposed method provides accurate switching activity values performing their calculation in reduced time interval. The experimental results prove that the proposed method achieves significant reduction up to 50% in terms of multiplications compared to method of [6].

Keywords: Low power design; Switching activity estimation; Power dissipation model; Markov chains; Temporal and spatial correlation; CMOS combinational circuits

1. INTRODUCTION

The requirement for long battery life at the wide spread portable communication systems forces the designers to take into consideration except of the two traditional parameters, area and speed, and a third one, the power consumption [1, 2].

Recently, many researchers have suggested a number of methods for estimating the power consumption in digital CMOS circuits [3–7]. In particular, using symbolic simulation and Ordered Binary Decision Diagrams (OBBDs) [10, 11], and considering spurious transitions, temporal correlation, and structural correlation a power estimator was introduced by Devadas *et al.* [5]. The main drawback of the method is its high computational complexity. Also, the spatial correlations of the input signals are not included. Schneider *et al.* [7]

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presented a method using Markov chain theory, Reduced OBBDs, first-order temporal correlation, and structural correlation. However, it has been assumed that the primary inputs are independent and spatially-uncorrelated. Marculescu *et al.* [6] based on [9], on OBDDs and on Markov chain theory, suggested an accurate model for power estimation, using probabilistic methods. Introducing the concept of the transition correlation coefficient (TCC), the spatiotemporal correlation is taken into account. Two methods, namely the global and incremental method, have been proposed. Comparing these methods, it is concluded that the latter method is less accurate than the first one. The common drawback is the large computational complexity.

In this paper a novel method for estimating the switching activity of a multilevel combinational circuit, is introduced. The proposed method belongs to the class of probabilistic approaches [12] and provides highly accurate switching activity values in smaller time interval than the existing methods. The method has as inputs the static probability, the transition probability, and the data correlations of the primary inputs, as well as, the after mapping structure of a logic network. The network consists of zero-delay basic logic gates, *e.g.*, AND, OR, and NOT. The outcome of the method is the switching activity value of any node of the logic network.

The proposed method is accurate and fast. More specifically, the accuracy arises from the fact that spatial, temporal, and structural correlations of the signals, at all logic levels are taken into account. The reduced time cost results from the reduced computational complexity in terms of multiplications. The proposed method comprises two steps: (i) switching activity estimation of a single basic gate and (ii) switching activity estimation of any node of the considered logic network. In particular, the switching activity of a single basic gate can be calculated by a set of newly-developed formulas. Detailed formal description of the derivation process of these formulas is given. The second step includes the development of a new procedure, which determines the propagation of the signal probabilities through the basic gates and the wires of the logic network, calculates the appropriate TCCs, and eventually, estimates the switching activity of a logic node. The computational complexity of the switching activity of a basic gate and logic network in terms of multiplications, have been computed by a series of formally proven lemmas. Moreover, the accuracy and complexity of the proposed method are compared with the ones of [6], using a number of lemmas. It is concluded that both methods have identical accuracy, while the proposed one has less complexity than [6]. The experimental results for a set of ISCAS circuits indicate remarkably reduced computational complexity.

The rest of the paper is organised as follows. Section 2, the proposed method for power estimation is presented in detail manner. The experimental results are shown in Section 3. Finally, the conclusions are given in Section 4.

2. THE PROPOSED METHOD

The estimation of the power consumption of a logic circuit can be stated as follows:

Assuming a without loops combinational logic network of n-input zero-delayed basic gates (i.e., AND, OR, NOT, etc.) and given the statistical properties of the primary inputs (transition probabilities and paiwise TCCs) estimate its switching activity and eventually, the power consumption.

The total number of switches of a circuit node is the sum of the functional transitions and the spurious transitions (glitches). The functional transitions come from the structure of the circuit and the applied input vectors, while the glitches arise mainly from the gate and wires delays.

In this paper only the functional transitions are considered since a zero delay model is assumed. Including the evaluation of the glitches the estimation becomes more accurate but the computational complexity is increased since additional parameters such as the circuit delay paths, the actual values of the capacitances of the nodes, the slope of the input pulses and the width of the input

pulses *etc.*, have to considered. However, in a synthesis environment, where a lot of power estimations are performed to characterize in terms of switching activity alternatives implementations of the circuit, a fast and an as possible as accurate estimation is required. Adopting a method which considers the contribution of glitches the evaluated power becomes more accurate but the computational complexity is increased prohibitively. Moreover, some of the parameters such as the delay of the circuit lines and the capacitance of the nodes are not available in a gate level description. Thus, a zero gate delay model is used adopting the introduced error since the contribution of the glitches is ignored.

2.1. Switching Activity Estimation of a Single Gate

The formula, which calculates the switching activity of the output of a gate in terms of its inputs, will be derived first. To compute the switching activity of an n-input gate, we must consider the Boolean behaviour of a gate, which is specified by its controlling value. The output of an n-input basic gate performs a transition, when one or more inputs perform identical transitions simultaneously in two successive clock cycles t and $t+T$, while the remaining inputs are non-controlling value. Firstly, the switching activity of the output of a 3-input AND gate will be studied in detail manner. Then, the study will be generalised for an n-input AND gate. It must be noted that the same analysis holds for all basic gates.

2.1.1. Computation of the Switching Activity of a 3-input AND Gate

A 3-input AND gate, $x_0, x_1, \ldots, x_{n-1}$, performs a $TC_{11,01}^{x_9,x_{10}}$ $(1 \rightarrow 0)$ transition in three cases:

(i) one input performs a $0 \rightarrow 1$ $(1 \rightarrow 0)$ transition, while the remaining inputs are in high state,
(ii) two inputs perform a $0 \rightarrow 1$ $(1 \rightarrow 0)$ transition simultaneously, while the remaining input is in high state, and
(iii) all inputs perform a $0 \rightarrow 1$ $(1 \rightarrow 0)$ transition simultaneously.

Consequently, the transition probability, $p(y_{0\rightarrow 1})$, can be approximated by:

$$\left.\begin{aligned} p(y_{0\rightarrow 1}) = {} & p_{0\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} + p_{1\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} + \\ & + p_{1\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} + p_{0\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} + \\ & + p_{1\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} + p_{0\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} + \\ & + p_{0\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} \end{aligned}\right\} \quad (1)$$

The transition probability, $p(x_{i\rightarrow j})$ $i, j \in \{0,1\}$, corresponds to probability a signal x to perform a transition from state i to state j in two successive time clocks. Thus, the switching activity is evaluated considering the first order temporal correlation. The higher order temporal correlation should be considered in a similar way but the computational complexity while the accuracy is not improved significantly.

Furthermore, Eq. (1) is an approximation of the switching activity, since the data correlations of the input signals are not taken into account. Considering that the data correlations can be described by the appropriate TCCs, $TC_{a,b,c}^{x_0,x_1,x_2}$, where $a, b, c \in \{00, 01, 10, 11\}$, the appropriate TCCs must appear in each product of Eq. (1). Employing the formula $TC_{a,b,c}^{x_0,x_1,x_2} = TC_{a,b}^{x_0,x_1} TC_{b,c}^{x_1,x_2} TC_{a,c}^{x_0,x_2}$ [6, 9], the first term of Eq. (1) can be expressed as:

$$\begin{aligned} & p_{0\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} TC_{011,111}^{x_0,x_1,x_2} \\ & \quad = p_{0\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} TC_{01,11}^{x_0,x_1} TC_{01,11}^{x_0,x_2} TC_{11,11}^{x_1,x_2} \end{aligned} \quad (2)$$

Therefore,

$$\left.\begin{aligned} p(y_{0\rightarrow 1}) = {} & p_{0\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} TC_{01,11}^{x_0,x_1} TC_{01,11}^{x_0,x_2} TC_{11,11}^{x_1,x_2} + \\ & + p_{1\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} TC_{10,11}^{x_0,x_1} TC_{11,11}^{x_0,x_2} TC_{01,11}^{x_1,x_2} + \\ & + p_{1\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} TC_{11,11}^{x_0,x_1} TC_{10,11}^{x_0,x_2} TC_{10,11}^{x_1,x_2} + \\ & + p_{0\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{1\rightarrow 1}^{x_2} TC_{00,11}^{x_0,x_1} TC_{01,11}^{x_0,x_2} TC_{01,11}^{x_1,x_2} + \\ & + p_{0\rightarrow 1}^{x_0} p_{1\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} TC_{01,11}^{x_0,x_1} TC_{00,11}^{x_0,x_2} TC_{10,11}^{x_1,x_2} + \\ & + p_{1\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} TC_{10,11}^{x_0,x_1} TC_{10,11}^{x_0,x_2} TC_{00,11}^{x_1,x_2} + \\ & + p_{0\rightarrow 1}^{x_0} p_{0\rightarrow 1}^{x_1} p_{0\rightarrow 1}^{x_2} TC_{00,11}^{x_0,x_1} TC_{00,11}^{x_0,x_2} TC_{00,11}^{x_1,x_2} \end{aligned}\right\} \quad (3)$$

The $1 \rightarrow 0$ transition can be studied in similar way. Eventually, the switching activity of an 3-input

AND gate can be calculated by:

$$E(y) = p(y_{0\to1}) + p(y_{1\to0}) \tag{4}$$

2.1.2. *Computation of the Switching Activity of an n-input AND Gate*

Based on the aforementioned analysis, the transition activity of an n-input AND gate, $y=f(x_0, x_1, \ldots, x_{n-1}) = x_0 x_1 \ldots x_{n-1}$, can be expressed by:

$$\begin{aligned} E(y) &= p(y_{0\to1}) + p(y_{1\to0}) \\ &= \sum_{j=0}^{2^n-2} \left(\prod_{i=0}^{n-1} A_{0\to1} \prod_{k=0}^{n-2} \prod_{l=k+1}^{n-1} B_{0\to1} \right) \\ &\quad + \sum_{j=0}^{2^n-2} \left(\prod_{i=0}^{n-1} A_{1\to0} \prod_{k=0}^{n-2} \prod_{l=k+1}^{n-1} B_{1\to0} \right) \end{aligned} \tag{5}$$

where:

$$A_{0\to1} = b_i(j) p_{1\to1}^{x_i} + (1 - b_i(j)) p_{0\to1}^{x_i} \tag{6}$$

$$\begin{aligned} B_{0\to1} = \{ & b_k(j)\, b_l(j)\, TC_{11,11}^{x_k,x_l} + (1 - b_k(j))\, b_l(j) \\ & TC_{01,11}^{x_k,x_l} + b_k(j)\,(1 - b_l(j)) TC_{10,11}^{x_k,x_l} + \\ & + (1 - b_k(j))\,(1 - b_l(j))\, TC_{00,11}^{x_k,x_l} \} \end{aligned} \tag{7}$$

$$A_{1\to0} = b_i(j) p_{1\to1}^{x_i} + (1 - b_i(j)) p_{1\to0}^{x_i} \tag{8}$$

$$\begin{aligned} B_{1\to0} = \{ & b_k(j)\, b_l(j)\, TC_{11,11}^{x_k,x_l} + (1 - b_k(j))\, b_l(j) \\ & TC_{11,01}^{x_k,x_l} + b_k(j)\,(1 - b_l(j)) TC_{11,10}^{x_k,x_l} + \\ & + (1 - b_k(j))\,(1 - b_l(j))\, TC_{11,00}^{x_k,x_l} \} \end{aligned} \tag{9}$$

Let $C = \{c_0, c_1, \ldots, c_j, \ldots, c_m\}$ with $c_j = [(x_0, x_1, \ldots, x_n)^t, (x_0, x_1, \ldots, x_n)^{t+T}]$ be the set of all possible pairs of the input values of an n-input gate in two successive time steps t and $t+T$, such that the gate output value changes.

The term, $b_i(j)$ corresponds to the i-th input of the j-th pair and equals to 0 when the i-th input changes and 1 otherwise. Due to the fact, that all inputs have identical effect at the output of the gate and there are also K inputs which when they are changed identically they alter the output, the total number of the corresponding pairs is equal to $\sum_{k=1}^{n} \binom{n}{K} = 2^n - 1$. As the numbering starts from the 0, then $0 \le j \le 2^n - 2$. It is sufficient to analyse the structure, the features, and the properties of the first summation of Eq. (6), which describes a $0 \to 1$ transition, because the second one describes the complementary transition (*i.e.*, $1 \to 0$).

For each AND gate with $x_0, x_1, \ldots, x_{n-1}$ inputs, an n-bit word $[b_0(j), b_1(j), \ldots, b_{n-1}(j)]$, where $b_i(j) = \{0, 1\}$, is created. Each bit, $b_i(j)$, corresponds to the x_i input and the transition behaviour of x_i is expressed by the following "encoding" method:

$$A_{0\to1} = b_i(j) p_{1\to1}^{x_i} + (1 - b_i(j)) p_{0\to1}^{x_i} \tag{10}$$

i.e., when $b_i(j) = 0$ a $0 \to 1$ transition occurs with probability $p_{0\to1}^{x}$.

Moreover, in order to calculate the switching activity, the TCCs have to be taken into consideration. The contribution of the TCCs in the parametric form of (6) is expressed by the term $B_{0\to1}$. The correlation coefficients for a $0 \to 1$ transition for two signals x_k, x_l are computed using the previous described encoding method.

The new formulas, which calculates the switching activity of the n-input NAND, NOR, and OR gates are given in Appendix I.

2.1.3. *Complexity*

Equation (5) consists of two parts, the first of which corresponds to the transition $0 \to 1$, while the second one to $1 \to 0$. Since the two parts are identical, it is sufficient to study the transition $0 \to 1$, only. The structure of the first part of Eq. (5) is depicted in Figure 1, where the segment $A_{0\to1}$ expresses the contribution of the transition probabilities to the transition $0 \to 1$, while the segment $B_{0\to1}$ expresses the contribution of the TCCs.

$A_{0\to1}$ consists of n terms, while $B_{0\to1}$ of $\binom{n}{2}$ terms. For computation reasons, the segment $B_{0\to1}$ is split into two sub-parts, *i.e.*, $B_{0\to1_a}$ and $B_{0\to1_b}$, as it is shown in Figure 1. Specifically, the sub-part $B_{0\to1_a}$ corresponds to TCCs, $TC_{i_0 i_k j_1 j_k}^{x_0,x_k}$, $0 \le k < l \le n-1$, between the signal x_0 and the remaining

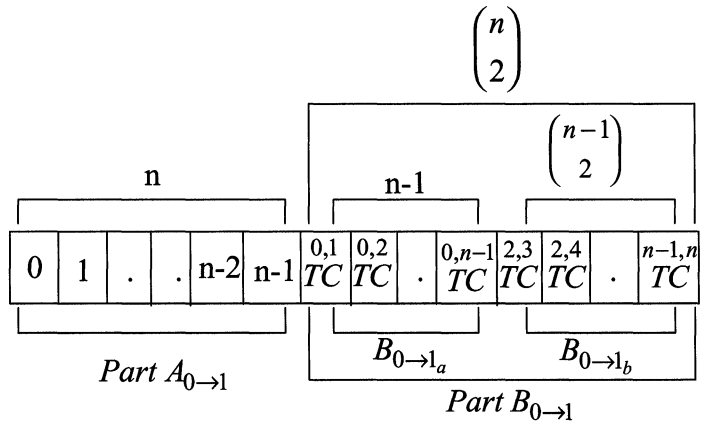

FIGURE 1 Structure of each term for of the transition activity of an n-input gate.

signals, while $B_{0\to 1_b}$ includes the remaining TCCs, $TC_{i_k i_l j_k j_l}^{x_k,x_l}$, $1 \le k \le l \le n-1$. The computational complexity of each part of Eq. (5) in terms of multiplications, can be calculated by the following lemmas.

LEMMA 1 *The computational complexity, $C_n(A_{0\to 1})$, of $A_{0\to 1}$ of an n-input AND gate in terms of multiplications equals*:

$$C_n(A_{0\to 1}) = 2^{n+1} - 5 \tag{11}$$

Proof The part $A_{0\to 1}$ can be calculated recursively as explained in the following. In the beginning the sub-part of $A_{0\to 1}$ which corresponds to $(n-2)$ and $(n-1)$ bits is calculated performing 2^2 multiplications and the result is stored 2^{n-2} times. Next, the sub-part that corresponds to $(n-3)$ to $(n-1)$ bits is calculated performing 2^3 multiplications and the result is stored 2^{n-3} times and so on until the calculation the whole part $A_{0\to 1}$. Consequently, the required number of multiplications for the calculation of $A_{0\to 1}$ equals: $2^2+2^3+\cdots+2^n-1=2^{n+1}-5$.

LEMMA 2 *The computational complexity, $C_n(B_{0\to 1})$, of $B_{0\to 1}$ of an n-input AND gate in terms of multiplications is*:

$$C_n(B_{0\to 1}) = 2^{n+2} + 2^{n+1} - 8(n+1) \quad \forall n \ge 3 \tag{12}$$

Proof The computational complexity of the segment $B_{0\to 1}$ can be computed as:

$$C_n(B_{0\to 1}) = C_n(B_{0\to 1_a}) + C_n(B_{0\to 1_b}) + C_n(Connect\,(B_{0\to 1_a}, B_{0\to 1_b})) \tag{13}$$

where $C_n(B_{0\to 1_a})$ and $C_n(B_{0\to 1_b})$ denote the complexities of the sub-parts $B_{0\to 1_a}$ and $B_{0\to 1_b}$, respectively. The last term corresponds to the required number of multiplications between $B_{0\to 1_a}$ and $B_{0\to 1_b}$. Then, the complexity of each term will be specified below:

(i) Using the approach of Lemma 2, the complexity $C_n(B_{0\to 1_a})$ is calculated. That is:

$$C_n(B_{0\to 1_a}) = 2^3 + 2^4 + \cdots + 2^n - 1 = 2^{n+1} - 9 \tag{14}$$

(ii) The complexity $C_n(B_{0\to 1_b})$ is the complexity of an $(n-1)$-input gate. That is:

$$C_n(B_{0\to 1_b}) = C_{n-1}(B_{0\to 1}) + 2 \tag{15}$$

(iii) To compute the whole segment $B_{0\to 1}$, the required multiplications are:

$$C_n(Connect\,(\mathrm{B}_{0\to 1_a}, \mathrm{B}_{0\to 1_b})) = 2^n - 1 \tag{16}$$

Substituting Eqs. (14), (15), and (16) into Eq. (13), we obtain

$$C_n(B_{0\to 1}) = C_n(B_{0\to 1_a}) + C_n(B_{0\to 1_b}) + C_n\big(Connect\,(B_{0\to 1_a}, B_{0\to 1_b})\big) = [2^{n+1} - 9] + [C_{n-1}(B_{0\to 1}) + 2] + [2^n - 1] \quad (17)$$

The complexity of Eq. (17) is computed by induction. We will prove that:

$$C_n(B_{0\to 1}) = 2^{n+2} + 2^{n+1} - 8(n+1) \quad \forall n \geq 3 \quad (18)$$

(i) For $n=3$, Eq. (17) results into:

$$C_3(B_{0\to 1}) = C_3(B_{0\to 1_a}) + C_3(B_{0\to 1_b}) + C_3(Connect(B_{0\to 1_a}, B_{0\to 1_b})) = [2^4 - 9] + [C_2(B_{0\to 1}) + 2] + [2^3 - 1] = 16 \quad (19)$$

where $C_{n-1}(B_{0\to 1}) = 0$, since a two-input gate includes one coefficient. It can be easily seen that Eq. (19) equals (18) for $n=3$.

(ii) We assume that Eq. (18) holds for $n=k$. That is:

$$C_k(B_{0\to 1}) = 2^{k+2} + 2^{k+1} - 8(k+1) \quad (20)$$

We will prove that Eq. (18) holds for $n=k+1$. Thus,

$$C_{k+1}(B_{0\to 1}) = C_{k+1}(B_{0\to 1_a}) + C_{k+1}(B_{0\to 1_b}) + C_{k+1}(Connect(B_{0\to 1_a}, B_{0\to 1_b})) = [2^{k+2} - 9] + [C_k(B_{0\to 1}) + 2] + [2^{k+1} - 1] = [2^{k+2} - 9] + [2^{k+2} + 2^{k+1} - 8(k+1) + 2] + [2^{k+1} - 1] = 2^{k+3} + 2^{k+2} - 8(k+2)$$

Eventually, $C_{k+1}(B_{0\to 1}) = 2^{k+3} + 2^{k+2} - 8(k+2)$.

To make clear the previous description of the estimation method regarding to the number of multiplications, the switching estimation of a 4-input AND gate is examined below.

The calculation of the part $A_{0\to 1}$ is shown in Figure 2. In the beginning the sub-part that corresponds to x_2, x_3 inputs (bits $n-2$ to $n-1$) is calculated and the partial product is stored four times (generally 2^{n-2} times). Afterwards, the sub-part that corresponds to x_1, x_2, x_3 inputs is calculated using the previous calculated partial

	Part $A_{0\to 1}$	**Part** $B_{0\to 1_a}$			**Part** $B_{0\to 1_b}$		
Word number	$x_0\,x_1\,x_2\,x_3$	$TC^{x_0,x_1}_{i_0 i_1, j_0 j_1}$	$TC^{x_0,x_2}_{i_0 i_2, j_0 j_2}$	$TC^{x_0,x_3}_{i_0 i_3, j_0 j_3}$	$TC^{x_1,x_2}_{i_1 i_2, j_1 j_2}$	$TC^{x_1,x_3}_{i_1 i_3, j_1 j_3}$	$TC^{x_2,x_3}_{i_2 i_3, j_2 j_3}$
0	0 0 0 0	00	00	00	00	00	00
1	0 0 0 1	00	00	01	00	01	01
2	0 0 1 0	00	01	10	01	00	10
3	0 0 1 1	00	01	11	01	01	11
4	0 1 0 0	01	00	00	10	10	00
5	0 1 0 1	01	00	01	10	11	01
6	0 1 1 0	01	01	10	11	10	10
7	0 1 1 1	01	01	11	11	11	11
8	1 0 0 0	10	10	10	00	00	00
9	1 0 0 1	10	10	11	00	01	01
10	1 0 1 0	10	11	10	01	00	10
11	1 0 1 1	10	11	11	01	01	11
12	1 1 0 0	11	10	10	10	10	00
13	1 1 0 1	11	10	11	10	11	01
14	1 1 1 0	11	11	10	11	10	10
15	1 1 1 1	11	11	11	11	11	11
Number of multipl.	27	23			Same as 3-inputs AND gate		

FIGURE 2 Encoding of a 4 inputs AND gate for the switching activity computation.

product and the product is stored two times. At the end the whole $A_{0\to1}$ is calculated performing 2^{n-1} multiplications. The total required number of multiplications of $A_{0\to1}$ is 27 (*i.e.*, $C_n(A_{0\to1}) = 2^{n+1}-5$).

The part $B_{0\to1}$ is split into two sub-parts $B_{0\to1_a}$ and $B_{0\to1_b}$. As it shown in Figure 1, 23 multiplications are required for the calculation of $B_{0\to1_a}$, while the part $B_{0\to1_b}$ is the same with the $B_{0\to1}$ part of a 3-input AND gate shown in Figure 3.

LEMMA 3 *The computational complexity of an n-input AND gate, using the method* [6] *is*:

$$C_n(E(y)) = (2^n - 1)(n^2 + n - 2) \qquad (21)$$

Proof It has been proved in [6] that the switching probability can be expressed as:

$$p(y_{i\to j}) = \sum_{\pi \in P_i} \sum_{\pi' \in P_j} \prod_{k=1}^{n} \left[p(x_{k_{i_k\to j_k}}) \prod_{1 \le k \le l \le n} TC^{x_k, x_l}_{i_k i_l, j_k j_l} \right] \qquad (22)$$

where P_i is the set of all paths of the corresponding OBDD in the ON set of f, P_j is the set of all paths of the corresponding OBDD in the OFF set of f, and $i_k, j_k = 0, 1, 2$ are the values of the variable x_k on the paths π and π', respectively. The number 2 denotes the *don't care* state.

By traversing the paths of the OBDD of an n-input AND gate to calculate the $p(y_{0\to1})$, the total number of products is equal to $N = (2^n - 1)$. Also, the required multiplications of each product are: $L = n + \binom{n}{2} - 1 = ((n^2 + n - 2)/2)$. Eventually, the total number of the required multiplications of $p(y_{0\to1})$ is $N \times L$ and thus, $C_n(p(y_{1\to0})) = (2^n - 1)((n^2+n-2)/2)$. Since $E(y) = 2E(y_{1\to0}) = 2E(y_{0\to1})$, it is obtained: $C_n(E(y)) = (2^n - 1)(n^2+n-2)$.

LEMMA 4 *The complexity of the switching activity, E(sw), of the proposed method is always smaller than the complexity of the method* [6].

Proof Since it holds: $n^2 = n^2 \Rightarrow n^2+n > n^2-15n \Rightarrow n^2+n-20 > n^2+n-30 \Rightarrow 2^n(n^2+n-20) > n^2+n-30$, from Eq. (21) and, (11) and (12), it is concluded that:

$$(2^n - 1)\frac{n^2+n-2}{2} > 2^{n+3} + 2^n - [8(n+1) - 6]$$
$$\Leftrightarrow 2^n(n^2+n-20) > n^2 - 15n - 30.$$

Table I shows the computational complexity of the proposed method and [6] in terms of multiplications for $n = 2, 3, \ldots, 10$ as well as the associated reductions. It can be noticed that the larger n, the larger the reduction.

	Part $A_{0\to1}$	Part $B_{0\to1_a}$		Part $B_{0\to1_b}$
Word number	$x_0\, x_1\, x_2$	$TC^{x_0,x_1}_{i_0 i_1, j_0 j_1}$	$TC^{x_0,x_2}_{i_0 i_2, j_0 j_2}$	$TC^{x_1,x_2}_{i_1 i_2, j_1 j_2}$
0	0 **0** ~~0~~	00	**00**	~~00~~
1	0 **0** ~~1~~	00	**01**	~~01~~
2	0 **1** ~~0~~	01	00	~~10~~
3	0 **1** ~~1~~	01	01	~~11~~
4	1 0 ~~0~~	10	**10**	~~00~~
5	1 0 ~~1~~	10	**11**	~~01~~
6	1 1 ~~0~~	11	10	~~10~~
7	1 1 ~~1~~	11	11	~~11~~
Number of multiplications	11	8		

FIGURE 3 Encoding of a 3-inputs AND gate for the switching activity computation.

TABLE I Complexity of the switching activity of an n-input basic gate

No. of multiplications for $E(y)$, $n \geq 2$	
$L = p(x_{i_k \to j_k})$	$2(2^{n+1}-5)$
$M = TC^{x_k x_l}_{i_k i_l, j_k j_l}$	0, $n=2$
	$2[2^{n+2}+2^{n+1}-8(n+1)-2]$, $n \geq 3$
L times M	$2(2^n-1)$
	12, $n=2$
Proposed approach	$2[2^{n+3}+2^n-8(n+2)]$, $n \geq 3$
Approach [6]	$(2^n-1)(n^2+n+2)$, $\forall n$

2.1.4. *Accuracy of the Proposed Method*

LEMMA 5 *The proposed method exhibits the same accuracy with method* [6].

Proof It is sufficient to prove that the proposed method and [6] result into identical transition probabilities. For that purpose a 3-input AND gate is considered. Employing Eq. (22), the switching probability $p(y_{0\to1})$ can be computed as follows:

$$\begin{aligned} p(y_{0\to1}) = {} & p^{x_0}_{0\to1} p^{x_1}_{2\to1} p^{x_2}_{2\to1} TC^{x_0,x_1}_{02,11} TC^{x_0,x_2}_{02,11} TC^{x_1,x_2}_{22,11} + \\ & + p^{x_0}_{1\to1} p^{x_1}_{0\to1} p^{x_2}_{2\to1} TC^{x_0,x_1}_{10,11} TC^{x_0,x_2}_{12,11} TC^{x_1,x_2}_{02,11} + \\ & + p^{x_0}_{1\to1} p^{x_1}_{1\to1} p^{x_2}_{0\to1} TC^{x_0,x_1}_{11,11} TC^{x_0,x_2}_{10,11} TC^{x_1,x_2}_{10,11} \end{aligned} \tag{23}$$

Substituting the *don't care* state (*i.e.*, subscript 2) with the values $\{0, 1\}$, Eq. (23) can be re-written as:

$$\left.\begin{aligned} p(y_{0\to1}) = {} & p^{x_0}_{0\to1} p^{x_1}_{1\to1} p^{x_2}_{1\to1} TC^{x_0,x_1}_{01,11} TC^{x_0,x_2}_{01,11} TC^{x_1,x_2}_{11,11} + \\ & + p^{x_0}_{1\to1} p^{x_1}_{0\to1} p^{x_2}_{1\to1} TC^{x_0,x_1}_{10,11} TC^{x_0,x_2}_{11,11} TC^{x_1,x_2}_{01,11} + \\ & + p^{x_0}_{1\to1} p^{x_1}_{1\to1} p^{x_2}_{0\to1} TC^{x_0,x_1}_{11,11} TC^{x_0,x_2}_{10,11} TC^{x_1,x_2}_{10,11} + \\ & + p^{x_0}_{0\to1} p^{x_1}_{0\to1} p^{x_2}_{1\to1} TC^{x_0,x_1}_{00,11} TC^{x_0,x_2}_{01,11} TC^{x_1,x_2}_{01,11} + \\ & + p^{x_0}_{0\to1} p^{x_1}_{1\to1} p^{x_2}_{0\to1} TC^{x_0,x_1}_{01,11} TC^{x_0,x_2}_{00,11} TC^{x_1,x_2}_{10,11} + \\ & + p^{x_0}_{1\to1} p^{x_1}_{0\to1} p^{x_2}_{0\to1} TC^{x_0,x_1}_{10,11} TC^{x_0,x_2}_{10,11} TC^{x_1,x_2}_{00,11} + \\ & + p^{x_0}_{0\to1} p^{x_1}_{0\to1} p^{x_2}_{0\to1} TC^{x_0,x_1}_{00,11} TC^{x_0,x_2}_{00,11} TC^{x_1,x_2}_{00,11} \end{aligned}\right\} \tag{24}$$

It is concluded that Eqs. (5) and (24) are identical.

2.2. Switching Activity Computation of a Logic Network

Taking into account all types of correlation, the switching activity calculation of any gate output, needs the TCCs of its inputs. However, only the TCCs of the primary inputs of the logic network are provided. Consequently, a mechanism for the calculation and propagation of the TCCs through the wires of all circuit levels must be developed. First, the theoretical framework for the calculation and propagation of the TCCs is given. Then, the implemented method for the propagation of these coefficient is also presented. It should be stressed that the proposed method based on a pre-possessing of the logic network, achieves to propagate only the required TCCs and therefore, significant savings can be achieved.

2.2.1. *Propagation of the Transition Correlation Coefficients*

It has been proved [6] that the correlation coefficient between a signal x and node f with immediate inputs $x_0, x_1, \ldots, x_{n-1}$, from which at least one depends on the signal x, is:

$$TC^{f\,x}_{ip,jq} = \frac{p(f_{i\to j} \wedge x_{p\to q})}{p(f_{i\to j})\, p(x_{p\to q})} \tag{25}$$

where $i, j, p, q \in \{0, 1\}$.

Since the transition probabilities of the node f and signal x have been already computed, the problem is reduced to the computation of $p(f_{i\to j} \wedge x_{p\to q})$. Also, $TC^{f\,x}_{ip,iq}$ is computed by [6]:

$$\begin{aligned} & TC^{f\,x}_{ip,jq} \\ & = \left(\sum_{p \in P_i} \sum_{p' \in P_j} \prod_{k=1}^{n} \left[TC^{x_k\,x}_{i_k p, j_k q} p\left(x_{k_{i_k \to j_k}}\right) \right. \right. \\ & \qquad \left. \left. \prod_{1 \leq k \leq l \leq n} TC^{x_k, x_l}_{i_k i_l, j_k j_l} \right] \right) \Big/ p(f_{i\to j}) \end{aligned} \tag{26}$$

It can be seen that the numerator of Eq. (26) consists of: (i) the product of $TC^{x_k\,x}_{i_k p, j_k q}$'s, (ii) the product of $p(x_{k_{i_k \to j_k}})$'s, and (iii) the product of the $TC^{x_k, x_l}_{i_k i_l, j_k j_l}$'s. Comparing Eq. (26) with (5), we infer that both equations similar structure except the first part. Consequently, the computational complexity in terms of multiplications is the complexity of

Eq. (5) plus $(2^n-1)(n-1)$ multiplications due to the first part.

LEMMA 6 *Let f be the output of an n-input AND gate and x be an arbitrary signal of a logic network. The number of the required multiplications for calculating of one TCC between two signals f and x is computed by*:

$$C_{TCC}(n) = (2^n - 1)(n^2 + 3n - 2) \qquad (27)$$

Proof Employing the approach of Lemma 3, we infer that n additional multiplications are required, since there exist n additional TCCs, $TC^{x_k\,x}_{i_k p, j_k q}$, that is $R = n + n + \binom{n}{2} - 1 = ((n^2 + 3n - 2)/2)$. Therefore, the total number of multiplications is $N \times R$. Eventually, $C_{TCC}(n) = p(y_{0\to 1}) + p(y_{1\to 0}) = (2^n - 1)(n^2 + 3n - 2)$. Identical results can be derived if f is the output of one of the remaining basic gates.

Table II summarises, the computational complexity of the proposed method and Marculescou's one in terms of the multiplications. It must be noticed that the Table II expresses the computational complexity of the *TCs* when the node f performs a $1 \to 0$ or a $0 \to 1$ transition (*i.e.*, $i, j = 0, 1$ or $i, j = 1, 0$). Since $TC^{f\,x}_{ip,jq}$ with $i, j = 0, 1$ or $i, j = 1, 0$ and $p, q \in \{0, 1\}$, this case covers 8 of the 16 coefficients.

In case of a transition between the non-controlling values of a gate with output f, for instance an AND gate, it means that $i, j = 1, 1$ and the required number of multiplications is equal to $(n-1) + (n-1) + \left(\binom{n}{2} - 1\right) + 2 = ((n^2 + 3n)/2)$. The paths π and π' are identical and due to the fact that are reached at the non-controlling value of the gate, only one path exists. Therefore, the part C consists of n terms and requires $n-1$ multiplications, the part A consists of n terms and requires $n-1$ multiplications, and the part B consists of $\binom{n}{2}$ terms and requires $\left(\binom{n}{2} - 1\right)$ multiplications. Eventually, two additional multiplications are required for the connection of the three parts. This case covers 4 of the 16 coefficients since $TC^{f\,x}_{ip,jq}$, $i, j =$ "*non controlling value*", and $p, q \in \{0, 1\}$.

The four remaining TCCs stem from the controlling values of a gate. Up to now the first 12 TCCs have been already calculated. However, it has been proved [6] that the system of the sixteen TCCs can be solved when at least 9 of the 16 coefficients are known.

LEMMA 7 *The complexity of the propagation of TCCs of the proposed method is always less than the corresponding complexity of* [6] *when $f_{0\to 1}$ or $f_{1\to 0}$.*

Proof Due the fact that the additional multiplications, $(2^n-1)(n-1)$, of Eq. (29) is added to the complexity of both methods and using Lemma 6, we conclude that the proposed method has less complexity.

TABLE II Complexity for the propagation of one *TC*, in terms of multiplications

	Number of multiplications for $TC^{f,x}_{ip,jq}$, $n \geq 2$	
	8 *TCs*, $i=0$ and $j=1$, $i=1$ and $j=0$, $p, q \in \{0,1\}$	4 *TCs*, $i, j =$ "non-controlling value", $p, q \in \{0,1\}$
$L = p(x_{k_{ik\to jk}})$	$2^{n+1} - 5$	$n-1$
$M = TC^{x_k x_l}_{i_k i_l, j_k j_l}$	0, $n=2$ $2^{n+2} + 2^{n+1} - 8(n+1) - 2$, $n \geq 3$	$\binom{n}{2} - 1$
$K = TC^{x_k, x}_{i_k p, j_k q}$	$(2^n - 1)(n-1)$	$n-1$
L times M	$2^n - 1$	1
K times L	$2^n - 1$	1
Proposed approach	24, $n=2$ $2^{n+3} + 2^n(n+1) - 9n - 16$, $n \geq 3$	$2n + \binom{n}{2} - 1$
Approach [6]	$(2^n - 1)\left[2n + \binom{n}{2} - 1\right]$	$2n + \binom{n}{2} - 1$

2.2.2. *The Proposed Algorithm*

The proposed algorithm performs: (i) the circuit pre-processing, (ii) the calculation and propagation of TCCs, and (iii) the calculation of the switching activity of any node. In particular, the circuit pre-processing is a forward traversal from the primary inputs to the primary outputs and consists of the steps:

(i) *Identification of the gate type*: We specify the type of each basic gate and thus, the proper formula for the switching activity calculation.
(ii) *Levelization of the circuit*: We specify the logic level of the logic network in which a gate belongs to.
(iii) *Correlation Level Length*: The Correlation Level Length of a node g, CLL_g, specifies the number of the logic levels, whose signal correlations are considered for calculating node g switching activity. Apparently, if two signals x_0 and x_1 have CLL_g greater than a chosen CLL, the signals are uncorrelated, that is $TC_{ij,pq}^{x_0,x_1} = 1$.
(iv) *Correlation List*: Choosing a certain CLL_g, the *Correlation List* of a node g, CL_g, specifies the correlated signal pairs.

The structure of the developed algorithm is:

function *power_estimation* (F, X) *–F= circuit, X= set of primary inputs*
begin
for each *gate* $g \in F$:
1. *find the type of gate g*
2. *find the level of gate g*
3. *construct the dependence list* L_g
4. *mark the proper TCCs of the pairs in* L_g
for each *level i*
for each *gate* $g \in F$: *calculate the transition probability* $E(g)$
for each *pair of signals of level i: precompute the marked TCCs*
return *switching activities* $E(g)$ *for each node g*
end function *power_estimation*;

Example The application of the previous algorithm is illustrated by a certain logic network shown in Figure 4. Our main purpose is to show the reduction of the computational complexity using the Correlation List.

The logic network shown in Figure 4 consists of: 6 primary inputs, 2 primary outputs, and 6 levels. The level and correlation list if $CLL = 2$, of the node x_{11} are: $level(x_{11}) = \max\{Level(x_9), Level\ (x_{10})\} + 1 = \max\{3, 2\} + 1 = 4$ and $CL_{x_{11}} = \{x_9, x_{10}, x_7, x_8, x_4\}$, respectively. Furthermore, the contents of the Correlation List, $CL_{x_{11}}$ for a full transition of the node x_{11} will be found. The associated probability in the case node x_{11} performs a $1 \rightarrow 0$ transition is

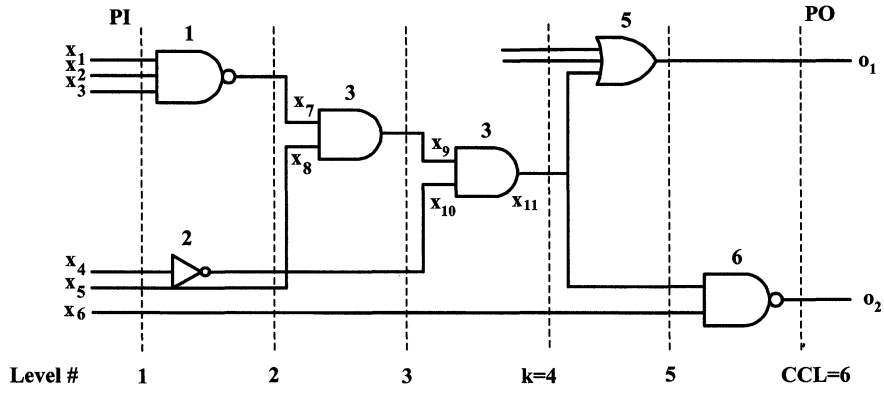

FIGURE 4 A logic network.

given by:

$$E_{1\to 0}(x_{11}) = p_{1\to 0}^{x_9} p_{1\to 1}^{x_{10}} TC_{11,01}^{x_9,x_{10}} + \\ + p_{1\to 1}^{x_9} p_{1\to 0}^{x_{10}} TC_{11,10}^{x_9,x_{10}} + \\ + p_{1\to 0}^{x_9} p_{1\to 0}^{x_{10}} TC_{11,00}^{x_9,x_{10}} \quad (28)$$

Since $CLL = 2$ the appropriate pairwise correlation coefficients between the signals (x_7, x_{10}) and signals (x_8, x_{10}) must be computed. Taking into account the Eq. (26) the numerator which corresponds to the $TC_{11,01}^{x_9,x_{10}}$ is equal to:

$$\begin{cases} TC_{11,01}^{x_7,x_{10}} TC_{11,01}^{x_8,x_{10}} p_{1\to 0}^{x_7} p_{1\to 0}^{x_8} TC_{11,00}^{x_7,x_8} + \\ + TC_{11,01}^{x_7,x_{10}} TC_{11,11}^{x_8,x_{10}} p_{1\to 0}^{x_7} p_{1\to 1}^{x_8} TC_{11,01}^{x_7,x_8} + \\ + TC_{11,11}^{x_7,x_{10}} TC_{11,01}^{x_8,x_{10}} p_{1\to 1}^{x_7} p_{1\to 0}^{x_8} TC_{11,10}^{x_7,g_2} \end{cases} \quad (29)$$

while the corresponding numerator of $TC_{11,10}^{x_9,x_{10}}$ is equals to:

$$TC_{11,10}^{x_7,x_{10}} TC_{11,10}^{x_8,x_{10}} p_{1\to 1}^{x_7} p_{1\to 1}^{x_8} TC_{11,11}^{x_7,x_8} \quad (30)$$

and eventually, the corresponding numerator of $TC_{11,00}^{x_9,x_{10}}$ is equals to:

$$\begin{cases} TC_{11,00}^{x_7,x_{10}} TC_{11,00}^{x_8,x_{10}} p_{1\to 0}^{x_7} p_{1\to 0}^{x_8} TC_{11,00}^{x_7,x_8} + \\ + TC_{11,00}^{x_7,x_{10}} TC_{11,10}^{x_8,x_{10}} p_{1\to 0}^{x_7} p_{1\to 1}^{x_8} TC_{11,01}^{x_7,x_8} + \\ + TC_{11,10}^{x_7,x_{10}} TC_{11,00}^{x_8,x_{10}} p_{1\to 1}^{x_7} p_{1\to 0}^{x_8} TC_{11,10}^{x_7,x_8} \end{cases} \quad (31)$$

Finally, the necessary correlation coefficients between the signals (x_7, x_{10}) and (x_8, x_{10}) can be summarized as follows:

$$CL_{1_{x_{11}}} = \{TC_{11,01}^{x_7,x_{10}}, TC_{11,11}^{x_7,x_{10}}, TC_{11,10}^{x_7,x_{10}}, TC_{11,00}^{x_7,x_{10}}\} \quad (32)$$

$$CL_{2_{x_{11}}} = \{TC_{11,01}^{x_8,x_{10}}, TC_{11,11}^{x_8,x_{10}}, TC_{11,10}^{x_8,x_{10}}, TC_{11,00}^{x_8,x_{10}}\} \quad (33)$$

Following a similar analysis for the $0 \to 1$ transitions it can be found that:

$$CL_{3x_{11}} = \{TC_{00,11}^{x_7,x_{10}}, TC_{10,11}^{x_7,x_{10}}, TC_{01,11}^{x_7,x_{10}}\} \quad (34)$$

$$CL_{4x_{11}} = \{TC_{00,11}^{x_8,x_{10}}, TC_{10,11}^{x_8,x_{10}}, TC_{01,11}^{x_8,x_{10}}\} \quad (35)$$

Eventually,

$$CL_{x_{11}} = \bigcup_{i=1}^{4} CL_{i_{x_{11}}} \quad (36)$$

Therefore, the required number of correlation coefficients is a subset of the sixteen coefficients of the each pair (x_7, x_{10}) and (x_8, x_{10}). Hence the above example shows the usefulness of the Correlation List in the reduction of the computational complexity.

3. RESULTS

The proposed method was implemented by C language and the experiments are performed on HP 735 workstation with 64 MB of memory.

Table III describes the characteristics of the benchmark circuits in terms of the number of the primary inputs, n, the primary outputs, m, the logic levels, L, and the number of gates.

Tables IV and V show the computational complexity of the proposed method and the approach of [6] in terms of the additions and multiplications for certain ISCAS circuits, considering $CLL = 3$ and $CLL = 6$, respectively. Column 2 gives the number, S, of the pairs of the correlated signals. Column 3 gives the required number of additions, which is the same for the two methods. Column 6 gives the percentage of the multiplication reduction. It must be noticed that the larger the Correlation Level Length, the larger the number of the correlated signals, since more pairs of signals are correlated.

In Table VI, power estimation results for seven large ISCAS benchmark circuits for a permitted

TABLE III Characteristics of ISCAS benchmark circuits

Circuit	# inputs	# outputs	# gates	# levels
C17	5	2	6	4
C432	32	7	184	21
C499	41	32	176	18
C880	60	26	221	23
C1355	41	32	180	16
C1908	33	25	205	22
C3540	50	22	1007	36
C6288	32	32	1491	74
alu4	14	8	547	37
z4ml	7	4	98	15
duke2	22	29	306	8

TABLE IV Comparison results for $CLL = 3$

Circuit	S	1,2 (+)	1 (*)	2 (*)	Gain %	Time (sec)
C17	19	524	464	512	+9.38	0.02
C432	2152	1070790	3555780	12041100	+70.47	38.08
C499	2472	197150	260252	313730	+17.05	4.01
C880	2052	174166	280880	407458	+31.07	4.27
C1355	2659	241524	342213	443475	+22.83	5.35
C1908	2495	1087300	3252930	5837080	+44.27	36.31
C3540	10524	1192420	2397970	4577050	+47.61	30.24
C6288	15286	1276930	1303120	1600930	+18.6	27.00
Alu4	2947	299674	527321	989751	+46.72	7.09
Z4ml	199	10126	9612	10482	+8.3	0.20
Duke2	5542	12341800	50629900	134862000	+62.46	521.85

(1) Proposed method, (2) [6]; (+) number of additions; (*) number of multiplications.

TABLE V Comparison results for $CLL = 6$

Circuit	S	1,2 (+)	1 (*)	2 (*)	Gain %	Time (sec)
C17	19	524	464	512	+9.38	0.01
C432	6909	2807330	11093600	31525500	+64.81	118.44
C499	6913	536762	631885	699713	+9.69	9.71
C880	6234	396978	645379	824143	+21.69	9.7
C1355	5667	472046	522461	600483	+12.99	8.83
C1908	5036	831122	1730760	2822290	+38.68	43.1
C3540	29932	5343370	15780800	38926700	+59.46	176.61
C6288	28794	2364310	2432780	3049380	+20.22	49.38
Alu4	8933	985776	1812830	2683400	+32.44	22.94
Z4ml	307	13164	12608	13598	+7.28	0.23
Duke2	5623	12359200	50632700	134535000	+62.36	522.49

(1) Proposed method, (2) [6]; (+) number of additions; (*) number of multiplications.

level of correlation $CLL = 3$ are presented. For these results a pseudo-random input vector set is used and the absolute error in a node-by-node comparison is reported. As it is shown, the MAX, MEAN, RMS and STD errors are small enough even for this small level of CLL.

Finally in Table VII, power estimation results with $CLL = 3$ are reported, using as input vector set a highly correlated input vector from a binary counter sequence. The reported errors are higher than the errors that are reported in previous Table VI, but they are still acceptable. All the values of power consumption are in μW at 20 MHz and 5 Volts.

The power estimation tool, which has been used to obtain the results of Tables VI and VII, is an

TABLE VI Power estimation results for $CLL = 3$ and pseudo-random inputs

Circuit	MAX	MEAN	RMS	STD	Tot. Power
C432	0.1837	0.0289	0.0460	0.0360	3209.81
C499	0.0650	0.0137	0.0179	0.0130	7780.56
C880	0.0687	0.0137	0.0204	0.0166	6372.55
C1355	0.0222	0.0041	0.0052	0.0030	6699.17
C1908	0.1346	0.0095	0.0200	0.0177	7153.51
C3540	0.1999	0.0517	0.0505	0.0408	15802.45
C6288	0.0870	0.0139	0.0233	0.0193	46687.58

TABLE VII Power estimation results for $CLL = 3$ and highly correlated inputs

Circuit	MAX	MEAN	RMS	STD	Tot. Power
C432	0.2642	0.0225	0.0567	0.0567	305.98
C499	0.1573	0.0429	0.0797	0.0615	2371.66
C880	0.0175	0.0013	0.0041	0.0039	251.45
C1355	0.1840	0.0216	0.0537	0.0452	1936.79
C1908	0.3864	0.0306	0.0893	0.0826	3000.16
C3540	0.0271	0.0265	0.0030	0.0031	161.52
C6288	0.1809	0.0234	0.0502	0.0466	8758.81

in-house developed tool. It consists of the following components:

(i) a library of primitive gates used to perform the mapping of the circuit,
(ii) a vector file (text file) corresponding to the applied input vector set,
(iii) a capacitance file, which provides the capacitance information of every circuit node. In case of the capacitance file is not available an estimation is used considering the fanout of each node,
(iv) the proposed switching activity estimator implemented in C.

A SLIF format or structural VHDL can be used to describe the circuit. More details on this tool can be found in: [14].

4. CONCLUSIONS

An efficient method for switching activity estimation of logic level networks is proposed. The method had as inputs the static and transition probabilities, the data correlations, and the exact structure of the logic network. New formulas for calculating the switching activity of a single gate, which are used by a novel algorithm for estimating the activity of any node, are proposed. The method provides accurate switching activity values, with small time cost. The experimental results proved that significant reduction of the required multiplications can be achieved.

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APPENDIX I

(A) The transition activity of an n-input NAND gate is given by:

$$E(y) = \sum_{j=0}^{2^n-2} \left(\prod_{i=0}^{n-2} A_{1\to 0} \prod_{k=0}^{n-2} \prod_{l=k+1}^{n-1} B_{1\to 0} \right) + \sum_{j=0}^{2^n-2} \left(\prod_{i=0}^{n-2} A_{0\to 1} \prod_{k=0}^{n-2} \prod_{l=k+1}^{n-1} B_{0\to 1} \right) \quad \text{(I1)}$$

where:

$$A_{1\to 0} = b_i(j) p_{1\to 1}^{x_i} + (1 - b_i(j)) p_{0\to 1}^{x_i}$$

$$B_{1\to 0} = \{ b_k(j) b_l(j)\, TC_{11,11}^{x_k,x_l} + (1 - b_k(j))\, b_l(j)\, TC_{11,01}^{x_k,x_l} +$$

$$
\begin{aligned}
&+ b_k(j)(1-b_l(j))\,TC^{x_k,x_l}_{11,10} + \\
&+ (1-b_k(j))(1-b_l(j))\,TC^{x_k,x_l}_{11,00}\}\\
A_{0\to1} &= b_i(j)p^{x_i}_{1\to1} + (1-b_i(j))\,p^{x_i}_{1\to0}\\
B_{0\to1} &= \{b_k(j)b_l(j)\,TC^{x_k,x_l}_{11,11} + \\
&+ (1-b_k(j))\,b_l(j)\,TC^{x_k,x_l}_{01,11} + \\
&+ b_k(j)\,(1-b_l(j))\,TC^{x_k,x_l}_{10,11} + \\
&+ (1-b_k(j))\,(1-b_l(j))\,TC^{x_k,x_l}_{11,00}\}
\end{aligned}
$$

(B) The transition activity of an n-input OR gate is given by:

$$
\begin{aligned}
E(y) = &\sum_{j=0}^{2^n-2}\left(\prod_{i=0}^{n-2}A_{1\to0}\prod_{k=0}^{n-2}\prod_{l=k+1}^{n-1}B_{1\to0}\right)\\
&+\sum_{j=0}^{2^n-2}\left(\prod_{i=0}^{n-2}A_{0\to1}\prod_{k=0}^{n-2}\prod_{l=k+1}^{n-1}B_{0\to1}\right) \qquad \text{(I2)}
\end{aligned}
$$

where:

$$
\begin{aligned}
A_{1\to0} &= b_i(j)p^{x_i}_{0\to0} + (1-b_i(j))p^{x_i}_{1\to0}\\
B_{1\to0} &= \{b_k(j)b_l(j)\,TC^{x_k,x_l}_{00,00} + \\
&+ (1-b_k(j))\,b_l(j)\,TC^{x_k,x_l}_{10,00} + \\
&+ b_k(j)\,(1-b_l(j))\,TC^{x_k,x_l}_{01,00} + \\
&+ (1-b_k(j))\,(1-b_l(j))\,TC^{x_k,x_l}_{11,00}\}\\
A_{0\to1} &= b_i(j)p^{x_i}_{0\to0} + (1-b_i(j))\,p^{x_i}_{0\to1}\\
B_{0\to1} &= \{b_k(j)b_l(j)\,TC^{x_k,x_l}_{00,00} + \\
&+ (1-b_k(j))\,b_l(j)\,TC^{x_k,x_l}_{00,10} + \\
&+ b_k(j)\,(1-b_l(j))\,TC^{x_k,x_l}_{00,01} + \\
&+ (1-b_k(j))\,(1-b_l(j))\,TC^{x_k,x_l}_{00,11}\}
\end{aligned}
$$

(C) The transition activity of an n-input NOR gate is given by:

$$
\begin{aligned}
E(y) = &\sum_{j=0}^{2^n-2}\left(\prod_{i=0}^{n-2}A_{1\to0}\prod_{k=0}^{n-2}\prod_{l=k+1}^{n-1}B_{1\to0}\right)\\
&+\sum_{j=0}^{2^n-2}\left(\prod_{i=0}^{n-2}A_{0\to1}\prod_{k=0}^{n-2}\prod_{l=k+1}^{n-1}B_{0\to1}\right) \qquad \text{(I3)}
\end{aligned}
$$

where:

$$
\begin{aligned}
A_{1\to0} &= b_i(j)p^{x_i}_{0\to0} + (1-b_i(j))p^{x_i}_{0\to1}\\
B_{1\to0} &= \{b_k(j)b_l(j)\,TC^{x_k,x_l}_{00,00} + \\
&+ (1-b_k(j))b_l(j)\,TC^{x_k,x_l}_{10,00} + \\
&+ b_k(j)\,(1-b_l(j))\,TC^{x_k,x_l}_{01,00} + \\
&+ (1-b_k(j))\,(1-b_l(j))\,TC^{x_k,x_l}_{11,00}\}\\
A_{0\to1} &= b_i(j)p^{x_i}_{0\to0} + (1-b_i(j))\,p^{x_i}_{1\to0}\\
B_{0\to1} &= \{b_k(j)b_l(j)\,TC^{x_k,x_l}_{00,00} + \\
&+ (1-b_k(j))\,b_l(j)\,TC^{x_k,x_l}_{00,10} + \\
&+ b_k(j)\,(1-b_l(j))\,TC^{x_k,x_l}_{00,01} + \\
&+ (1-b_k(j))\,(1-b_l(j))\,TC^{x_k,x_l}_{00,11}\}
\end{aligned}
$$

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