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Low Power Digital Multimedia Telecommunication Designs

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The increasing prominence of wireless multimedia systems and the need to limit power capability in very-high density VLSI chips have led to rapid and innovative developments in low-power design. Power reduction has emerged as a significant design constraint in VLSI design. The need for wireless multimedia systems leads to much higher power consumption than traditional portable applications. This paper presents possible optimization technique to reduce the energy consumption for wireless multimedia communication systems. Four topics are presented in the wireless communication systems subsection which deal with architectures such as PN acquisition, parallel correlator, matched filter and channel coding. Two topics include the IDCT and motion estimation in multimedia application.

These topics consider algorithms and architectures for low power design such as using hybrid architecture in PN acquisition, analyzing the algorithm and optimizing the sample storage in parallel correlator, using complex matched filter that analog operational circuits controlled by digital signals, adopting bit serial arithmetic for the ACS operation in viterbi decoder, using CRC to adaptively terminate the SOVA iteration in turbo decoder, using codesign in RS codec, disabling the processing elements as soon as the distortion values become great than the minimum distortion value in motion estimation, and exploiting the relative occurrence of zero-valued DCT coefficient in IDCT.

Keywords: Low-power; Wireless; Multimedia; Correlator; Matched filter; Channel coding; IDCT; Motion estimation

1. INTRODUCTION

In recent years, the need for personal mobile communications – "anytime, anywhere" access to data and communication service – has become increasingly clear. In addition, the portable multimedia systems are expected to be used more frequently and for longer durations [1]. This concern has been accelerated by the growing popularity of portable multimedia systems [2].

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The advent of Personal Communications Service (PCS) and Personal Data Assistant (PDA), the future trend is to run multimedia applications on those wireless devices. The need for high speed data and video transmission will lead to much higher power consumption than traditional portable applications [3]. Due to the limited power-supply capability of current battery technology, we are facing a dilemma that has two design problems to conquer. One is to explore high-performance design and implementation that can meet the stringent speed constraint for real-time multimedia applications. The other is to consider low-power design so as to prolong the operating them of the wireless multimedia systems (PCS/PDA devices) [3].

In this paper, we will review the design of low-power wireless multimedia systems. The structure of the paper is organized as follows. In Section 2, we introduce four low power designs techniques: PN acquisition, parallel correlator, matched filter and channel coding which corrects the error of received data in receiver. Section 3 introduces the design of an IDCT macrocell and motion estimation suited for mobile and the multimedia systems. In Section 4 we draw a conclusion.

2. WIRELESS COMMUNICATION

We discuss PN acquisition, (2) correlator, (3) matched filter and (4) channel coding in Code Division Multiple Access (CDMA) communication systems that are being widely deployed today.

(1) In spread-spectrum systems, the receiver must synchronize on to the transmitted PN (Pseudo-Noise) code and has to de-spread the received signal into original symbol by calculating the correlation of input data and the PN sequence [6].
(2) The correlator used to for cell synchronization, timing recovery, data recovery and channel estimation in a Direct Spread Code Division Multiple Access (DS-CDMA) receiver [23]. Synchronization process is to determine the location of a periodically occurring marker (say N bits long, where N may be as large as 256) transmitted by all transmitters (base station) in the system.
(3) In CDMA communications, matched filters and sliding correlators are usually employed in the despreading of spread-signal. Generally speaking, sliding correlator is suitable for narrow-band CDMA systems because it takes long time to carry out a complete correlation calculation for a long PN sequence. A matched filter, however, is more attractive in W-CDMA (Wideband Code Division Multiple Access) communication that high flexibility, spectral efficiency and advanced data services up to 2 Mbps because it just takes a single chip time to perform the correlation calculation.
(4) Power efficient system design requires attention to implementation of algorithms and functions as well as proper selection of system level components such as error-control coding and modulation schemes. We must consider what combinations of components give optimum performance. For error-control codes, we concentrate on the decoders because these consume much more power than the encoder. The decoder performance *vs.* power consumption tradeoffs for several common codes is compared [4, 5, 21]. It shows how we can optimize an example communication system with respect to energy consumption. For a given error-control code, tremendous savings in power consumption can be attained both through algorithm reformulation and architectural innovations specifically targeted for energy conservation. We shall revisit those power-hungry components as a following subsection.

2.1. PN Acquisition

To compute the autocorrelation function, either matched filters or serial correlators can be used. The matched filters compute values for the autocorrelation function after each chip duration

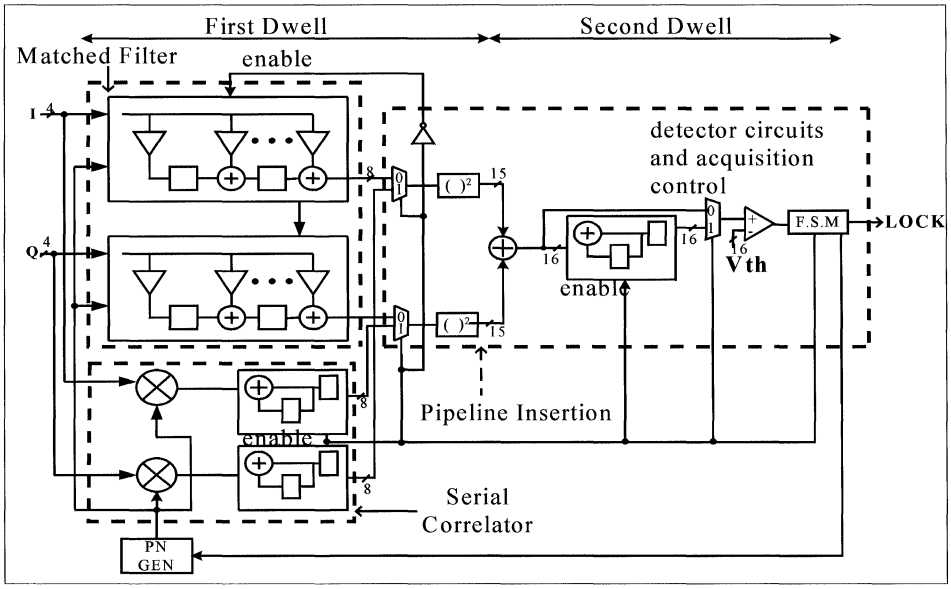

FIGURE 1 Hybrid PN acquisition architecture.

while serial correlators produce a value after each period of a data bit. Since a chip duration is much shorter than a data bit duration, the matched filters compute the autocorrelation values much faster than serial correlators. Consequently, the acquisition time, the amount of time takes to find the autocorrelation peak and thus the alignment of PN sequences, is much shorter for a matched filter design than serial. However, a matched filter design requires significantly higher complexity and power than a serial correlator. In the serial correlators approach, each value of the autocorrelation function is computed at the data rate, which is much slower compared to the chipping rate that the matched filters operate at.

The PN acquisition must process the spread-spectrum signal at a speed much faster than the transmitted data rate, its energy consumption can become significant and should be minimized for portable applications. Typically, either matched filter or serial correlators are used to acquire the PN code timing. We describe a hybrid PN acquisition architecture which employs both matched filters and serial correlators to achieve a lower energy consumption and fast acquisition time as compared to the traditional approaches of using either matched filters or serial correlators alone [6]. The result shows a factor-of-four reduction in energy for the hybrid scheme as compared to the matched filters architecture and a factor-of-two reduction in energy as compared to the serial architecture. Figure 1 shows the hybrid PN acquisition architecture that employs both matched filters and serial correlators. For better performance, a double dwell scheme is used.

The key to low energy dissipation in the hybrid architecture is to use low power serial correlators during the second dwell, while during the first dwell the higher power matched filters are used, so that a fast acquisition time can be maintained. In contrast, only in the matched filters approaches, the filters are used for the second dwell. Since the second dwell averages the autocorrelation value at a single code phase over many bits, the matched filters dissipate more energy than necessary.

2.2. Parallel Correlator

Direct Sequence Spread Spectrum (DSSS) transmissions require a despreading stage within the

standard receiver block to recover the spread spectrum signal. For long spread spectrum codes, the correlation block can be a large portion of the receiver size, hence a considerable portion of the power consumption. In [7], a correlator structure for detecting a periodically repeating marker sequence in W-CDMA systems is suggested.

We describe two power reduction alternatives for a parallel spread spectrum correlator, by analyzing the algorithm and designing a baseline correlator and by investigating how to streamline the arithmetic operations in one case, and optimizing the sample storage in the other.

A generally correlator structure is the shift register storage [8]. Given the shift register storage, there are potential power savings that can be realized in the adder tree by looking at the data statistics. As the data is shifted by one position, the previous coefficient and the new coefficient will remain the same for half the number of samples (in runs of length 2 or greater). In order to capture this behavior we define "bypass bits" (see Fig. 2) which tell the adder stages if a term is not changing and thus it has zero contribution to the difference between the present and next correlation sum.

By storing the previous sum and identifying the factors that are changing we can streamline the arithmetic operation to reduce the number of terms. The overall number of adders cannot be reduced as different codes change the locations of inactive adders, but we can shutdown the unused adder [8], and limit their power consumption. The equation for the correlator can be rewritten to express the new computation as follows,

$$y_k = y_{k-1} + 2\sum_{\tau=2}^{2^m-2}(h_\tau^*)x_{k-\tau} + h_1 x_{k-1} + h_{2^m-1}x_{k-2^m+1}$$
$$\text{where } h_\tau^* = h_\tau(h_\tau \oplus h_{\tau-1}) \qquad (1)$$

If the coefficient for a sample has not changed from the previous calculation, then h_t^* is 0 in (1), otherwise h_t^* will reflect the new polarity (+1 or −1). When the coefficient changes, the original sample value must be removed from the sum, and then the sample with the new polarity must be added. In order to take advantage of the new method of calculating the correlation sum, a specialized adder cell was developed as in Figure 3. In the case where a coefficient has not changed as a sample is shifted, its particular contribution to the overall sum should be zero.

When a term bypassed, the adder can be configured to ignore its value (using *cs*), and only pass the other input as the result (using *ca* or *cb*).

Another approach to reduce power dissipation is to reduce the activity in the storage area. A possible approach to reduce the unnecessary activity on the data-lines is to use a register file (with pointer) implementation instead of the n-bit wide shift register, as seen in Figure 4. With this scheme, only one register out of the total of $2m-1$ will experience clock and output transitions for each new sample. Because the global bus feeds every register in the register file, minimizing the transitions on this bus can reduce the overall power consumption considerably.

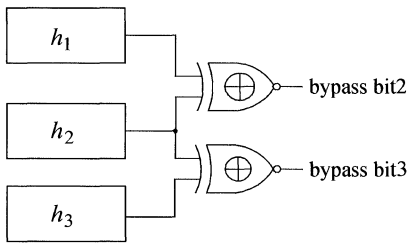

FIGURE 2 Bypass bit generation.

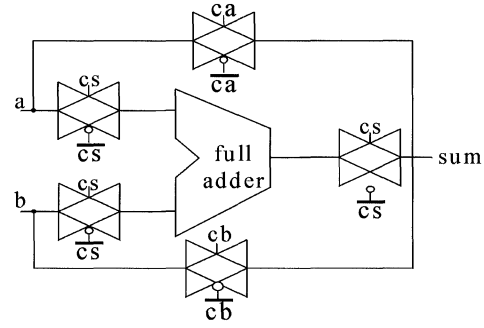

FIGURE 3 Modified adder cell with bypass function.

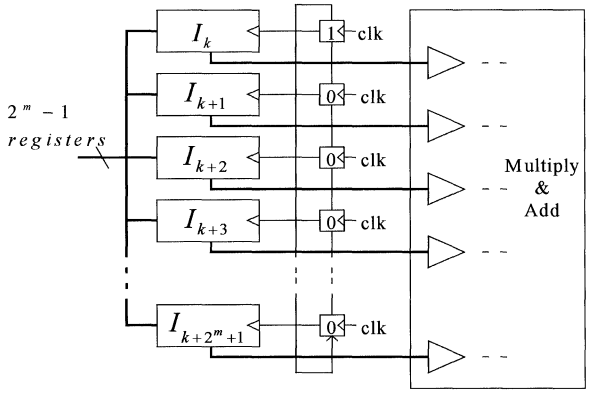

FIGURE 4 Register file concept.

A simple, but effective coding technique to reduce power is the Bus Invert method [22], and for a 6 bit bus, it reduces transition activity by approximately 20%.

2.3. Matched Filter

We describe the mixed analog-digital LSI implementation of a high-speed low-power complex matched filter. The basic idea behind the developed complex matched filter is that the massive and high-speed despreading operation of the QPSK modulated complex spread-signals are directly carried out in analog domain by using the low power analog operational circuits controlled by digital signals. Comparing to pure digital matched filters, two high-speed Analog-to-Digital (A/D) converters operating at chip rate are omitted, and the total dissipation power is greatly reduced [9].

We address the despreading algorithm of the complex matched filter for QPSK modulated spread-signal. A simplified CDMA receiver is shown in Figure 5. At the receiver side, after the RF demodulation and the quadrature demodulation, the spread baseband complex signal $R(t) = R_I(t) + j\ R_Q(t)$ is separated into an inphase signal $R_I(t)$ and a quadrature $R_Q(t)$, which are then despread by a matched filter bank combined with two A/D converters operating at chip rate. The despread signal $D(t) = D_I(t) + j\ D_Q(t)$, coming from the matched filter section is furthermore fed to a RAKE combiner in order to compensate for the fading or the multi-path effects by risen the radio channel. Now let us address the algorithm of the complex matched filter. Let N and T_C denote the number of taps and the chip duration of the PN codes, respectively, the despreading operation of the complex matched filter can be formulated as

$$\begin{aligned} D(t) &= \frac{1}{N}\sum_{i=1}^{N}\overline{C(i)}R(t - iT_C) \\ &= \frac{1}{N}\sum_{i=1}^{N}C_I(i)R_I(t - iT_C) + \frac{1}{N}\sum_{i=1}^{N}C_Q(i)R_Q(t - iT_C) \\ &\quad + j\frac{1}{N}\sum_{i=1}^{N}C_I(i)R_Q(t - iT_C) - j\frac{1}{N}\sum_{i=1}^{N}C_Q(i)R_I(t - iT_C) \end{aligned} \tag{2}$$

where C(i) are the PN codes.

Based on the algorithmic structure shown in Figure 6, a complex matched filter corresponding to 128-tap PN-codes can be realized by the system architecture shown in Figure 7. The four B-MFs shown in Figure 6 is configured by using two

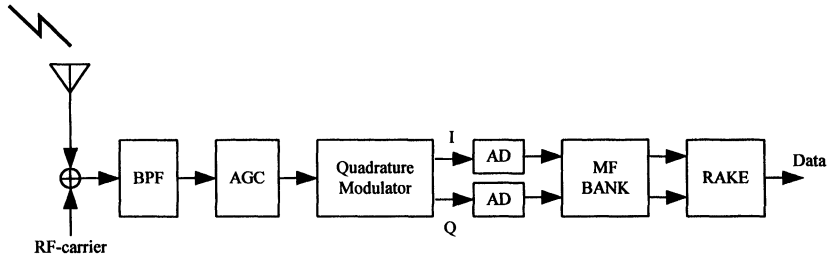

FIGURE 5 A simplified CDMA receiver.

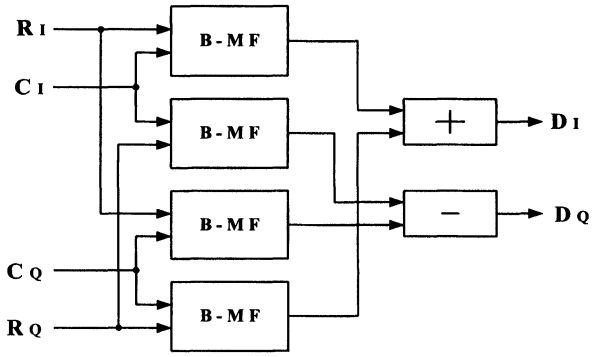

FIGURE 6 Algorithmic structure of a complex matched filter consisting of four basic matched filter (B-MF).

Sample-Hold (SH) banks with 128 units, four multiplex (MUX) banks with 128 units, eight sets of Analog Parallel Adder Bank (ADDB), four 8-input analog parallel subtracters. The ADDB consisting of four 32-input analog parallel adders is with 128-inputs and 4-outputs. The outputs of the four B-MFs are combined by 2-input analog subtracter and 2-input analog adder.

The digital circuits mainly consist of four 128-bit registers, a writing-register W-R, two PN-code operation register C_I-R and C_Q-R, and a clock generation register CLK-R. The writing-register W-R operates in serial-in and parallel-out used to temporarily store the PN sequence from outside, and load the stored data to the operational registers in parallel. The operational registers C_I-R and C_Q-R with parallel-input and parallel-output are self-shifted at chip rate to carry out the multiplication with the input spread analog signals $R_I(t)$ and $R_Q(t)$, respectively.

The register CLK-R with parallel-output is designed to generate 128 clock signals to control the two SH (Sample Hold)-banks.

Now let us describe the operational behaviors of the analog circuits. The spread inphase signal $R_I(t)$ is serially sampled and hold by the 128 SH-units controlled by the sample-hold clock signals of sclki, "i = 1, 2, ..., 128". For each SH-unit, the sampled-value is hold until the next sampling-pulse comes, and the hold-value is multiplied by the corresponding bit of the PN-code. Since the PN-code bit only takes the value of "1" corresponding to "+1" or "0" corresponding to "−1", the multiplication operation can be simply realized by a MUX which outputs the input-analog signal when the PN-code bit is "0". The output signal of each MUX is simultaneously connected to the analog parallel adder banks at plus-side and at

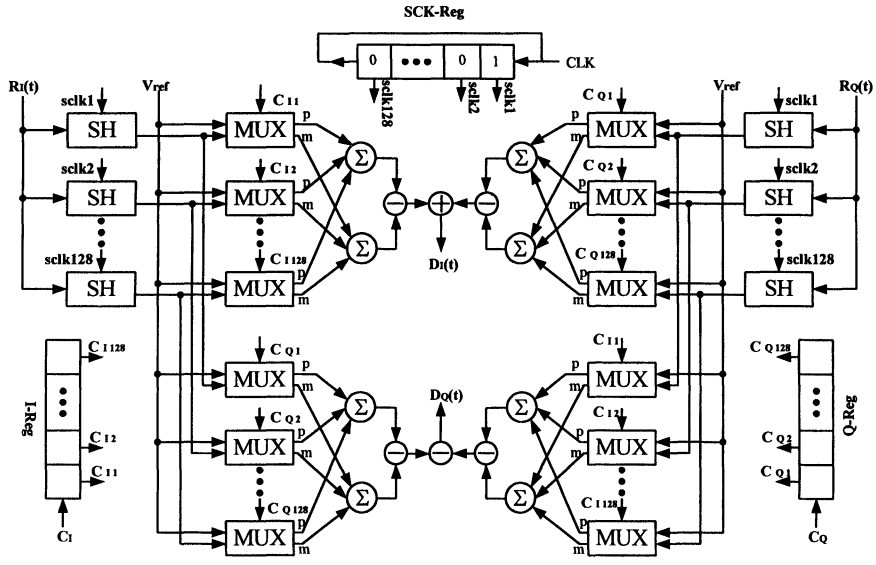

FIGURE 7 Architecture of the complex matched filter for 128-tap PN-code.

minus-side. The four output signals of each ADDB at the plus-side are subtracted with those of the ADDB at the minus-side, which gives the result of the B-MF operation. The output signals of the four B-MFs are finally combined by 2-input adder and 2-input subtracter to give the final results of $D_I(t)$ and $D_Q(t)$, respectively.

2.4. Channel Coding

The purpose of Forward Error Correction (FEC) is to improve the capacity of a channel by adding some carefully designed redundant information to the data being transmitted through the channel.

2.4.1. Bit-serial Viterbi Decoder

Viterbi decoders employed in digital wireless communications are complex and dissipate high power. The low-power design of Viterbi decoders has been an important issue for mobile and portable applications. The power dissipations of two different implementations of viterbi decoder (which is the register-exchange approach with less switching activity and the traceback approach with shift update scheme) is investigated [10].

This paragraph presents a low-power bit-serial Viterbi decoder chip [11] with the coding rate $r = 1/3$ and the constraint length $K = 9$ (256 states). The design of a low-power Viterbi decoder with a large number of states which is targeted for next generation wireless applications. We discuss the adopted *bit-serial arithmetic* for the ACS (Add-Compare-Select) operations. The bit-serial approach has made it possible to obtain an area and power efficient ACS architecture. The trace-back technique is very power efficient due to the use of application-specific memories.

The architecture of the bit-serial ACS unit is depicted in Figure 8. Each ACS unit has three full-adders. Two of them are used to add the state metrics and the branch metrics and the third one is used to compare two new state metrics. After processing the most significant bit, a decision bit is stored in a register and a new state metric is selected from two candidates stored in two sets of FIFO depending on the decision bit.

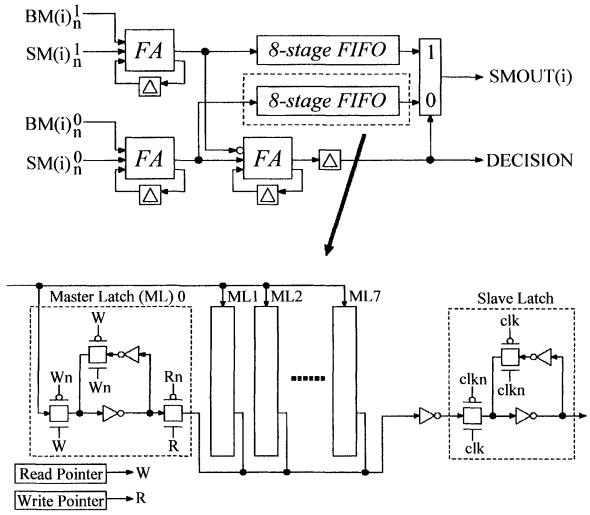

FIGURE 8 Bit-serial ACS unit.

The trace-back strategy is depicted in Figure 9, where W, T and D represent "WRITE", "TRACE BACK" and "RECODE", respectively. During "WRITE" operation, 256 decision bits are written to survivor path memories simultaneously. Both "TRACE BACK" and "DECODE" are read operations, but only "DECODE" gives decoded outputs. After 48 "TRACE BACK" operations, 24 decoded bits are obtained consecutively.

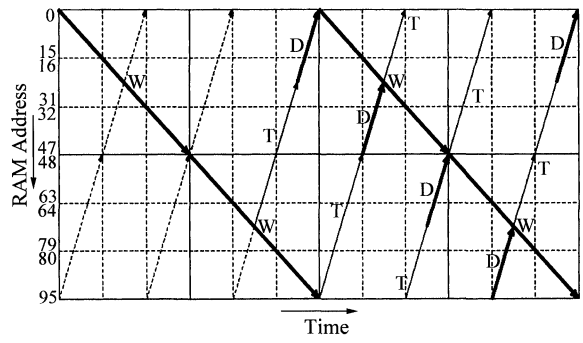

FIGURE 9 Trace back operation.

2.4.2. *Turbo Code Decoder*

One of the problems for decoding turbo code in the receiver is the complexity and the high power consumption since multiple iterations of Soft Output Viterbi Algorithm (SOVA) have to be carried out to decode a data frame. An approach using Cyclic Redundancy Checking (CRC) to adaptively terminate the SOVA iteration of each frame is presented [12]. This results in system that has variable workload of which the amount of computation required for each data frame is different. Dynamic voltage scaling is then used to further reduce the power consumption.

Turbo code consists of multiple RSC (Recursive Systematic Convolutional) component codes and the encoder creates a powerful code by feeding randomly shuffled (interleaved) versions of the same information sequence to the encoders of these component codes. Using the component code structures, the turbo code decoder first estimates the likelihood ratios of the information bits and then iteratively revises these estimates. For a turbo code with 2 component codes, one turbo decoding iteration corresponds to two SOVAs. It follows that the complexity of one iteration would correspond to that of four classical Viterbi decoders. Significant increase in the complexity also implies that the power consumption of the decoder goes up considerably, which has a fatal effect on many applications, especially portable applications.

We introduce a turbo code decoding algorithm using adaptive iteration. The basic idea is to employ a CRC scheme in each decoding iteration so that no redundant iteration will be performed once the frame is correctly decoded. Let S_{max} denote the maximum number of decoding iterations that can be used. The proposed adaptive iteration decoding algorithm is as follows.

(a) Initialize the number of iterations S to 1.
(b) Decode the frame using SOVA.
(c) Check if there is any bit error in the frame by checking the CRC.
(d) If the frame contains bit errors and $S < S_{max}$, increment S by 1 and go back to Step 2. Otherwise, stop.

This adaptive iteration decoding algorithm is shown in the Figure 10. The x_k are the received systematic bits and x_k' are the interleaved version of x_k. The $y_{k,1}$ and $y_{k,2}$ are the received coded bits after the first and second constituent recursive systematic encoders, respectively. $L_E(u_k)$ is the extrinsic information after the SOVA $\{u_k\}$ is the non-interleaved survivor sequence after passing through a SOVA. CRC is performed right after each SOVA.

2.4.3. *Reed-Solomon Codec*

Reed-Solomon (RS) coders are used for error control coding in many applications such as digital audio, digital TV, software radio, CD player, and

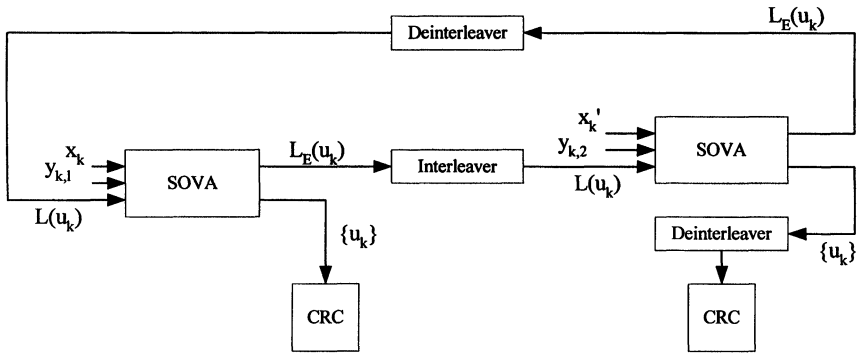

FIGURE 10 Turbo decoder employing SOVA with adaptive iteration algorithm.

wireless and satellite communications. These universal RS(n, k) codecs are to be implemented as a combination of hardware and software in application-specific DSP processor with specially designed programmable finite field datapath and dedicated and optimized software to reduce the total energy consumption.

This paragraph presents hardware/software codesign of low-energy programmable Reed-Solomon (RS) codecs [13]. With current scaled technologies, many DSP algorithms based on binary two's complementary arithmetic can be realized using domain specific programmable digital signal processor (DS-PDSP) optimized for targeted application.

If finite field arithmetic would be implemented in a programmable DSP datapath, the universal RS codecs (and other finite field based systems) could be easily implemented in software. A low-energy architecture, vector–vector (or vector-matrix) multiplications for one of the most frequently use DSP operations can lead to 70% energy reduction compared with the straightforward multiplication datapath containing one parallel multiplier.

Universal RS decoders are coded using this decoding algorithm as well as other frequency-domain and time-domain decoding schemes based on three types of datapath architectures presented in [14]. The performance characteristics of RS encoder and these RS decoders based on various datapaths are evaluated and compared.

A domain-specific programmable DSP processor (DS-PDSP) is assumed whose datapath is specialized for finite field operations, especially multiplications. These are two major operations involved in finite field multiplication, namely polynomial multiplication and polynomial modulo operation over GF (2). They can be implemented as a whole in one parallel multiplier as shown in the parallel datapath architecture in Figure 11(a). These two operations also were implemented using two separate units, a MAC array for polynomial multiplication and a DEGRED array for polynomial modulo operation, and with separate instruction, as illustrated in Figure 11(b). Using finite field vector–vector (or vector-matrix) multiplication operation (which are the most frequently used operation in finite field applications) as bench-mark, this datapath architecture can lead to 70% energy reduction compared with the datapath shown in Figure 11(a).

Low energy programming scheme for major computations in the RS encoding and decoding algorithms are as follows;

(A) *Vector–vector multiplications*

The vector–vector multiplications can be performed using N polynomial multiply-accumulate operations (*MAC*) and 1 polynomial modulo operation (*DEGRED*). This leads to about 70% energy reduction.

(B) *Convolution*

Convolution requires N *MAC* and 1 *DEGRED* operation.

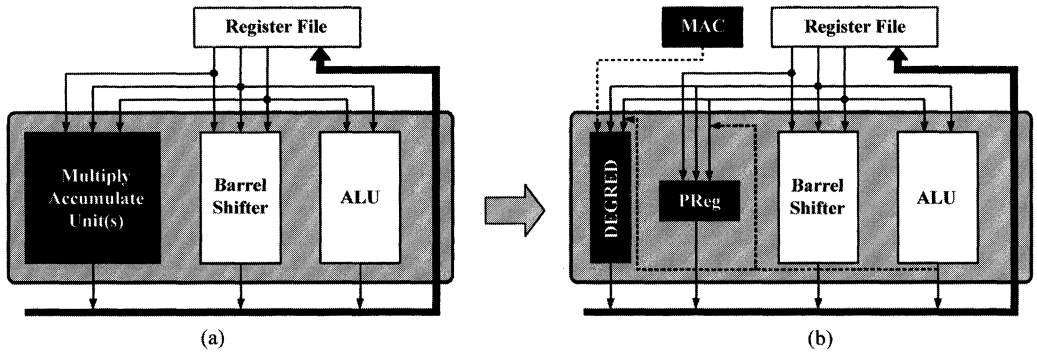

FIGURE 11 Finite field datapath architectures in a DS-PDSP processor. (a) Parallel datapath (b) (MAC + DEGRED) datapath.

(C) *Polynomial evaluation*

N memory accesses, N *MAC* operations and 1 *DEGRED* operation.

(D) *Finite field division*

$2(m-1)$ multiplications if the datapath in Figure 11(a) is used. $m-1$ *MAC* operation and $2(m-1)$ *DEGRED* operation if the datapath in Figure 11(b) is used.

For the comparison, the performance characteristics of RS encoders and five typical RS decoders are summarized as follows;

RSD1, uses the division-free BM (Berlekamp-Massey) algorithm for finding the error-locator polynomial.

RSD2, uses the original BM algorithm with division for finding the error-locator polynomial.

RSD3, is based on the Modified Euclidean algorithm.

RSD4, corresponds to the transform decoding algorithm, which uses the original frequency-domain BM algorithm and compute error polynomial using DFT/IDFT.

RSD5, is time domain RS decoding algorithm based on the division free BM algorithm and the coefficients of error polynomial are computed using the time-domain correspondence of Forney's algorithm.

Low-energy RS codecs through datapath selection.

We can conclude that the RS(255,247) encoder based on (MAC+DEGRED) datapath consume about 30.9% of the energy of the encoder based on the non-pipelined parallel multiplier (Mult(0-p)) datapath, about 42.7% of the energy of the encoder based on the one level pipelined parallel multiplier (Mult(1-p)) datapath. The RS decoder based on the (MAC+DEGRED) datapath consumes about 28.8% of the energy of that based on the (Mult(0-p)) datapath, about 40% of the energy of that based on the (Mult(1-p)) datapath. As a result, the energy-latency product of RSD1 decoder based on (MAC+DEGRED) is only 29.5% of that based on the (Mult(0-p)) datapath, 39.6% of that based on the (Mult(1-p)) datapath.

Low-energy RS codecs through algorithm selection.

RS decoding based on RSD4 and RSD5 consume much more energy than that based on the frequency-domain decoding algorithms RSD1, RSD2 and RSD3. Moreover, RS decoding based RSD4 and RSD5 also have much greater latency value. Therefore, they are not suitable for low-energy software implementations.

RSD1, RSD2 and RSD3 differ only in the computation of error locator polynomial and the error-evaluator polynomial. If the parallel multiplication datapaths (Mult(0-p) or (Mult(1-p)) are used, the RSD1 decoder outperform the RSD2 and RSD3 decoders for small t; as t increase ($t \geq 8$), the RSD2 decoder has the best performance. However, if the (MAC+DEGRED) datapath is used, the RS decoder programmed using RSD1 algorithm always consumes the least energy.

We can conclude that for RS(255, k) codes with the generally-used error-correcting range of $2 \leq t \leq 16$, the RS encoder using the generator-matrix approach and the RS decoder using the proposed RSD1 algorithm based on the (MAC+DEGRED) datapath have the best overall performance in term of both energy and energy-latency product.

3. MULTIMEDIA APPLICATION

In video coding, motion estimation has been shown to be very useful in reducing temporal redundancy but requires very high computational complexity. The most commonly used motion estimation architectures are based on the block matching motion estimation algorithm.

Discrete cosine transform (DCT), which can exploit the spatial redundancy, has played an important role in video compression standards. The technique for reducing power dissipation of the DCT by targeting the multiplier section of a DCT processor is presented [15]. The pivot of this technique is a multiplication algorithm for the low power implementation of the DCT on CMOS based signal processing systems. The algorithm reduces power consumption by reducing the

effective switched capacitance of the multiplier through effective manipulation of the multiplication process between the cosine and data matrices.

The computation complexity requirement makes hardware solution of inverse DCT (IDCT) be adopted in real time application.

3.1. Motion Estimation

Among the algorithms used for motion estimation by block matching, the FS-BM algorithm uses an exhaustive search to find the candidate block that is closest to the reference block. The low power full-search block matching (FSBM) motion estimation design for the H.263+ low bit rate video coding was proposed [16]. These registers that named as G register means that the clock of this register is gated control. To reduce the power consumption in each PE, this use gated clock control in the block accumulator.

FS-BM estimation processors typically adopt systolic array architecture and are responsible for the major part of power consumption in video coding system. Reference [17] eliminates unnecessary computations by computing a conservative estimation of distortion values before computing the exact value. There is another method of power consumption reduction by disabling the Processing Elements (PE) as soon as the distortion values become greater than the minimum distortion value already computed. Equation (3), (4) is conventional method of full search algorithm.

$$D(l,c) = \sum_{i=0}^{n-1} D_i(l,c);\ D_i(l,c) = \sum_{j=0}^{n-1} |x_t(i,j) - x_{t-1}(l+i, c+j)| \quad (3)$$

$$(u,v) = (l,c) | D\_\min[-p/2] \le l, \quad c \le [p/2] \quad (4)$$

Equation (5) is the method of disabling the PE.

$$\begin{aligned} &D^i(l,c) = D^{i-1}(l,c) + D_i(l,c);\ \ 0 \le i \le n-1 \\ &D_i(l,c) = \begin{cases} \sum_{j=0}^{n-1} |x_t(i,j) - x_{t-1}(l+i,c+j)|, & \text{if} D^{i-1}(l,c) < D\_\min_t \\ D_{i-1}(l,c), & \text{otherwise} \end{cases} \\ &D(l,c) = D^{n-1}(l,c) \\ &D\_\min_t = \min(D(l,c))\{(l,c)\} \in AAS \end{aligned} \quad (5)$$

The power consumption of the architectures is reduced by blocking new values of x the enter into the PEs, presenting the circuits to switch when $D_i(l,c) = D_{i-1}(l,c)$ in Eq. (5). For reduction power consumption with such pipeline architectures, it is necessary to compute $D^{i-1}(l,c)$ and $D\_\min_t$ on time to block the computation of $D_i(l,c)$. This problem can be solved by spacing out in time the computation of $D_i(l,c)$ and $D_{i+1}(l,c)$ for a given (l,c), *i.e.*, by computing in sequence partial distortion values for different candidate blocks.

The absolute differences corresponding to a single row of the reference block are accumulated for a line of candidate block in sequence (c loop). The (p+1) elements of the BLOCKING bit vector identify when the computation for any one of those candidate blocks should be disable. The (p+1) elements of this vector are updated in every iterations of the i loop, and the value of $D\_\min_t$ is updated after processing a line of candidate blocks.

```
D_min_t:=∞; BLOCKING(,,0):=FALSE
for l=[−p/2] to [p/2]
  for i=0 to n−1
    for c= [−p/2] to [p/2]
      for j=0 to n−1
        if BLOCKING(l,c,i)=FALSE then
D(l, c,i,j+1) := D(l,c,i,j) + | x_t (i,j)−x_{t−1}(l+i,c
+j)|
        end{j}
        D(l,c,i, n) := D(l,c,i,n) + D(l,c,i−1,n)
        if D(l,c,i,n) ≥ D_min_t then
BLOCKING(l,c,i+ 1) := TRUE
      end{c}
    end{i}
    for c= [−p/2] to [p/2]
      if D(l,c,n−1,n) < D_min_t then
        D_min_t := D(l,c,n−1,n); (u,v) := (l,c)
    end{c}
    end{l}
```

Algorithm 1. Single assignment code to derive low-power linear architecture

The low-power linear architecture proposed in Figure 12(a) is derived from the single assignment

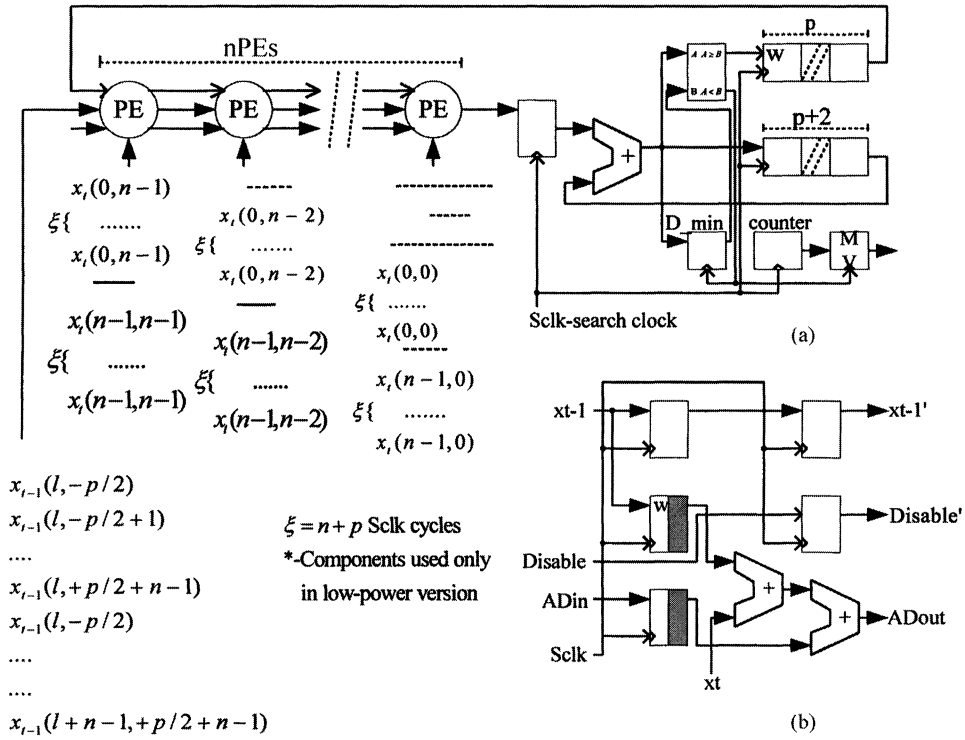

FIGURE 12 Low-power architecture (a) linear array (b) processing element.

code presented in Algorithm 1 [18]. Candidate blocks are placed in raster format at the input of the first PE. For each row I of the reference block, the sums of absolute differences corresponding to all (p+1) candidate blocks in a line are computed in consecutive clock cycles, 2 × n clock cycles after $x_{t-1}(l+I,[-p/2])$ appears on the input, the value of $D_i(l,[-p/2])$ is provided by the last PE to one of the final adder inputs. This adder sums $D_i(l,[-p/2])$ with $D^{i-1}(l,[-p/2])$, provided by the output shift register. The value of the sum is then compared with the minimum distortion value found for the AAS and the comparison result is stored in the blocking register. At the same time, the updated value of D^i is stored in the output shift register. This processing is repeated in the next p clock cycles for the remaining p candidate blocks in line l. Every time a pixel of the first column of a candidate block appears in the array input, the blocking shift register provides a disabled signal to eliminate the unnecessary computations. Blocking registers are introduced in each PE to prevent the internal AD and adder circuits from switching when the disable signal is asserted, as depicted in Figure 12(b). The disable signal is pipelined through the array, to match the pipelining of the distortion computation. Few additional registers (marked with '*') are required to implement the part of the algorithm designed to reduce the power consumption. This architecture fully implements the processing presented in Eq. (3) with no restrictions on p and n values.

Processors with linear array architectures require a high working frequency. For the proposed architecture, about $clk_B = (n+p) \times n \times (p+1)$ clock cycles are necessary to process a reference block and $clk_I = clk_B \times M$ clock cycles are needed to process an entire image with M blocks. The minimum working frequency for a frame rate F is $f_{min} = clk_B \times M \times F$. Therefore, for CIF ($M_{CIF} = 18 \times 22$) and QCIF($M_{QCIF} = 9 \times 11$) images and (n = 16, p = 31) the minimum working

frequency is $f_{CIF} = 190.6\,MHz$ and $f_{QCIF} = 47.7\,MHz$, for a frame rate of 20 fps.

The minimum working frequency value can be decreased by using multiple linear arrays, in order to process in parallel the distortion for different blocks. For example, if two linear arrays are used, the values of the working frequency referred in the previous paragraph are reduced to half. The control of these two linear arrays in quite independent, assuming that the frame buffer supports two simultaneously accesses to different positions. Another way of decreasing the minimum working frequency is to design low-power 2-D array architectures based on Eq. (3). However, it is more difficult to solve the dependency problem in 2-D structures, because two loops have to be processed in parallel. Consequently, the power consumption reduction is lower [19].

3.2. IDCT

We discuss the design of an IDCT macrocell suited for mobile and highly integrated applications [20]. The Strategy for reducing the chip power was twofold. First, this selected an IDCT algorithm that minimized activity by exploiting the relative occurrence of zero-valued DCT coefficients in compressed video. Previous IDCT implementations have relied on conventional fast IDCT algorithms that perform a constant number of operations per block independent of the data distribution. Typically, DCT blocks of MPEG-compressed video sequences have only five to six nonzero coefficients, mainly located in the low spatial frequency position. Based on the information on the statistical distribution of DCT coefficients, this decided to depart radically from conventional IDCT algorithms that perform a fixed number of operations per block. Given such a input data statistics, the direct application of IDCT equation below will result in a small average number of operations since multiplication and accumulation with a zero-valued X[k] coefficient may constitute a "no operation" (NOP). In result, the data-driven algorithm requires a smaller number of operations per block compared to the conventional Chen algorithm.

$$\text{cf. IDCT Eq. } \left(x[n] = \sum_{k=0}^{7} \frac{c[k]}{2} X[k] \cos \left(\frac{(2n+1)kx}{16} \right),\ c[k] = \frac{1}{\sqrt{2}} \ \textit{if}\ k = 0, 1\ o.w \right) \tag{6}$$

Second, this minimized the energy through aggressive voltage scaling using deep pipelining and appropriate circuit techniques so that the chip could produce 14 M samples/sec (640×480, 30 fps, 4, 2, 0) at 1.3 V in a standard 3.3 V process (VTP = −0.9 V, VTN = 0.7 V) and meet the requirement for MPEG2 *MP@ML* (main level, main profile). Details are as follows. The presence of many zero-valued coefficients must be exploited in order to reduce the switching activity and reap the low power benefits of the selected algorithm. Clock gating in a pipeline can be implemented if each stage used a separate clock net gated by an appropriated qualifying pulse. The qualifying pulse propagates from stage to stage along with the non-zero coefficient enters the pipeline, only the stage that corresponds to the zero is powered down.

But this meets one problem. A clock-gated $t_1 - t_0 > t_{CLK \to Q} + t_{pd} - t_{hold}$ (Fig. 13(a)) pipeline is susceptible to race conditions since the clock nets are not

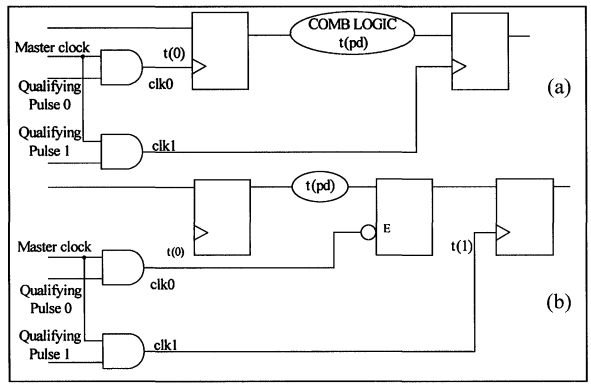

FIGURE 13 Potential race conditions in clock-gated pipelines. (a) Potential race condition. (b) No race condition.

nominally equipotential, if the wrong data will be sampled at the second stage.

In such cases a negative level-sensitive latch was inserted Figure 13(b) to ensure functional correctness with a minimal penalty ($< 2\%$) in power and no effect on the critical path.

4. CONCLUSION

Battery lifetime will dominate system and wireless multimedia system design issues in the next generation. The low-power technique designs these systems requires vertical integration of the design process at all levels, from algorithm development to system architecture to circuit layout. This paper presented possible optimization to reduce the energy consumption for wireless multimedia communication that will be used in next generation wireless multimedia systems. We illustrated examples of design, how we addressed some of the issues in low-power wireless multimedia system.

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