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Efficient Low Power/Low Swing Bus Design Architectures

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Novel low-power circuits based on low swing voltage technique, in the internal nodes of bus architectures, are proposed. Different classes of driver/receiver and repeater circuits are presented. They are implemented on conventional CMOS technology. The proposed technique is based on inserting a variable number of MOSFET transistors in the driver circuits, causing variable low swing voltage levels in the output of the driver circuits. In order to re-pull up the low swing voltage to full swing, innovated high-speed, cross-coupled latch voltage receiver circuits are proposed. In applications having high load capacitance due to long interconnections, novel repeater circuits, based also on low swing voltage technique, are introduced. The difference between the values of threshold voltage of the nMOS transistor and the pMOS transistors is exploited to decrease the power dissipation. The effect of the proposed technique in noise margins is also analysed.

Keywords: Low power design technique; Low swing voltage technique; Low power bus architecture; Long interconnection; Repeater circuit

1. INTRODUCTION

The increasing complexity of VLSI circuits and the growing demand for portable equipment makes power dissipation one of the most important issues in modern VLSI applications [1]. Decreasing the dynamic power dissipation is the most significant part of decreasing the total power dissipation. Bus architectures, clock designs and long interconnections are examples where high capacitance exists in the output. They are often routed over long distance resulting in large load capacitances that must be charged and discharged. Usually up to 50% of the total power dissipation is dissipated due to clock signal, while 40% of power dissipation is caused of long interconnections [2–6].

Several low-power bus architectures have been proposed. They are based on reducing the voltage swing on the internal nodes [7–12]. In [7], non-conventional technology is required and transistors with different resistances are used in order to decrease the swing voltage at the

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output of the driver. In [8], careful design and reference voltage threshold generators are required. The idea to reduce the clock voltage swing was pursued in [9], but it required four clock lines, which caused increasing of the clock interconnection capacitance. BiCMOS technology is used in [10] in order to satisfy high-speed operation and lower power dissipation. Moreover, routing four clock lines is disadvantageous in area, and skew adjustment is difficult to implement. In [11], a method based on diodes using additional clock circuit design without significant decrease in power dissipation is presented. A similar to our proposed technique design based on [10] is proposed in [12], but it requires second external supply voltage of 6V (V_{well}) in order to decrease static DC current dissipation.

As shown from the above techniques, the main disadvantage of the low swing voltage technique is the complex design and the large silicon area. In this paper, we propose three different driver, receiver and repeater circuits based on conventional architecture using simple circuit design. In the proposed technique, variable level of low swing voltage in the output of the driver can be generated. In this way, the proposed technique can be used widely in large number of applications where the low swing level value is dependant on the application. Different values of power savings can be achieved by increasing/decreasing the inserted number of the MOS transistors as will show in next section.

The organization of this paper is as follows: In Section 2, the new low swing bus architectures are presented. Bus architecture evaluation is discussed in Section 3. For long interconnections bus architecture, repeater circuits are proposed in Section 4. The influence of the noise margin in the proposed architecture is shown in Section 5. We conclude in Section 6.

2. BUS ARCHITECTURE

The conventional CMOS bus architecture is shown in Figure 1. It consists of a driver, a delay element (interconnection line), and a receiver. Both the driver and the receiver are designed with conventional CMOS inverters. The input/output voltage level of the driver/receiver ranges between 0 and the power supply voltage (V_{DD}).

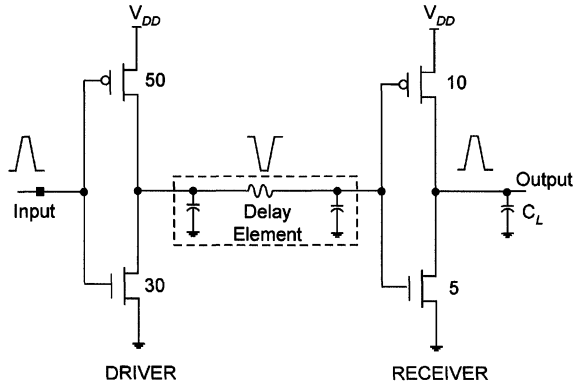

FIGURE 1 Conventional CMOS bus architecture.

In a CMOS circuit the decrease of the supply voltage is the most efficient way to reduce the power dissipation. However, this results also to circuit speed reduction. So, new circuits that combine high-speed operation with low power dissipation should be proposed.

2.1. Low Swing Voltage Driver Architectures

Current state-of-the-art bus architectures are based on reducing the voltage swing in the internal nodes. They require additional circuitry for the bus structures, consisting of a driver and a receiver. Although the techniques achieve high reduction in power dissipation, they also have a number of constraints that reduce their usability. By comparing our proposed technique with existing low swing techniques, improvements in the power saving and in decreasing in the delay time are shown.

Three different classes of proposed driver circuits, achieving reductions in output swing voltage levels are shown in Figures 2a, b, Figures 4a, b, Figures 6a, b. The M1 nMOS transistor (Fig. 2), which is inserted between the pMOS and nMOS transistors of a simple inverter, is used to reduce the output voltage swing. Applying a

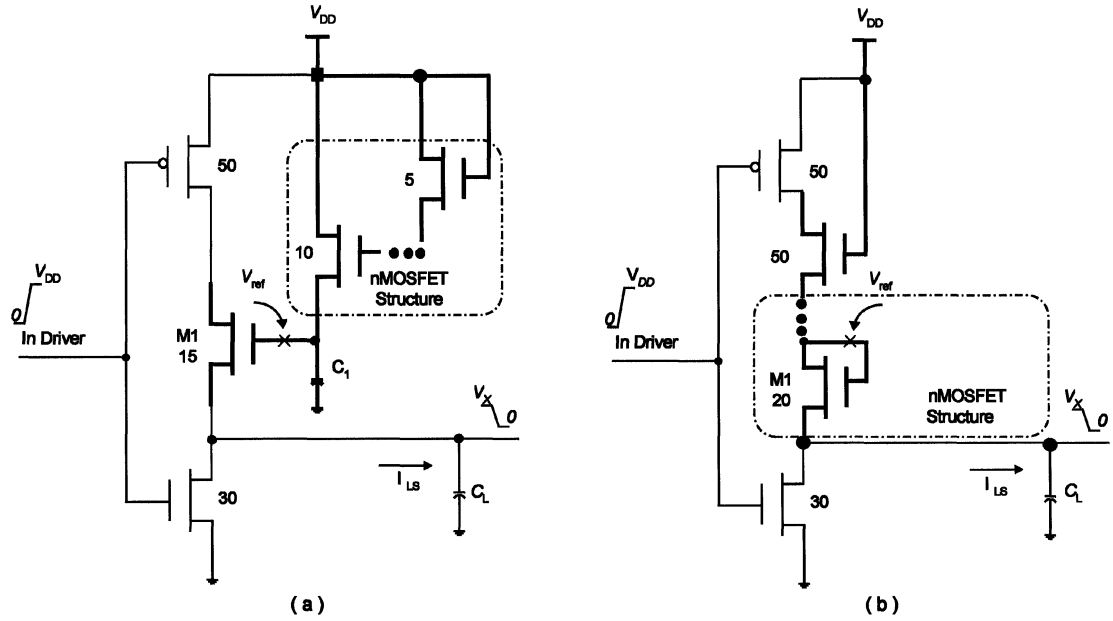

FIGURE 2 Up-Low swing voltage Driver circuits (ULD).

reference voltage V_{ref}, on its gate, the voltage on its source and therefore on the output node of the driver cannot exceed the voltage value $V_{ref} - V_{TH}$, where V_{TH} is the threshold voltage of the M1 transistor [13, 14].

A simple method is used for the derivation of the V_{ref}. This is accomplished by a structure of MOS transistors. In this method, a parallel or serial structure of MOSFET transistors is used. As the gate of each MOSFET transistor (in the MOSFET structure) is connected on the source/drain of the previous one, the voltage value on the source node of the last transistor is:

$$V_{ref} = V_{DD} - nV_{TH}, \quad (1)$$

where n is the number of the MOSFET transistors used in the structure. It is clear that with this driver design, the number of the inserted MOSFET transistors easily controls the output swing-voltage and therefore the saving power dissipation.

As shown in Figures 2a, 4a because of the gate-to-source and gate-to-drain capacitance of the transistor, as the voltage on the source and drain nodes of the M1 transistor varies, an amount of charge is trapped on these gates. This causes an increase in the gate voltage, which destroys the operation of the circuit. In order V_{ref} to remain in the proper value, the C_1 capacitor with a value at least five times the value of the source and drain parasitic capacitance, is inserted. This capacitance can be easily produced using CMOS technology (gate capacitance of a transistor with proper size) [15–17].

The driver circuits in Figures 2a, b belong to the first class called **Up Low Swing Voltage Driver (ULD)**. In this class, the low swing output voltage (V_{LS}) ranges between 0 and V_X, where $V_X = V_{ref} - V_{TN}$ and V_{TN} is the threshold voltage of nMOS transistor. For the same input voltage and load capacitance of each driver, the total power dissipation of the proposed driver is compared with the power dissipation of the conventional driver as with drivers proposed in [18 (Fig. 2)] [10] and [12 (Fig. 3)]. It shows clearly a distinct improvement of the proposed two driver circuits over the other low swing driver circuits. Simulation results are given using only *one* nMOS transistor in the nMOS structure. It should be emphasised here that inserting second or more

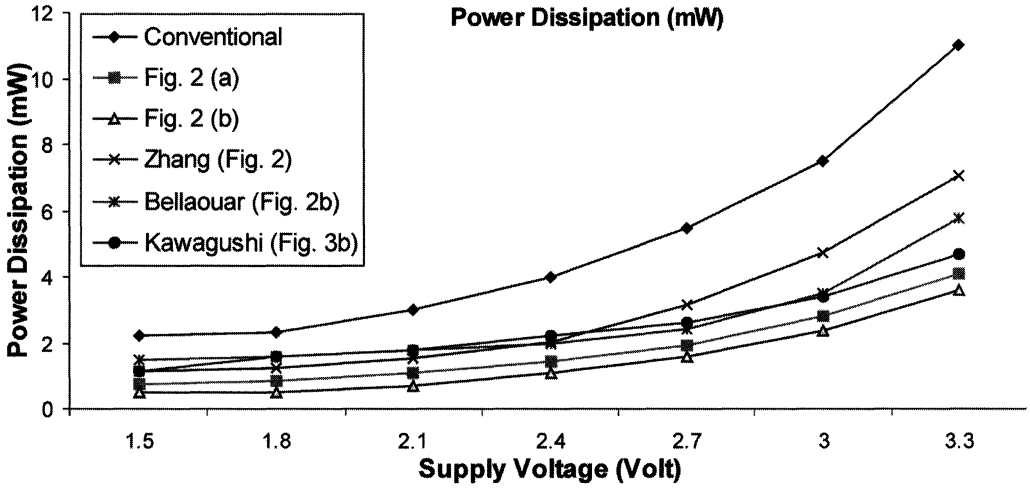

FIGURE 3 **ULD** power dissipation.

nMOS transistors in the MOSFET structure increase the power savings, as will be shown later.

The second class of the low-swing voltage driver is called **D**own **L**ow swing voltage **D**river (**DLD**). It is shown in Figures 4a, b. It is the inverse form of the first class, replacing the nMOS transistors in the case of (**ULD**) by pMOS transistors. In this class, the low swing output voltage (V_{LS}) ranges between V_Y and V_{DD}, where $V_Y = V_{ref} + V_{TP}$, $V_{ref} = n\,V_{TP}$, and V_{TP} is the threshold voltage of pMOS transistor.

The choice between **ULD** and **DLD** depends on the absolute value of the n/pMOS transistor threshold voltages [19]. According to our knowledge no other driver's circuits are proposed in this class. We have compared the proposed driver circuits with the conventional CMOS driver using only one pMOS transistors in the pMOSFET structure (Fig. 5).

The driver circuits in Figures 6a, b belong to the third class called **U**p-**D**own **L**ow swing voltage **D**river (**UDLD**). It is a combination of both previous designs. In this case, the V_{LS} swing output voltage ranges between V_X for low input and V_Y for high input. The differences in the threshold voltages between the inserted (n/pMOS) transistors cause differences in the range of low swing at the output voltage of the driver circuit.

For different values of supply voltage and load capacitance, Figure 7 shows comparison results of the proposed technique with other techniques proposed in [18 (Fig. 5a)].

It is obvious from the above proposed driver designs that the output voltage swing and therefore the power savings is easily controlled by two factors: (1) the value of the threshold voltage of the inserted n/pMOS transistor and (2) the number of the n/pMOS transistors in the MOSFET structure.

2.2. Pull-up Receiver Circuits

When the conventional CMOS inverter is used to convert a low-swing signal to a full-swing signal, the standby power can be important [7]. Symmetric structures of the proposed receiver circuit offer a solution to the problem of standby power dissipation.

Special receiver circuits are required to pull-up the low swing output voltage of the driver circuits to the conventional full swing (range between 0 and V_{DD}). Different receiver circuits are proposed in different published papers based on different methods [7, 20, 10, 12, 18]. In case of the receiver circuits, the main problems are the large silicon area used and the increase of the delay time

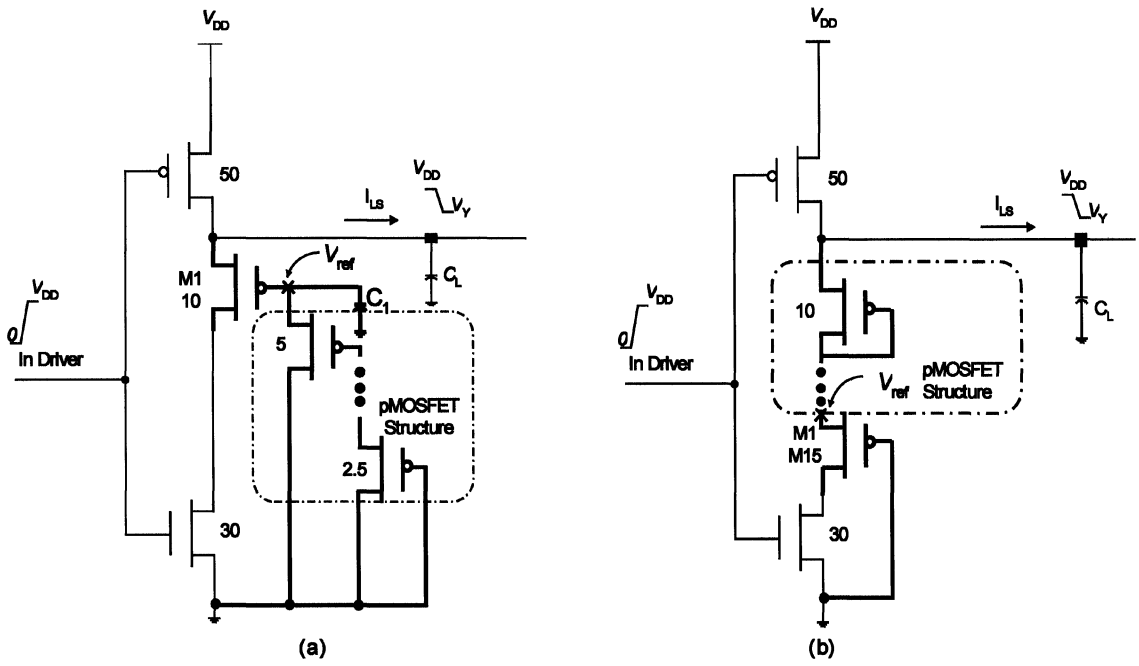

FIGURE 4 Down Low swing voltage Driver circuits (DLD).

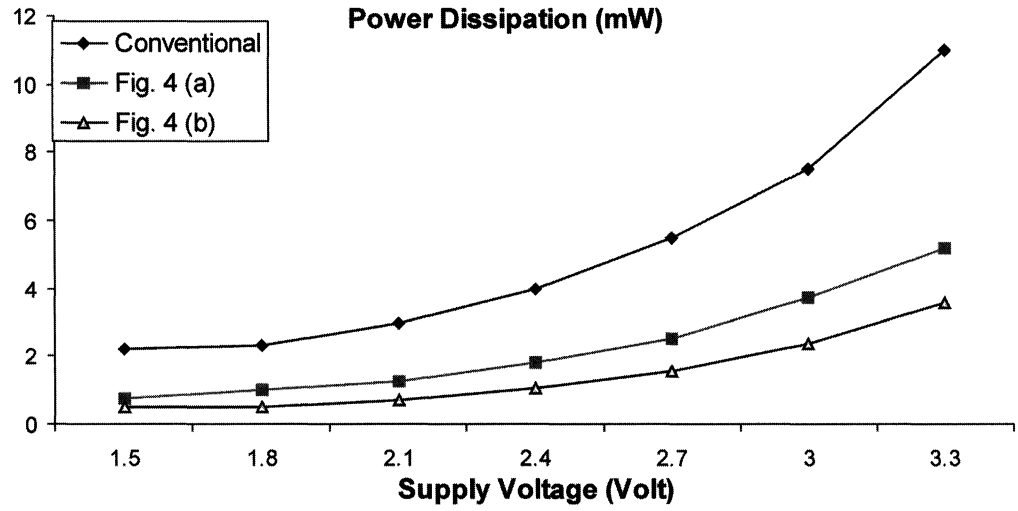

FIGURE 5 DLD power dissipation.

compared to the conventional CMOS receiver. So special attention must be taken during the design of receiver circuits. In our case, we are interested in designing receiver circuits based on conventional CMOS technology, using simple circuit design with least silicon area and delay time.

Because both power dissipation and the propagation delay time are the most important factors of

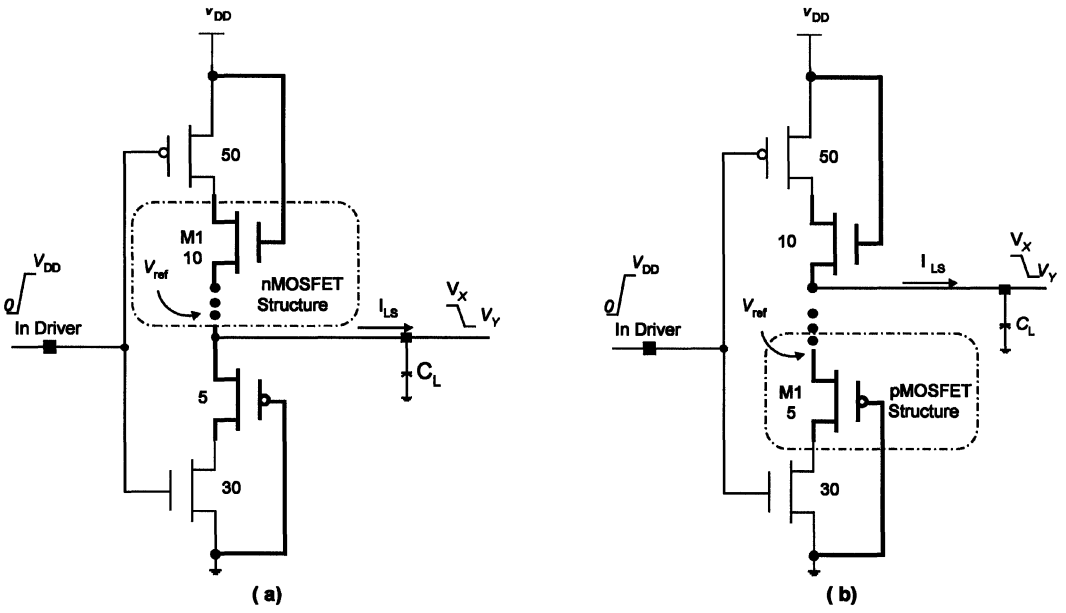

FIGURE 6 Up Down Low swing Drivers (UDLD).

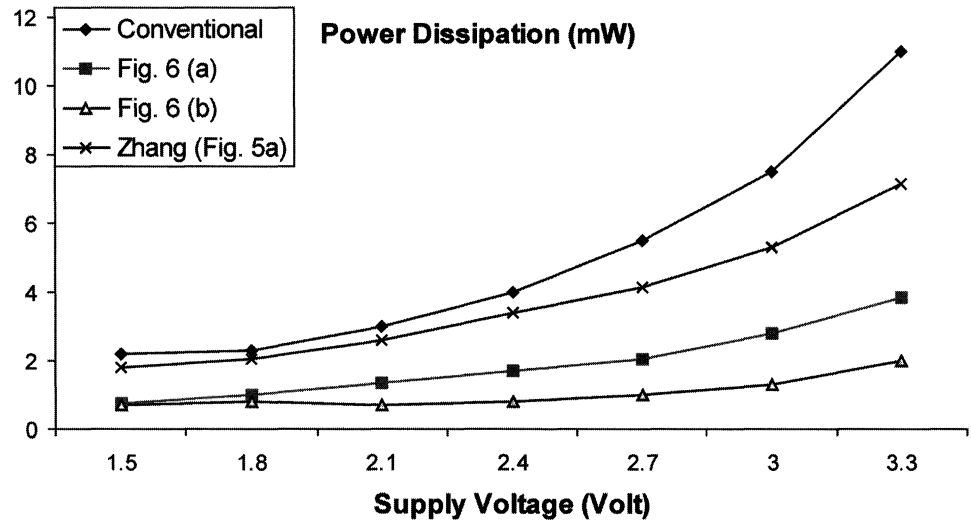

FIGURE 7 UDLD power dissipation.

the receiver circuits, we will use in the following comparisons the normalized power delay product for simplicity. For each class of the proposed driver circuit, an appropriate corresponding receiver circuit is proposed.

The Up-Full swing Receiver circuit (UFR) is shown Figure 8a. It based on voltage sense transistor circuit. The operation of the proposed receiver circuit is as follows: As the receiver input (InReceiver) is connected to the driver output (V_{LS}), the receiver input voltage swings between the values 0 and ($V_{DD} - n V_{TN}$). When $V_X = V_{DD} - n V_{TN}$, transistor M2 turns on, discharging the receiver output node to the ground. Thus, M3

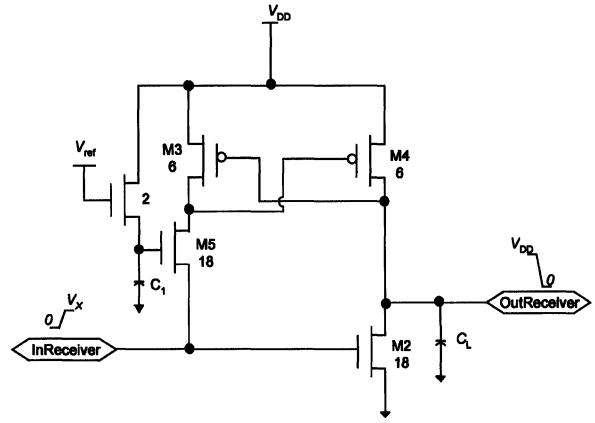

FIGURE 8a Up Full swing voltage Receiver (**UFR**).

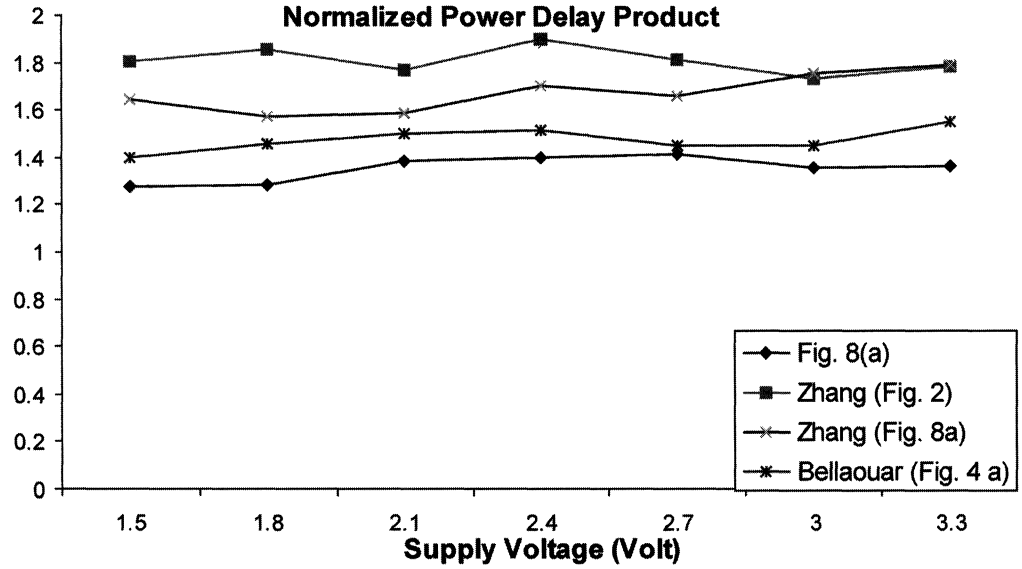

FIGURE 8b **UFR** normalized power delay product.

turns on charging to V_{DD} the gate node of M4, which turns off. At this time, for the proper operation of the circuit, transistor M5 must be off. When the receiver input (V_{LS}) is 0, transistor M2 turns off while transistor M5 turns on, discharging the gate of transistor M4 to 0 V. Thus, M4 turns on, charging the output load to V_{DD} and ensuring a full swing operation.

Normalized power delay product of the proposed receiver circuit (Fig. 8a) and other correspondent receivers proposed in previous published papers [18 (Figs. 2, 8a)] [10 (Fig. 4a)] are compared to the conventional receiver (CMOS Inverter). The simulation results are obtained using the same low swing input voltage and output load capacitance, as shown in Figure 8b.

The same logic of the previous receiver circuits can be implemented in order to cooperate with the **D**own **L**ow swing voltage **D**river circuit (**DLD**). The proposed **D**own **F**ull swing voltage **R**eceiver (**DFR**) is shown in Figure 9a. The logic operation of this receiver is exactly the inversed of the (**UFR**).

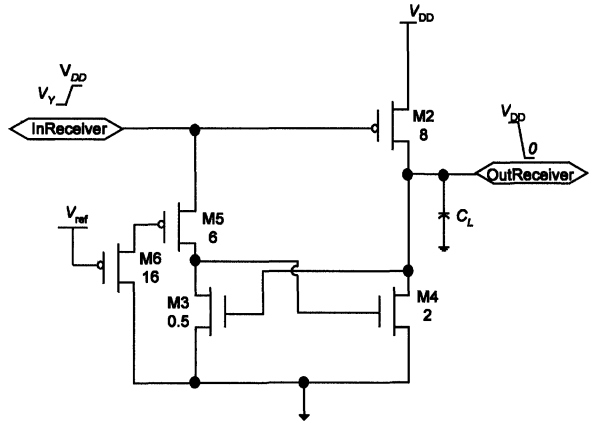

FIGURE 9a Down Full swing Receiver (DFR).

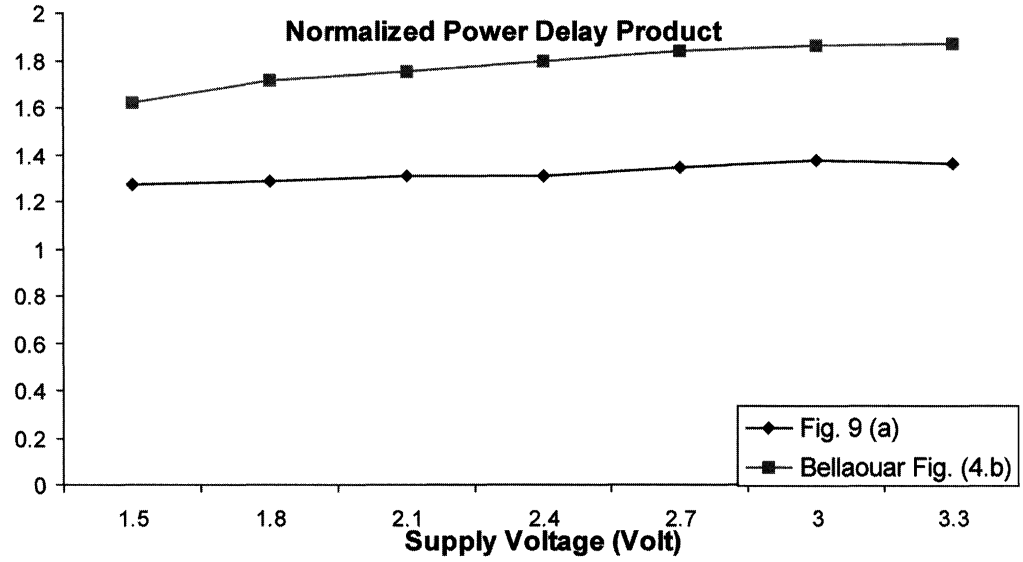

FIGURE 9b **DFR** normalized power delay product.

As the receiver input (InReceiver) is at V_{LS} voltage, the transistor M2 turns on, charging the receiver output node to V_{DD}. Thus, M3 turns on, discharging the gate node of M4 to GND, which turns off. In this case M5 turns off. When the receiver input is V_{DD}, the transistor M2 turns off while the transistor M5 turns on, charging the gate of transistor M4 to V_{DD}. Thus, M3 turns off discharging the output load to 0 and ensuring a full swing operation.

Normalized power delay product of the proposed receiver circuit and receiver circuit proposed in [10 (Fig. 4b)] compared to the conventional CMOS inverter for the same input voltage and load capacitance are shown in Figure 9b.

The combination of the receiver circuits described above, results in the **Up-Down Full swing voltage Receiver circuit (UDFR)** as illustrated in Figure 10a. The circuit is symmetric. When the low swing is high, the up half receiver converts

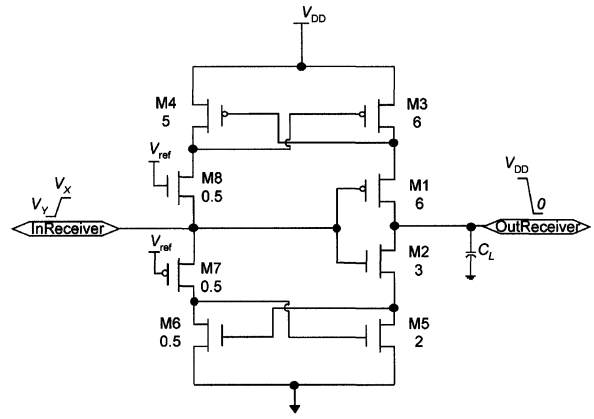

FIGURE 10a Up-Down Full swing voltage Receiver (UDFR).

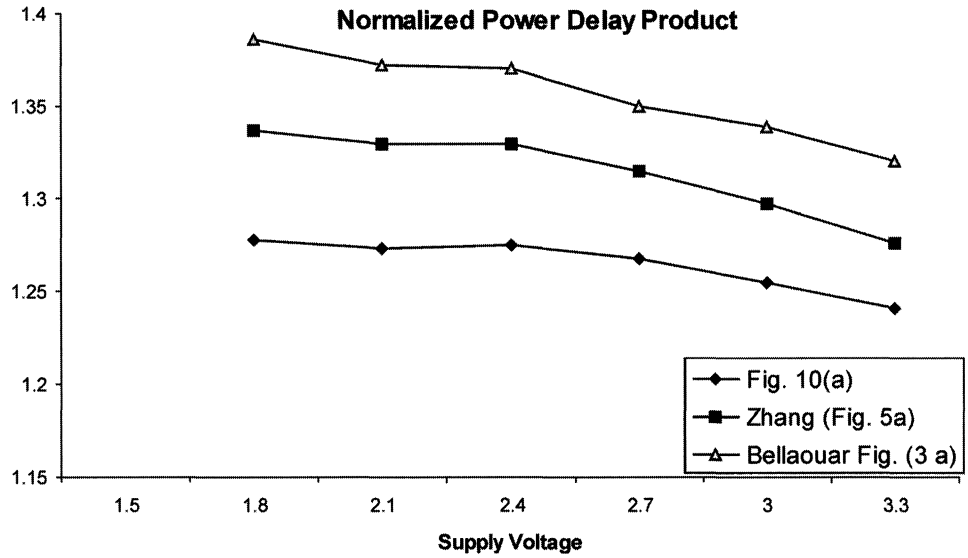

FIGURE 10b UDFR normalized power delay product.

the low swing to V_{DD}, while when the low swing is low, the down half swing receiver converts the low swing to 0 V. The main advantage of the proposed design is the output of the receiver, derived from the CMOS inverter. The output voltage in this case will be 0 volts (low logic) or V_{DD} (high logic).

Normalized power delay product of the proposed receiver circuit and other correspondent receivers proposed in different published papers [18 (Fig. 5a)] [10 (Fig. 3a)], are compared to the conventional receiver as shown in Figure 10b.

3. BUS ARCHITECTURE EVALUATION

In order to show the improvements of the proposed driver and receiver circuits, the proposed architecture is compared with the conventional bus architecture (using two CMOS inverter circuits).

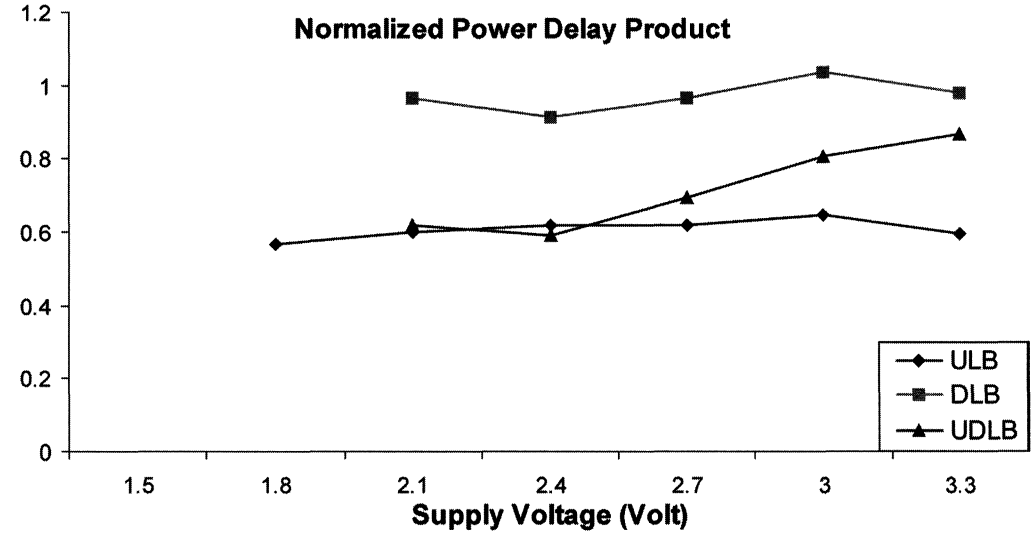

FIGURE 11 Bus architecture normalized power delay product.

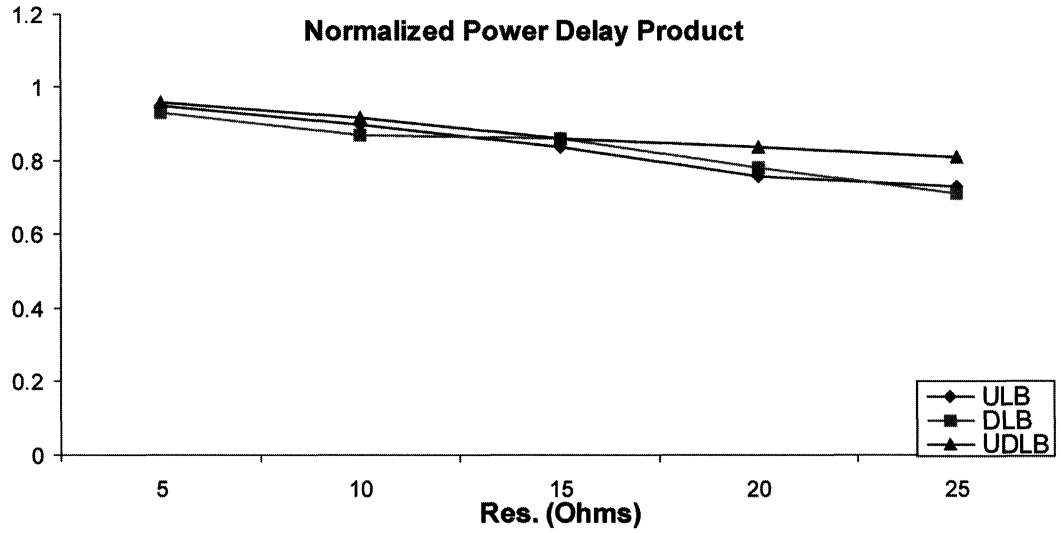

FIGURE 12 Bus architecture normalized power delay product.

Each driver-receiver pair of the three proposed classes forms a bus architecture. The combination of **ULD** and **UFD** forms an **U**p **L**ow swing **B**us architecture (**ULB**), the **DLD** and the **DFD** forms a **D**own **L**ow swing **B**us architecture (**DLB**), and the **UDLD** and the **UDLR** forms an **U**p-**D**own **L**ow swing **B**us architecture (**UDLB**).

Figure 11, shows the normalized power delay product of the three proposed bus architectures compared to the conventional bus architecture under the same conditions of the load capacitance, input voltage and transistor widths.

In Figures 12 and 13 the normalized power delay product for different resistance and capacitance values, in the delay element, are illustrated respectively.

The normalized propagation delay and total power dissipation for the three proposed classes of

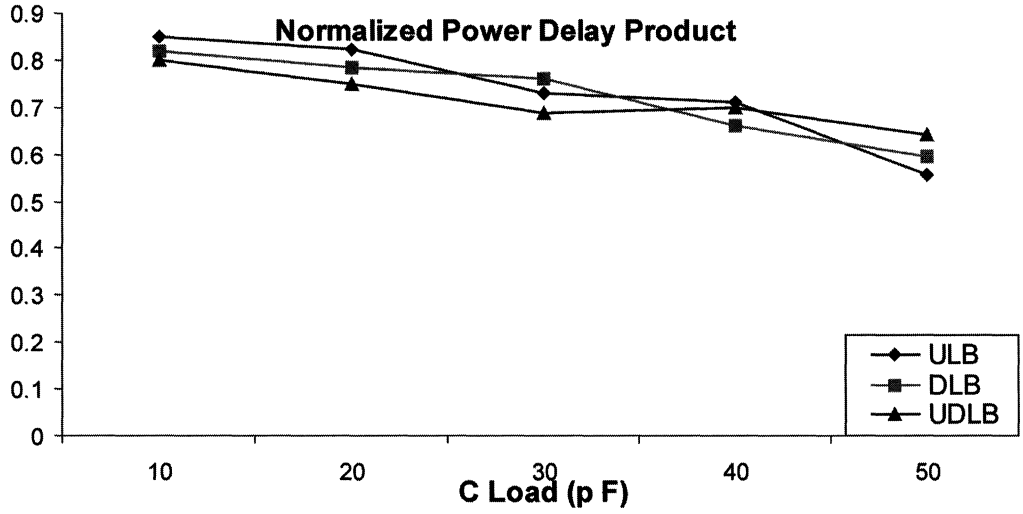

FIGURE 13 Bus architecture normalized power delay product.

bus architecture using different numbers of n, are shown in Table I. An increase of the number of MOS transistors (n) in the inserted structure results in an increase of the delay time and a reduction of the power dissipation. The comparison results are obtained using supply voltage 3.3 V, load capacitance 10 pF and delay line with 0.5 Ω resistance and 0.2 pF capacitors. The widths of transistors are shown in the corresponding figures. The measurements of the power dissipation, was made by the power-meter circuit proposed in [21].

3.1. Dynamic Power Dissipation in the Proposed Bus Achitectures

In CMOS technology, dynamic power dissipation (P_d) occurs when current flows from the power supply voltage (V_{DD}) to the output load, and is calculated by multiplying the total load capacitance (C_L), the operation frequency (f_c) and the square of the supply voltage (V^2_{DD}):

$$P_d = f_c C_L (V_{DD} * V_{DD}) \tag{2}$$

Dynamic power dissipation in the proposed architecture can be calculated by

$$P_d = f_c C_L (V_{DD} * V_{LS}) \tag{3}$$

where V_{LS} is the low swing voltage in the output of the driver. Compared to the full voltage-swing case, a reduction in power dissipation

$$(V_{LS} / V_{DD}) * 100\% \tag{4}$$

is achieved. The above equation indicates the significant savings in the dynamic power dissipation that can be achieved by reducing the supply voltage (V_{DD}). In the case of the **U**p **L**ow swing voltage **B**us architecture and for the low voltage swing operation, the energy required to charge a capacitive load C_L to the value

$$V_{ref} = V_{DD} - nV_{TN} \tag{5}$$

is:

$$E = V_{DD} \int i \cdot dt = V_{DD} \int_0^{\Delta V} C\, dv$$
$$= C V_{DD} (V_{DD} - (n+1) V_{TN}) \tag{6}$$

TABLE I Normalized propagation delay time

	ULB		DLB		UDLB	
n	Norm. Delay	Norm. Power	Norm. Delay	Norm. Power	Norm. Delay	Norm. Power
1	0.82	0.88	0.84	0.85	0.86	0.87
2	0.84	0.70	0.88	0.68	0.90	0.70
3	1.55	0.44	1.73	0.52	1.78	0.66

The power savings, compared to the power dissipation, E_{tot} of the full swing operation, is given by the power saving factor k,

$$k = \left(1 - \frac{E}{E_{tot}}\right) 100\% = \frac{(n+1)\,V_{TN}}{V_{DD}} 100\%. \tag{7}$$

The dynamic power dissipation of the two other bus classes can be calculated using similar equations.

4. REPEATER CIRCUITS

The delay of a long line, with distributed resistive and capacitive components, grows as the square of its length [22–24]. To avoid this dependence, a common solution is to separate regularly the interconnection line in equal length segments, which are driven by repeaters [25, 8, 2, 3].

We propose three different classes of repeater circuits. They are appropriate to the three classes of the driver-receiver circuits. For **ULB**, the **U**p **L**ow swing **R**epeater (**ULR**) (Fig. 14a), for **DLB**, the **D**own **L**ow swing **R**epeater (**DLR**) (Fig. 14b) and for **UDLB**, the **U**p-**D**own **L**ow swing **R**epeater (**UDLR**) (Fig. 14c) are proposed.

The operation of the repeater circuits is as follows (*e.g.* Fig. 14a): The repeater circuit has input the driver's output which is ranging between values 0 and $V_{ref} - V_{TN}$ (V_X). When the input value is 0, the pMOS transistor turns off and the nMOS transistor turns off. The voltage value in the source of transistor M1 can not exceed the value of ($V_{ref} - V_{TN}$), which is the same value of the output voltage of the repeater. When the input voltage is V_{LS} ($V_{ref} - V_{TN}$), the nMOS transistor turns off and the pMOS transistor turns on. Therefore, the output of the repeater is exactly 0, which satisfies the logic operation of the circuit. The inverse logic operation is satisfied for the repeater in 14b.

In the third class 14c, the input of the **UDLR** ranges between values V_Y ($V_{ref} - V_{TN}$) and V_X. When the input voltage value is V_X, the pMOS transistor (M1) turns off and the nMOS transistor (M2) turns on (its source voltage value is V_{TP}). The voltage value in the source of transistor M1 can not exceed the value of ($V_{DD} - V_{TN}$), which is the value of the output voltage of the driver. When the input voltage is V_X, transistor M2 turns off and transistor M1 turns on (its source voltage value is V_{TN}). The output of the repeater in this case can not exceed the voltage value V_{TP}.

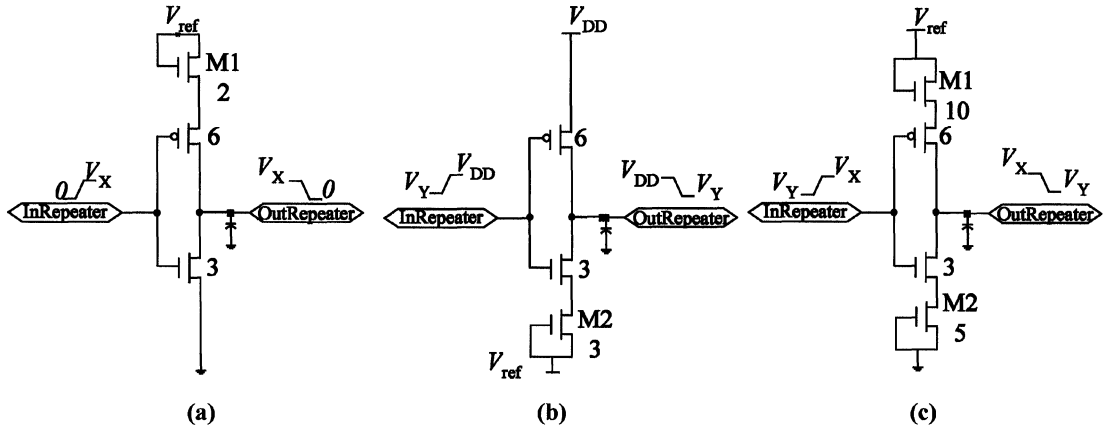

FIGURE 14 Proposed repeater circuits.

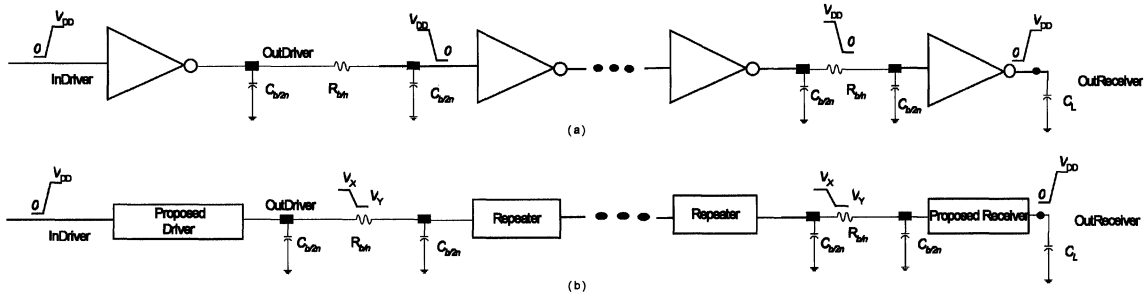

FIGURE 15 Bus architecture with repeaters.

TABLE II Measurements by using different number of repeaters (k)

	Normalized propagation delay			Normalized power dissipation		
k	**ULB**	**DLB**	**UDLB**	**ULB**	**DLB**	**UDLB**
5	0.86	0.89	0.92	0.85	0.88	0.87
10	0.80	0.85	0.90	0.83	0.84	0.83
15	0.74	0.80	0.85	0.80	0.79	0.78
20	0.68	0.73	0.78	0.76	0.77	0.74

TABLE III Measurements by using different number of inserted transistors (n)

	Normalized propagation delay			Normalized power dissipation		
n	**ULB**	**DLB**	**ULB**	**DLB**	**ULB**	**DLB**
1	0.91	0.92	0.90	0.85	0.84	0.86
2	0.93	0.95	0.94	0.72	0.69	0.61
3	0.97	1.06	0.98	0.64	0.66	0.58

TABLE IV SPICE Parameters

Parameter	Value
Gate Length	0.65 μm
Gate Oxide Thickness	110 Å
N-Channel: Vth	0.65 V
P-Channel: Vth	−0.92 V
N-Channel: Kp	1.9647E-04
P-Channel: Kp	4.8740E-05

Because the input and the output of the repeater circuit range in low swing voltage level, the power dissipation in this case will be calculated from the following equation:

$$P_{Rep} = f_c C_L (V_{LS} * V_{LS}) \tag{8}$$

So the saving power in k repeater circuits comparing with the same number of conventional CMOS repeaters (single inverters), is

$$\left(1 - \frac{V^2_{LS}}{V^2_{DD}}\right) \times k \times 100\% \tag{9}$$

In order to evaluate the repeater's delay time and power dissipation, we applied a different number of repeaters for each of the proposed bus classes. The long interconnection line (Fig. 1) was cut to symmetrical segments as shown in Figure 15. For the measurements, 10 pF capacitor values and 0.5 Ω resistance values were used.

The normalized propagation delay and normalized power dissipation measurements for the three bus architectures with different number of repeaters (k) are shown in Table II.

The measurements are obtained using only one MOS transistor in each inserted structure. In [23]

TABLE V Noise margin measurements

	$V_{IH\ min}$	$V_{IL\ max}$	$V_{OH\ min}$	$V_{OL\ max}$	NM_L	NM_H
Conventional design	0.262	1.63	0.61	3.3	0.35	1.65
Proposed design	0.258	1.56	0.58	2.7	0.30	1.07

an analysis for the optimum number of repeaters is given. From Table II, it is obvious that an increase in the number of repeaters (k) results in a decrease in the normalized delay time, as it is expected.

The normalized propagation delay and normalized power dissipation measurements for the three bus architectures with different number of MOS transistors (n) are shown in Table III.

For all the above measurements the SPICE parameters shown in Table IV, are used.

5. NOISE MARGIN

Noise margin is an important factor in applications with low swing voltage. Maximum noise margin can be defined as the noise margin that can be tolerated in a circuit without producing a logic error. The worst case of noise margin in either low or high noise margin is 0.1 V_{DD} [26]. Measurements show that in the proposed bus architectures, the lowest voltage of the noise margin is 0.45 V_{DD}, (in case of **UDLB**). Noise margin measurements taken for **UDLB**, are shown in Table V. In the proposed designs and in order to increase the value of the noise margin, we proposed also the repeater circuits that can also keep the values of noise margin in high values.

6. CONCLUTIONS

In this paper, three low power bus architectures are presented. They are based on the voltage swing reduction technique. Simple design principles and conventional CMOS technology are strictly employed. Symmetrical driver/receiver circuits for different low swing voltage are proposed. Using a structure of nMOS/pMOS transistors, parametrical reduction in voltage swing can be achieved. High power dissipation savings are obtained, while the trade-off between the power dissipation and the propagation delay was also examined. In order to decrease the delay time in long interconnections, repeater circuits compatible to each type of proposed driver/receiver circuits are also proposed, resulting in the decrease of the delay time as well as the increase of the value of the noise margin.

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