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Effect of Reverse Body Bias on Current Testing of 0.18μm Gates

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Systematic investigations on defect-free I_{DDQ} in deep submicron CMOS with reverse body bias were performed by SPICE simulation towards an attempt to improve resolution of I_{DDQ} measurement. Effects of reverse body bias on off-state leakage of scaled CMOS devices and I_{DDQ} of typical CMOS circuit cells were investigated. It was found that reverse body bias can effectively reduce defect-free I_{DDQ} of typical 0.18 μm technology devices and logic gates while the faulty current is not as much reduced. The reduction in defect-free I_{DDQ} was enhanced as the device temperature went up and diminishes as the temperature went down. Further investigation showed that reverse body bias also makes the defect-free I_{DDQ} less sensitive to the input state; therefore, a single I_{DDQ} current threshold might still be used for I_{DDQ} testing of 0.18 μm CMOS circuits. It was found that there might exist an optimal reverse body bias that minimized the defect-free I_{DDQ} current. The optimal reverse bias value decreases as the temperature went down and might vary from circuit to circuit, process to process, and technology generation to generation.

Keywords: I_{DDQ}; Current testing; CMOS; Deep submicron; Subthreshold current; Reverse body bias

1. INTRODUCTION

Current testing is a widely accepted defect detection technique for CMOS ICs. It relies on the fact that static CMOS devices have a very low quiescent current, when they are in the off state. This current is elevated in the presence of manufacturing defects. Figure 1 shows a typical distribution of the good and leaky (faulty) die. I_g and I_f are the means of each distribution. It is customary to use a single current threshold, I_{th}, such that $I_g < I_{th} < I_f$, as a pass/fail indication. Outliners from the good distribution with current higher than I_{th} are rejected good die. Similarly, faulty die with currents lower than I_{th} pass the test. Thus the determination of the value of I_{th} is critical to the yield. As CMOS

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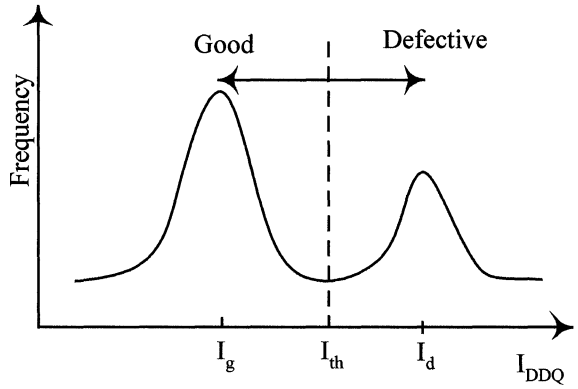

FIGURE 1 Generic distribution of I_{DDQ} for good and faulty circuits.

technology moves toward the deep submicron feature sizes, the off state current increases dramatically [11, 18, 24]. Meanwhile, ICs are becoming denser and larger which further increases their quiescent currents. On the other hand, for deep submicron technology circuits, the voltage has been reduced while the resistance remains relatively constant [4]. Thus the quiescent current of defective ICs is expected to decrease and that makes it very difficult to separate good and defective products based upon I_{DDQ} values.

For I_{DDQ} testing to continue to be effective in future technologies, techniques to control the defect free quiescent current must be developed [21, 26, 31]. Investigation of the nature and causes of I_{DDQ} elevation in deep submicron (DSM) devices are necessary to develop a solution for this problem as well as for reducing standby power [2, 26, 5, 12]. Some potential solutions have been suggested. These solutions include among others: (1) cooling down device during testing [7], (2) partitioning network and performing I_{DDQ} test on individual segment of design [1], (3) using state dependent I_{DDQ} instead of a single current threshold [8, 17], (4) architectural changes such as using dual threshold devices [28], (5) reverse biasing the substrate during testing [21], and (6) use of alternative technologies; for example, lightly doped drain (LDD) and silicon on insulator (SOI) [28].

Of these various proposals, multiple-threshold and substrate back biasing have been demonstrated to be effective in reducing standby power in logic circuits and DRAMs [6, 30, 20, 19]. These techniques rely on controlling the threshold voltage of scaled down technology. Because of their success in reducing standby power, it is encouraging to investigate their use for I_{DDQ} testing in very deep submicron circuits.

In this paper, we examine the effect of body biasing on the effectiveness of I_{DDQ} testing in DSM technology. We have used extensive SPICE simulation to characterize the off current in 0.18 μm technology MOS devices and the quiescent current of typical CMOS circuit cells such as an inverter, a NAND gate, and a NOR gate. Results on reduction in defect-free I_{DDQ} and input state dependence are reported and discussed.

The rest of this paper is organized as follows: In Sections 2 and 3 we list the causes of I_{DDQ} elevation and describe substrate biasing. The effect of body bias on off-state current of MOS devices and I_{DDQ} of elementary logic gates is presented in Section 4. The effectiveness of body biasing in current testing is evaluated in Section 5. The effect of the temperature on the body bias solution is reported in Section 6. Finally, a summary and conclusions are presented.

2. OFF-STATE LEAKAGE CURRENT

The off-state current in devices and quiescent current in logic gates consist of various components that are due to several physical phenomena. Of these components, the most relevant are illustrated in Figure 2: (1) the channel subthreshold current, I_S, increases due to the reduction of the threshold voltage since $V_{th} \propto L^{0.2}$ [18], (2) the second component is characterized as the drain induced body lowering effect (DIBL), which is the precursor to punch-through current. It flows through the channel unregulated by the gate voltage V_g; and (3) the current due to band-to-band tunneling (BTBT).

The first two components are referred to as the short channel effect and the third component is

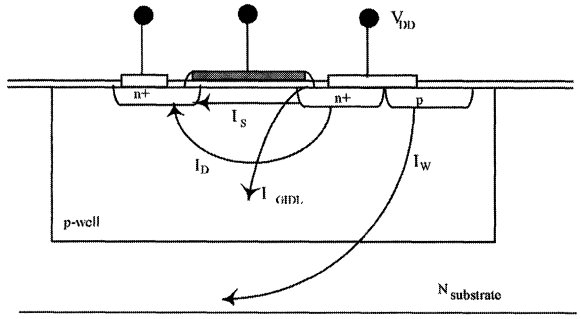

FIGURE 2 Components of off-state current of an NMOS transistor.

due to various phenomena: the gate-induced drain leakage (GIDL) I_{GIDL}, and the reverse bias of the drain-substrate junction (I_D) and the well-substrate junction (I_W).

Depending on the value of the gate-source voltage, V_{gs}, some components are more dominant than others [27, 3]. In the off state, $V_{gs} < 0$ or is slightly negative (positive) for NMOS (PMOS) transistors. In this region, the most important components are I_S and I_D. The latter component is function of the geometry of the device, as well as the voltage across this device, V_{ds}. However, it is projected to be more dominant when the feature size reaches 0.03 μm [18, 3]. As V_{gs} is further reverse biased, the effect of GIDL, which also lowers V_{th}, starts to become an important component. For the value of V_{gs} of interest to our study ($-0.5\,V \leq V_{gs} \leq 0\,V$ for NMOS), the most dominant components are then I_S through the channel and I_W through the bulk.

For logic gates, which consist of several combinations of transistors in series and parallel, the quiescent current depends on the state of the gate [15, 5, 16, 9]. The logic state is defined as the input combination of the gate. Only I_W is state independent.

In the subthreshold region, the current I_S is given by

$$I_S \propto \mu_0 C_{ox} \left(\frac{W}{L}\right) V_T^2 \exp\left(\left(\frac{V_{gs} - V_{th}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right)\right),$$

where $V_T = q/kT$, $n = 1 + C_D/C_{ox}$ and C_D is the depletion channel region per unit area [9].

3. SUBSTRATE BIASING

On the average, half of the devices are turned off when digital CMOS circuits are in standby mode. That is, for these devices $V_{gs} = 0$ or is slightly negative (positive) for NMOS (PMOS) devices. For NMOS transistors the bias is such that $-0.5\,V \leq V_{gs} \leq 0\,V$. This value depends on the operating position of the transistor in the circuit; that is, it depends on the state of the circuit. For this range of V_{gs}, the off-state leakage current is due mostly to thermal conduction. With scaling down the device dimensions and the voltages (V_{dd} and V_T), the gate delays and the off-state current are increased. To manage this rise in the current, it is possible to bias the substrate. Three approaches to substrate bias are possible: (1) apply the bias only when the circuit is in standby mode to reduce the standby power, (2) tie the substrate to the gate for all devices to reduce gate delays, and (3) apply forward bias during normal mode of operation and back-bias in the standby mode (substrate-over-bias). The advantage of substrate over bias is to reduce gate delays during active mode as well as reduce standby power [20]. However, this technique increases the off-state current when the circuit is in active mode. The substrate-gate tie is more effective in this situation. It is possible, of course, to use both methods. Substrate-gate tie proved to be successful in dynamic logic while substrate-back-biasing is effective for static logic [20]. In this paper, we concentrate on reverse body bias (RBB).

4. DEFECT-FREE I_{DDQ} UNDER RBB

It is important to fully understand the effect of the reverse body bias (RBB) lowering the defect-free I_{DDQ} for a large circuit. For this we first investigate how RBB affects off-state leakage of MOS transistors and simple CMOS circuit cells.

This was accomplished by extensive SPICE simulations on DSM transistors and simple logic gates, which represent parallel and series configurations of NMOS and PMOS transistors. The cells used were an inverter, a three-input NAND, and a three-input NOR. The body bias is applied through biasing the whole N/P-wells, and the bias values for N-well and P-well were assumed to be the same. This is illustrated in Figure 3. The simulations used BSIM3 MOSFET models in which the parameters are derived from measurements made of actual devices. Device parameters and operating points are listed in Table I. All simulations in this section were carried out at 25°C. Simulations at a high temperature of 150°C and a low temperature of −50°C were also conducted to investigate temperature dependence of defect-free I_{DDQ} with reverse body bias. The results are discussed in Section 6.

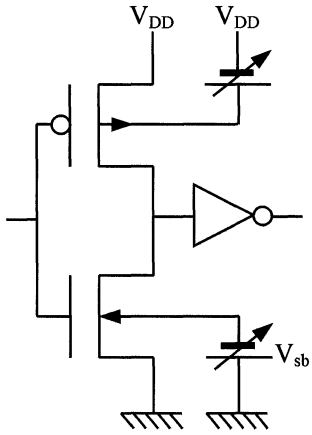

FIGURE 3 Applying reverse body bias to the devices of an inverter.

TABLE I Device parameters used in the experiments

Technology	0.18 μm	0.25 μm	0.35 μm
V_{dd} (V)	1.8	2.5	3.3
V_{tn0} (V)	0.35	0.41	0.61
V_{tp0} (V)	0.42	0.52	0.76
L (μm)	0.18	0.25	0.35
W_n (μm)	0.3	0.3	0.35
W_p (μm)	0.9	0.9	1.0

4.1. MOSFETs Devices

To characterize the RBB dependence of the I_{DDQ}, this current is measured for both the NMOS and PMOS transistors for different technology features as well as for various channel lengths. Figure 4 shows the off-state leakage current as a function of RBB voltage (V_{bs}) for NMOS transistors at room temperature of 25°C. The off-state leakage currents for NMOS transistors are significantly reduced by applying RBB. In particular, we notice that for the finer technology features (1) the leakage current at any value of body bias voltage is higher, and (2) RBB is more effective in lowering the current. The same results are observed for PMOS transistors. The leakage current does not decrease monotonically with reverse body bias and there exists an optimal reverse body bias that minimizes the off-state leakage. After this optimal point, the leakage current mostly increases with RBB. This increase is due to dominance of GIDL, which becomes dominating under a high RBB [2, 27, 3].

Figure 5 shows the off-state leakage current as a function of the RBB for different channel lengths of NMOS and PMOS transistors, respectively. The transistor channel length, Lg, varies from 0.18 μm to 2 μm. As expected, the off-state

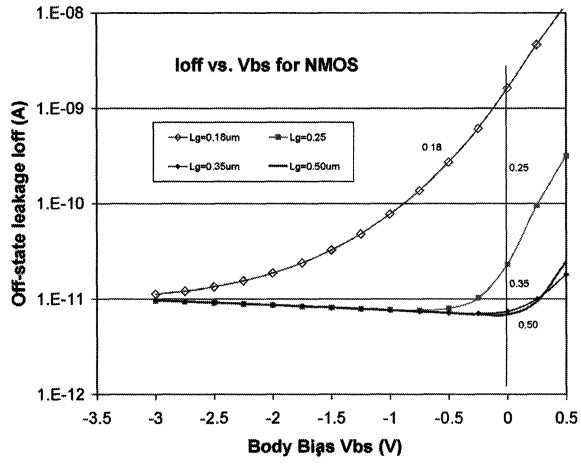

FIGURE 4 RBB effect on the off-state current of various submicron technology NMOS devices.

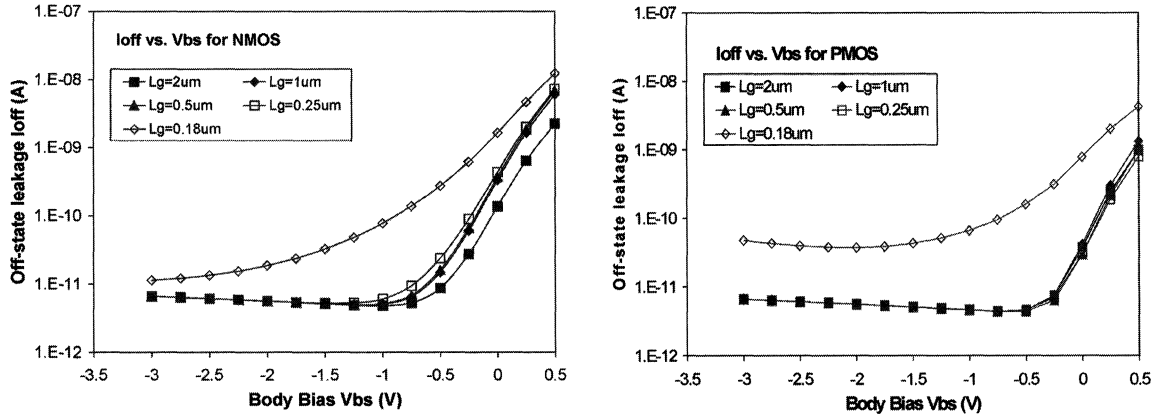

FIGURE 5 RBB effect on off-state current of 0.18 μm NMOS and PMOS devices for various channel lengths.

current without back bias ($V_{bs} = 0$) is lower for a longer channel length. Another finding is that the body effect, or body effect coefficient, tends to become weaker as the channel length decreases. This also reduces the effectiveness of the reverse body bias on I_{DDQ}. However, if we select a body bias at which the I_{DDQ} is the lowest for the shortest channel length, $Lg = 0.18\,\mu m$ ($V_{bs} = -3\,V$), there is a 3-order current reduction, from 10 nA to 0.01 nA. This is roughly the same order of magnitude reduction for longer channels. For these channel lengths, this reduction still stands for $V_{bs} = -1\,V$, whereas for the shortest channel length the reduction is only to 0.1 nA. The selection of the V_{bs} depends on the circuit design and layout.

4.2. State Dependence of Defect-free I_{DDQ} with Reverse Body Bias

To compare the leakage currents in the PMOS and NMOS transistor, we plotted these currents *versus* V_{bs} for channel length 0.18 μm. The curves are normalized to the NMOS current at $V_{bs} = 0$ and shown in Figure 6. It is clear that the leakage in the PMOS transistor is lower than that in the NMOS. This difference is quickly reduced as RBB is applied. The difference in leakage currents by type of transistor is one of the causes that

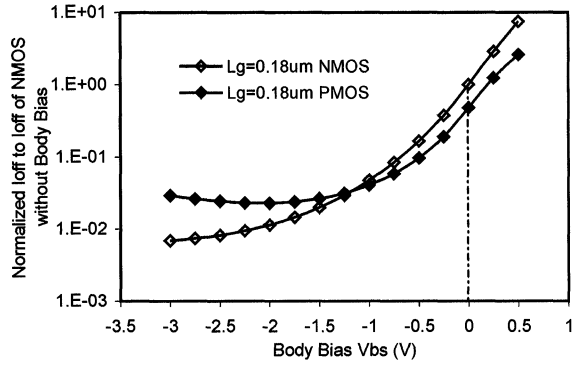

FIGURE 6 Comparing the off-state currents in NMOS and PMOS devices and to RBB.

make the leakage in a logic gate dependent on the state of the gate. For an inverter then we expect that the leakage will be higher when it is in the 0-state than in the 1-state. This is demonstrated in Figure 7 for inverters of features sizes 0.25 μm and 0.18 μm.

It can be clearly seen that the defect-free I_{DDQ} is input-state dependent when no body bias is applied ($V_{bs} = 0$). By applying an optimal reverse body bias, significant reduction in maximum I_{DDQ} current as well as state dependence is observed. The I_{DDQ} state dependence of inverter is mainly due to different type (NMOS or PMOS) of off transistors in different state, that is, in state 0 the NMOS is turned off and in state 1 the PMOS is

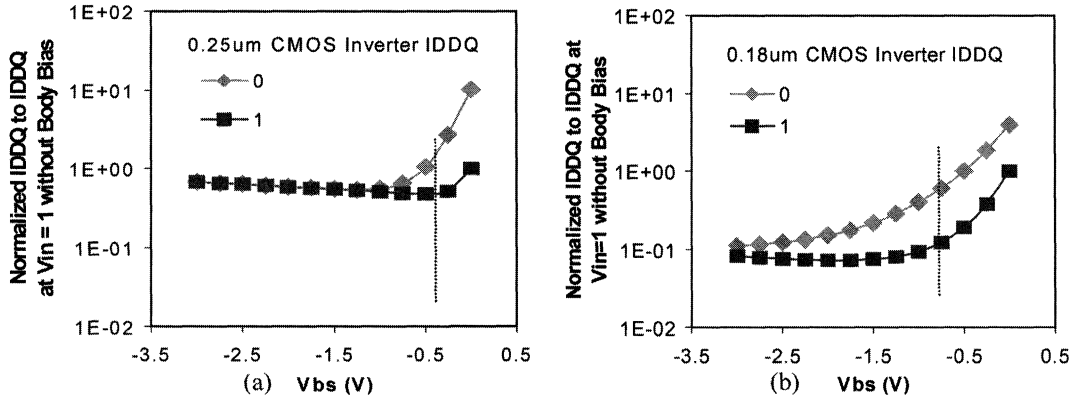

FIGURE 7 Defect-free I_{DDQ} state dependence for inverters of technology features (a) 0.25 μm and (b) 0.18 μm.

turned off. The difference of off-state leakage current between NMOS and PMOS is process dependent. However, when a body bias is applied, the body-to-source/drain diode leakage currents, which are determined by body to source/drain voltages, increase with reverse body bias due to band-to-band tunneling. As the reverse body bias increases, the band-to-band tunneling current may dominate the leakage current. Therefore, the state dependence tends to diminish as the RBB increases (see Fig. 6).

4.3. I_{DDQ} of Typical CMOS Cells with Reverse Body Bias

For NAND and NOR gates, the situations are more complicated. The value of defect-free I_{DDQ} in NAND or NOR gates is determined by both number of transistors turned off and the V_{ds} values of the individual off transistors in the series stack of the logic gate [9, 5]. Note that the subthreshold leakage is dependent of drain-to-source voltage (V_{ds}), *i.e.*, subthreshold leakage increases with V_{ds}. For the NAND gate shown in Figure 8 the state is determined by the inputs (ABC). The highest I_{DDQ} current occurs for the (011) state, because there is only one off NMOS transistor having a $V_{ds} = V_{dd}$. For states 101 and 110, V_{ds} is reduced to $V_{dd} - V_t$. For states 001, 010 and 100, there is more than one off transistor. The lowest leakage current occurs for state 000. This is exactly the state for which the highest leakage current occurs for the NOR gate, while its lowest value is at state (111).

Figures 9a, b shows the three-input NAND and NOR gates defect-free I_{DDQ} at 25°C as a function of reverse body bias for different input states. The I_{DDQ} values are normalized to the I_{DDQ}, without body bias, at state (000) and (111) for the NAND and NOR, respectively. As shown in the figures, the defect-free I_{DDQ} is input-state dependent when no body bias is applied ($V_{bs} = 0$). The worst case I_{DDQ} (with input 011 for NAND and 000 for NOR) can be significantly reduced by more than one order in magnitude by applying reverse body bias. The optimal reverse body bias is -2.2 V for NAND gates, and -3.0 V NOR gate. However, these values are not the most optimal for all the states. Figure 9c shows the worst state defect-free I_{DDQ} of the two gates as a function of reverse body bias. To reduce the I_{DDQ} state dependency, we selected the bias -2.25 V and compared its effect to the case of no bias. The plots are shown in Figure 10. The reduction in state dependence with reverse body bias for NAND gate is again due to body-to-source/drain diode currents of the off transistors, especially the band-to-band tunneling current that increases with reverse body bias and may become dominating at high reverse body bias. Thus RBB makes I_{DDQ} current less sensitive to state changes on the NAND gate. Similar analyses apply to the NOR gate.

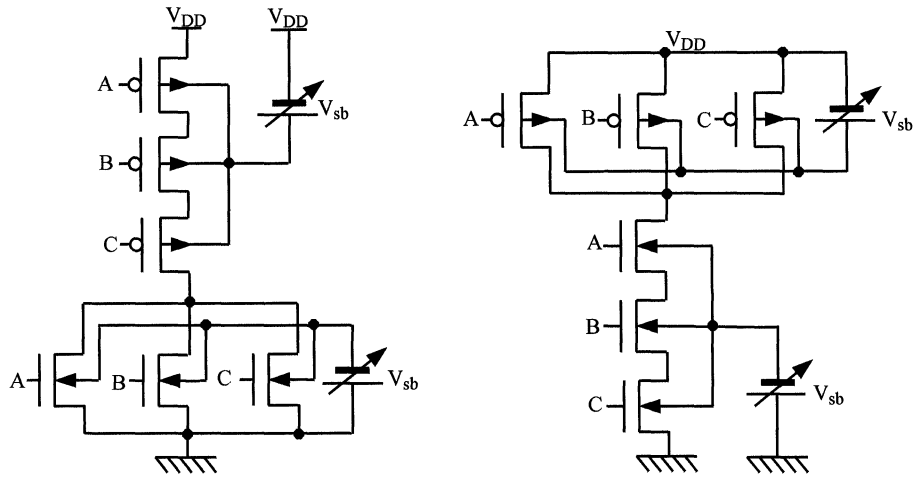

FIGURE 8 Three-input NOR and three-input NAND used in the experiment.

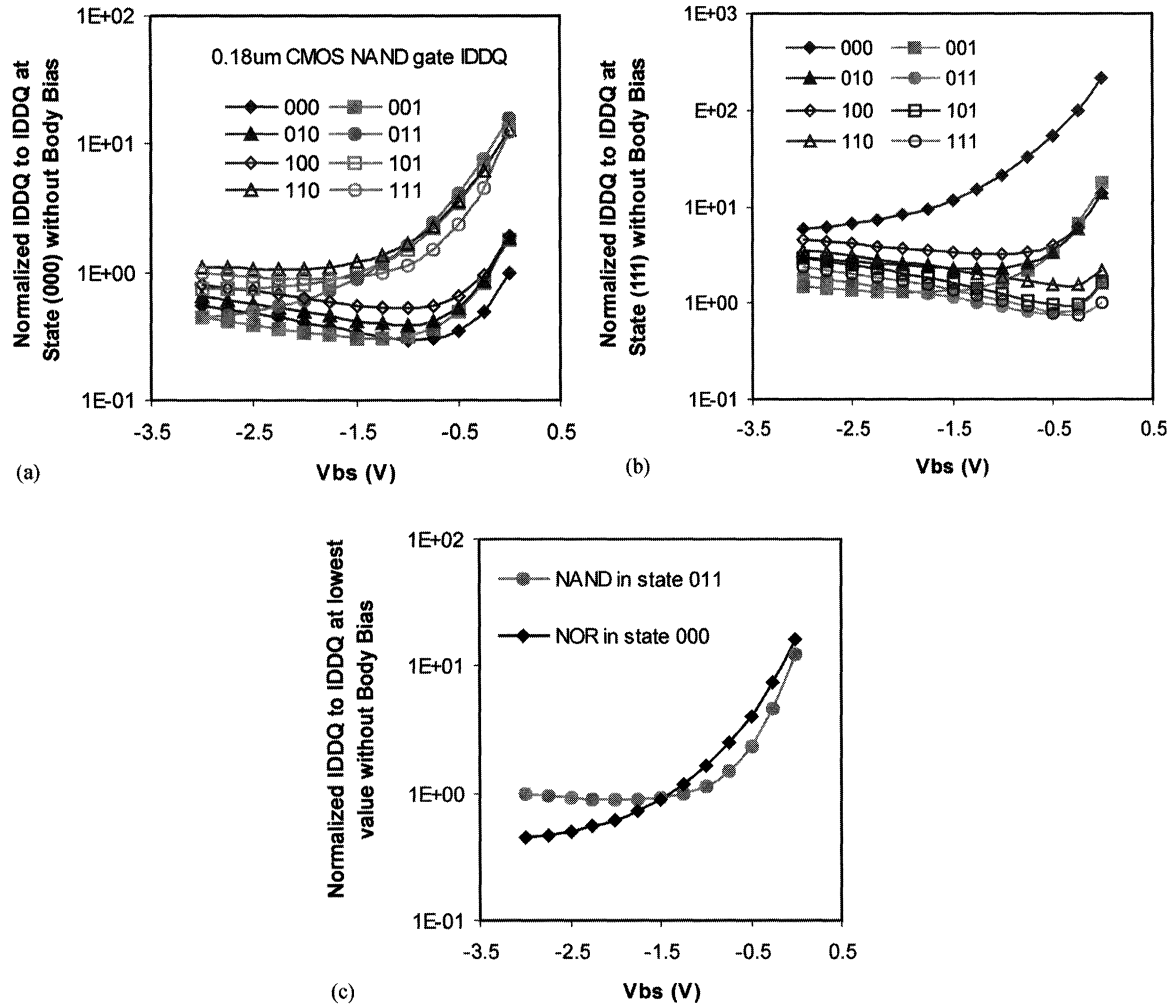

FIGURE 9 State dependency of defect-free I_{DDQ} of (a) three-input NAND neither gate (b) three-input NOR gate as a function of RBB. (c) comparing RBB dependence of both gates.

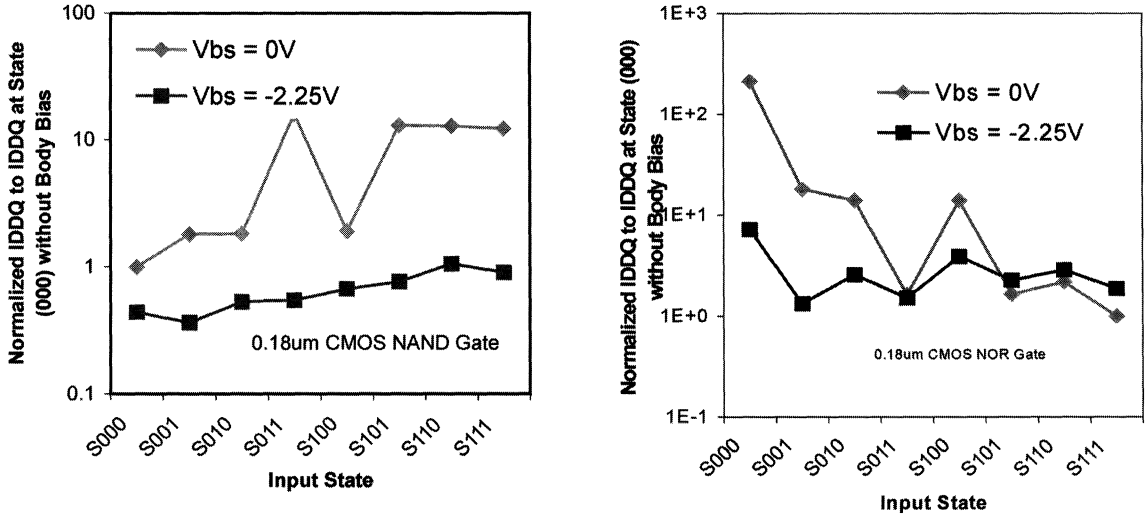

FIGURE 10 State-dependence of defect-free I_{DDQ} with and without RBB for three-input NAND gate and three-input NOR gate.

5. DEFECT DETECTION IN RBB CIRCUITS

In this experiment we used the same three logic gates used for studying the effect of RBB on the defect-free leakage current: an inverter, a three-input NAND gate, and three-input NOR gate. We injected a drain-to-source short at various transistors of the logic gate and measured the faulty circuit, I_{DDQ}, under specific RBB (V_{bs}) values. For each faulty circuit we swept the value of the shorting resistance, $R_{short,\ from}$ 100.0 Ω to 200 KΩ and recorded the current.

Table II summarizes the values of I_{DDQ} for the defect-free and defective gates under no-bias and $V_{bs} = -3$ V. For the inverters of 0.18 μm and 0.25 μm technology features and only the currents for the NMOS short are given. The results confirm the effect of RBB in reducing I_{DDQ} for the finer technology. As the bias has changed to −3 V, the defect-free I_{DDQ} has been reduced to 88% and 3% of its value at no bias for 0.25 μm and 0.18 μm technology features respectively. In the case of the defective inverters, I_{DDQ} has not changed appreciably for the 0.25-μm technology feature inverter (98%) while it has been reduced by 80% for the

TABLE II I_{DDQ} for technology features 0.18 μm and 0.25 μm logic gates

		Technology feature			
		0.25 μm		0.18 μm	
Gate	Current	$V_{bs}=0$	$V_{bs}=-3$	$V_{bs}=0$	$V_{bs}=-3$
Inverter	Defect-free	6.21 pA	5.485 pA	396 pA	11 pA
	Defective	298 μA	289 μA	236 μA	187 μA
NAND	Defect-free	28.8 pA	12.0 pA	333.75 pA	20.23 pA
	Defective	120.5 μA	112.68 μA	100.32 μA	72.52 μA
NOR	Defect-free	30.05 pA	26.25 pA	364.23 μA	20.98 pA
	Defective	137.08 μA	95.06 μA	108.39 μA	78.91 μA

0.18 technology feature. That is, RBB has lowered considerably the defect free current and has kept the faulty circuit current almost unchanged. From this information we may conclude that RBB has decreased the fault-free quiescent current considerably and left the faulty current unchanged. It seems promising then to continue using current testing for 0.18 μm technology if the appropriate reverse body bias is applied during testing.

Plots of the current *versus* the short resistance, R_{short}, are shown in Figure 11 for $V_{bs} = 0$ and $V_{bs} = -3$. For large values of the short resistance, it is difficult to distinguish the faulty current whether or not the circuit is biased. However, there is no evidence that current testing anyway uncovers such failures.

For the NAND and NOR gates, we examined the cases of drain to source shorts of the transistors in series and one of the transistor in parallel. The range of the short resistance was the same as in the case of the inverter. As R_{short} increased, the faulty current became independent of the V_{bs}. I_{DDQ} plots for the four defects with $R_{short} = 100\,\Omega$ in a three-input NOR gate are given in Figure 12. Shown also are the defect-free currents for the same input states; they are measured in pA as indicated with the right-side axis. The input state S000 represent the case where any of the NMOS transistors is shorted. This state represents the highest leakage current for the defect-free NOR gate as depicted in Figure 9.

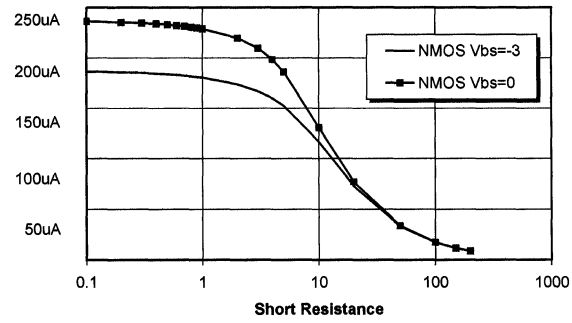

FIGURE 11 Defective inverter I_{DDQ} with and without bias.

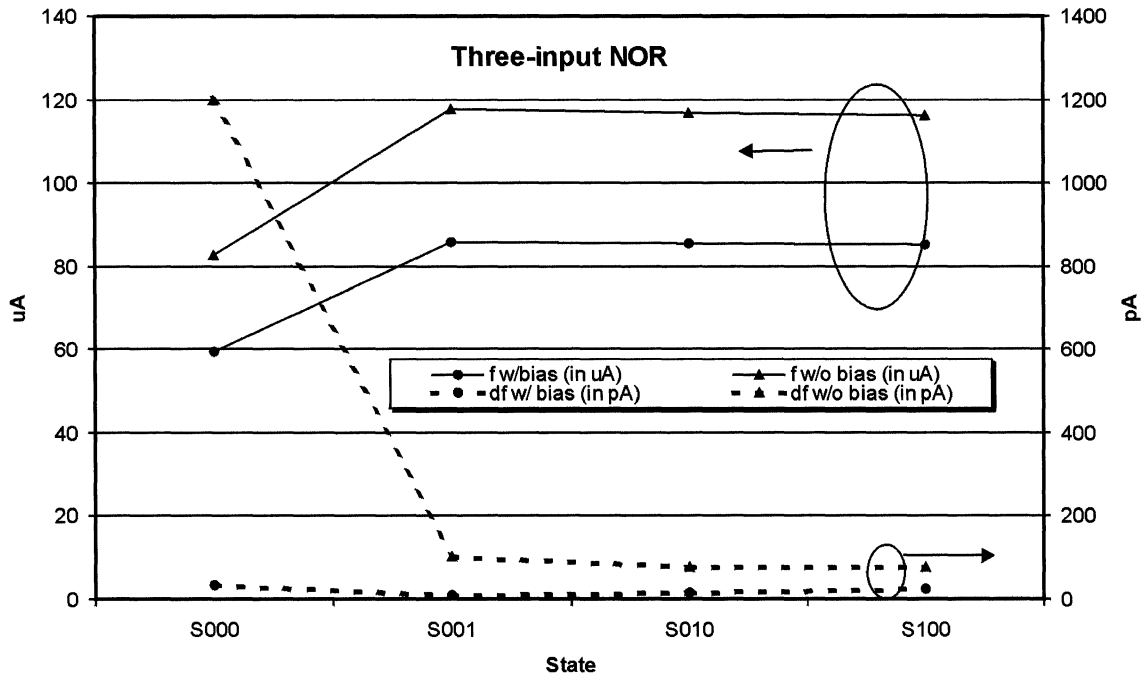

FIGURE 12 I_{DDQ} in defective and defect-free three-input NOR.

However, the current for the faulty circuit is lower since all three PMOS transistors are on and their path resistance is higher than in the case of the other states.

The average currents for the four defects with $R_{short} = 100$ as well as for the defect-free circuit in the case of 0.0 V and −3.0 V biases are listed in Table II. As in the case of the inverter, RBB has more considerably reduced the quiescent current for defect-free gate than the current for the corresponding defective gate.

6. TEMPERATURE DEPENDENCE OF DEFECT-FREE I_{DDQ} WITH REVERSE BODY BIAS

Experiments to study the effect of temperature on the quiescent current have been conducted for same logic gates used in the preceding experiment at three temperatures: 125°C, 25°C, and −50°C. The I_{DDQ} values are normalized to the I_{DDQ} of an 0.18 μm gate at 150°C without body bias ($V_{bs} = 0$). At temperature of 150°C, the worse case I_{DDQ} can be significantly reduced by nearly two order of magnitude by applying reverse body bias for all three gates (0.18 μm technology) with channel length 0.25 μm and 0.18 μm. However, the effect of body bias on I_{DDQ} weakens as temperature goes down. This is believed to be caused by different temperature dependencies of MOSFET leakage current components. The sub-threshold current increases dramatically with temperature, but the band-to-band tunneling current is almost temperature independent. For DSM MOSFETs, the sub-threshold current at room temperature dominates the leakage current. Therefore, raising the device temperature can significantly increase the sub-threshold current, and hence I_{DDQ}. Accordingly, lowering the device temperature will result in a significant reduction of sub-threshold current, and hence I_{DDQ}. This temperature dependence of I_{DDQ} at zero body bias can be clearly seen from Figure 13. At a low temperature, because the sub-threshold current is greatly reduced, the band-to-band tunneling current increases with reverse body bias and becomes dominant at a high reverse bias. Consequently, the reduction of I_{DDQ} by reverse body bias diminishes and the optimal reverse body bias that minimizes the I_{DDQ} shifts to a smaller value as the temperature goes down. For the three investigated logic gates, the state dependence is very different and the worse case defect-free I_{DDQ} occurs at different input states. However, the effects of reverse body bias and temperature on the worse case defect-free I_{DDQ} are very similar.

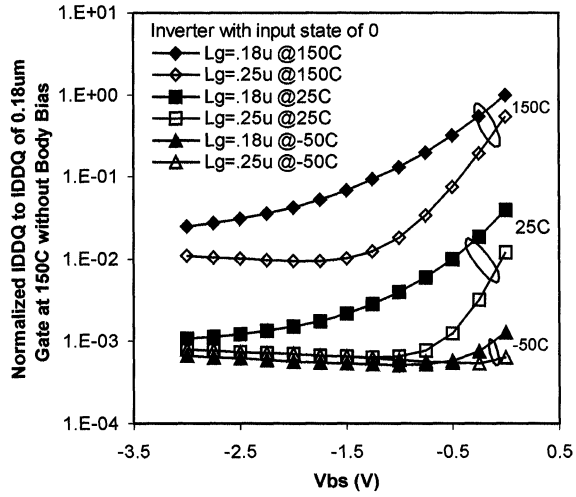

FIGURE 13 Worse case defect-free I_{DDQ} as a function of RBB for 0.18 mm CMOS technologies inverter with channel lengths 0.25 μm and 0.18 μm at three temperatures of 125°C, 25°C and −50°C.

7. DISCUSSION

7.1. Improvement in I_{DDQ} Resolution

For 0.18 μm technologies, worst state defect-free I_{DDQ} reduction of more than one order in magnitude has been demonstrated with optimal reverse body biases for typical CMOS gates, inverter, NAND, and NOR. Although the optimal values of V_{bs} for the inverter and for the other gates are different, it is possible to use either value and achieve significant reduction in the current. We also established that although RBB lowered

the faulty current too, the reduction is small as compared to that in the fault-free current. This implies that the I_{DDQ} pass/fail threshold can be reduced by one order in magnitude; therefore, the discrimination of I_{DDQ} testing will be significantly improved. The observation of existence of an optimal reverse bias for reduction of defect-free I_{DDQ} in simple cells also implies that there may exist an optimal reverse body bias for a certain product. Practically speaking, this means that one may not be able to continuously reduce defect-free I_{DDQ} by simply increasing the reverse body bias. One also needs to keep in mind that the optimal reverse body bias is dependent of product, process, and technology generation.

7.2. State Dependence of Defect-free I_{DDQ} with Reverse Body Bias

Strong state-dependence is one of the important characteristics for defect-free I_{DDQ} of deep sub-micron CMOS circuits [5, 16]. The I_{DDQ} pass/fail threshold has to be set high enough to account for the state with the most leakage. Unfortunately, such a threshold selection opens the door for chips with defects that are active in one of the states with naturally lower leakage to still pass the I_{DDQ} test, which leads to the shipment of defective ICs. On the other hand, to achieve reasonable defect screening means setting a threshold that is below even the maximum defect-free I_{DDQ} for some parts, resulting in excessive yield loss by rejecting good parts. One proposed alternative to the use of a single current threshold is to make use of state dependencies, both for defect-free and defective circuits. This approach, known as "current signatures" [8], has already been discussed as a potential basis for I_{DDQ} pass/fail determination. With high background leakage currents in deep sub-micron technology, however, these variations will become unnoticed [16, 17]. Another proposed approach for finding defective chips is to utilize differences between the observed state dependence and predicted one. However, it is very difficult to predict the state dependence of total leakage currents for large circuits and set I_{DDQ} limits for different states. Reverse body biasing has been shown effective in reducing the standby power of CMOS ICs. It is thus possible to exploit this design approach for I_{DDQ} testing. Demonstrations of significant reduction in defect-free I_{DDQ} and state dependence with reverse body bias in this study have suggested that, by applying reverse body bias during test, simple single pass/fail threshold I_{DDQ} testing can still work well for down to 0.18 μm generation.

7.3. Effect of RBB at Various Temperatures

Maintaining the circuit's temperature to $-50°C$ is definitely more effective in lowering I_{DDQ} than applying RBB. However, such a solution is possible only in very few applications. Under normal operating conditions, the circuit will not be working at 25°C. With an increase of the temperature, the quiescent current increased and RBB will be more valuable in reducing it.

7.4. Implication of RBB on Circuit Design

The use of multiple power supplies will definitely affect the design. According to [22], the overhead area is only marginal and the extra buses will not experience much switching activity. The main problem will be the increased chance for Latchup phenomenon. However, as we mentioned before, there are many successful designs with these extra buses [13, 29, 19].

8. CONCLUSIONS

In conclusion, investigations on defect-free I_{DDQ} in deep submicron CMOS with reverse body bias were performed by SPICE simulation to improve resolution of I_{DDQ} testing. Effects of reverse body bias on off-state leakage of scaled CMOS devices and I_{DDQ} of typical CMOS circuit cells were investigated. It was found that RBB could effectively reduce worst case defect-free I_{DDQ} of

typical circuit cells by more than one order in magnitude for technology generation down to 0.18 μm. Meanwhile, the faulty current has not been reduced as much which kept the difference between faulty and fault-free currents large enough to permit the selection of one unique threshold. This reduction is more pronounced as the device temperature increases. Reverse body bias also makes the defect-free I_{DDQ} less sensitive to the input state, therefore one single I_{DDQ} current threshold may still be used for I_{DDQ} testing down to 0.18 μm technology generation. It is found that there may exist an optimal reverse body bias that minimizes the defect-free I_{DDQ} current.

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