VLSI Design, 2002 Vol. 14 (2), pp. 193–202

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An Embedded Low Transistor Count 8-bit Analog-to-digital Converter Using a Binary Searching Method

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(Received 6 December 1999; Revised 23 May 2000)

Small analog-to-digital converter (ADCs) are very popular when they are required in many interfaces or system designs. Ever since the system-on-chip (SOC) became one of the major trends in chip designs, the demand for small and less power draining ADCs has urgently emerged. The area factor is particularly critical when it comes to the cost issue. In this paper, a small but stable ADC intellectual property (IP) macro design is proposed wherein a binary search scheme is utilized to produce the ADC function. A total of eight cycles are needed to convert the analog signal based upon simulation results. A physical chip is fabricated to verify the correctness of our design.

Keywords: ADC; Area-saving; Binary searching method; SOC; IP; VLSI

INTRODUCTION

Ever since the emergence of system-on-chip (SOC) design methodology, the demand of efficient intellectual property (IPs) became urgent when it comes to the integration of mixed-signal interface IC or system designs. One of the key IPs is the macro design of analog-to-digital converter (ADCs), which are widely used in interface designs. Prior works to improve ADCs are mainly focused on speed and bit length by using alternative architectures, e.g. pipelined, flash, delta–sigma modulation, etc [2,3]. If the mentioned ADCs are to be incorporated with other design modules, e.g. codecs or microprocessors, on a single chip, the area factor will appear. Hence, we propose a simple ADC design method that is able to provide an area efficient solution with reasonable conversion cycles. Also, the proposed design approach can be expanded to a longer data length at the expense of linear hardware overhead. Meanwhile, a real chip design for 8-bit ADCs using our design approach is given together with successful and convincing simulation results. The chip has been approved by Chip Implementation Center (CIC) of National Science Council (NSC) and fabricated by United Microelectronics Co. (UMC). The testing results turn out to be very appealing.

AREA-SAVING ADC DESIGN

Binary Searching Method

A simple approach to design an efficient ADC is to utilize a digital-to-analog converter (DAC). Take an 8-bit conversion as an illustrative example. The entire ADC conversion procedure is as follows.

1. Use the DAC to produce a reference voltage, V_r, given input digital data as 10000000.
2. Compare the input analog voltage, V_i, with V_r.
3. If $V_i > V_r$ the first bit is set to 1. Then the input data to the DAC is 11000000. By contrast, if $V_i < V_r$, then the first bit is set to 0. Then the input data to the DAC is 01000000.
4. Repeat the procedure of generating the reference voltage, comparing two voltages, and set the input digital data for eight times.
5. The conversion result will be kept in designated FFs after eight cycles.

The entire binary searching concept is graphically shown in Fig. 1 Although the complexity of the design looks severe, most of the hardware units are reusable.

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ISSN 1065-514X print/ISSN 1563-5171 online © 2002 Taylor & Francis Ltd
DOI: 10.1080/10655140290010105

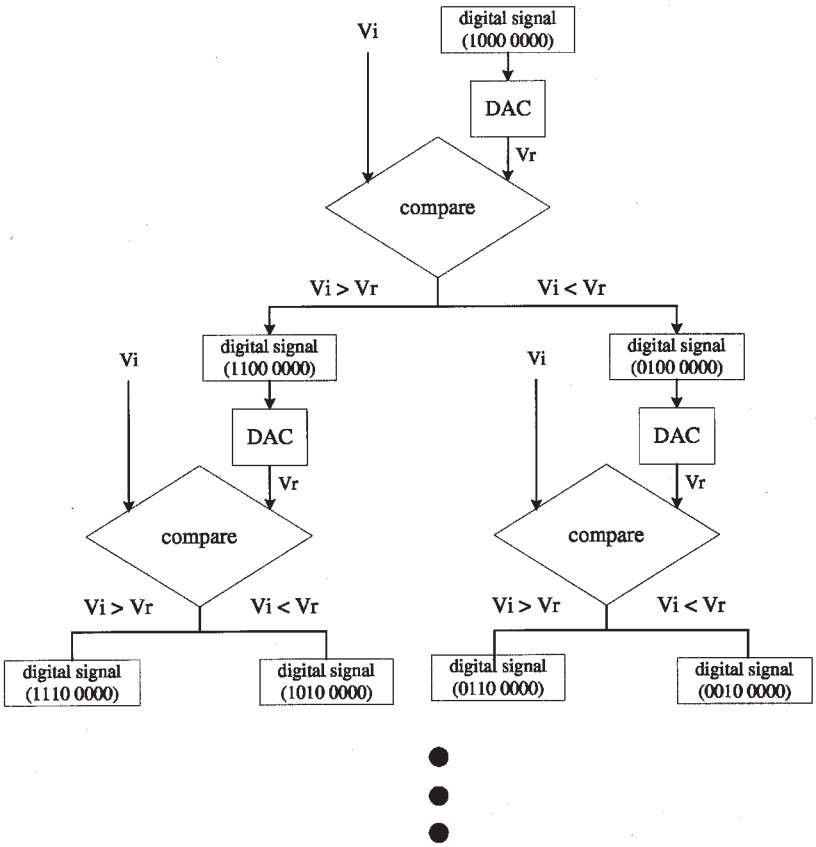

FIGURE 1 Binary searching scheme.

Circuit Implementation

In order to implement the mentioned design approach, two sets of DFFs are required. One set of nine DFFs is composed of a byte-wide P_7–P_0 whose outputs of are fed into the clock pins of the other set of eight DFFs, B_7–B_0, respectively, and one single P_X. Thus, two major functions of P_i's and P_X can be achieved. Firstly, a zero pulse train generated by P_i's and P_X, as shown in Fig. 2, preset the B_i's sequentially in each cycle. Then, the total eight

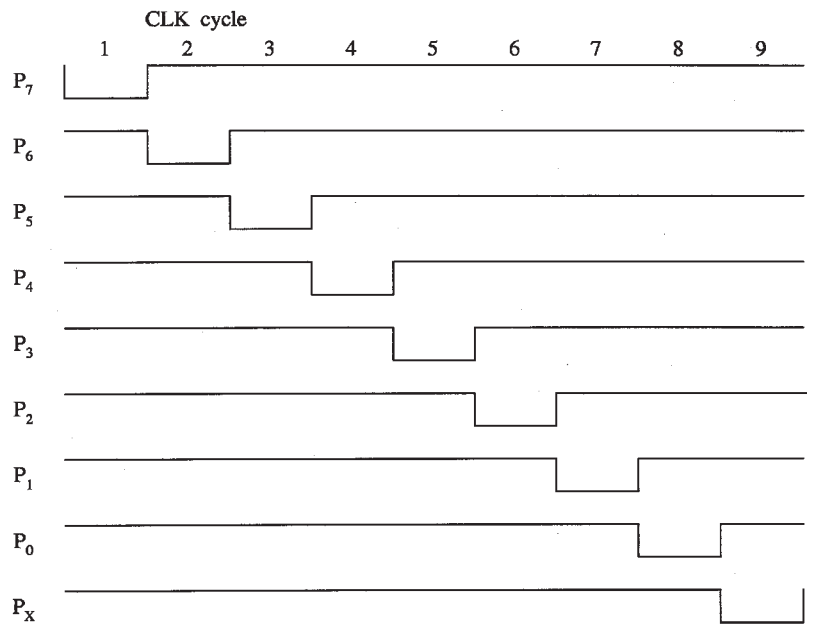

FIGURE 2 Low pulse train.

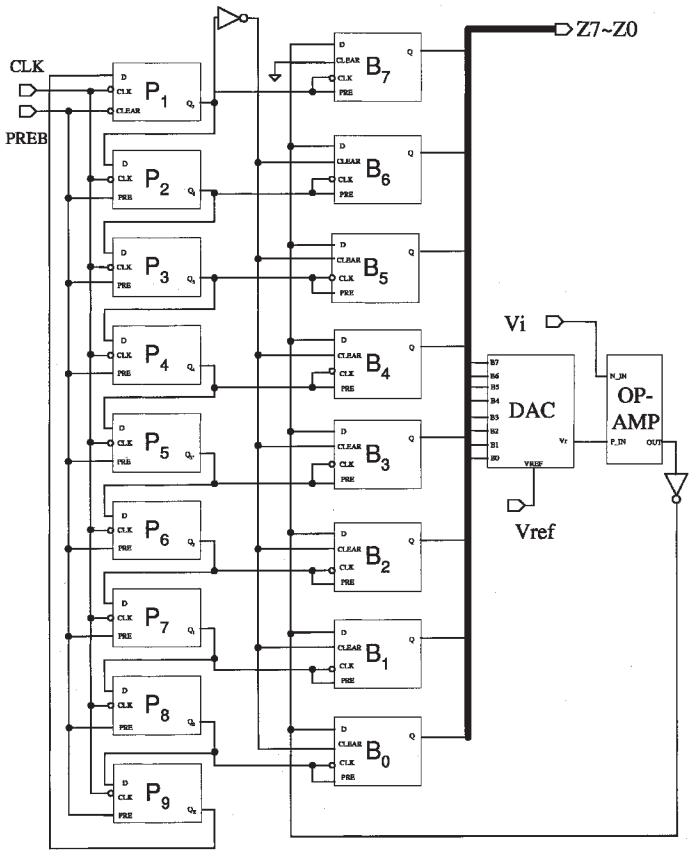

FIGURE 3 Proposed 8-bit ADC design.

outputs of B_i's are fed into the following DAC to generate a reference voltage. Secondly, owing to that the outputs of this set of DFFs are fed into the clock and preset pins of the other set of eight DFFs, B_7–B_0, such that the comparison result bit generated by OP-AMP can be locked in its corresponding B_i DFF, where $i = 7\ldots0$. The entire design is shown in Fig. 3. Restated, PREB is the signal to start the entire ADC cycle so that it is also used as either preset or clear signal for the DFFs. Another feature of the proposed ADC is that the DFFs used in the entire design are back-to-back inverter-based flip–flops, which consume less chip area than master–slave style flip–flops. For instance, the schematic of P_7 is shown in Fig. 4 where the first inverter pair loop is controlled by a

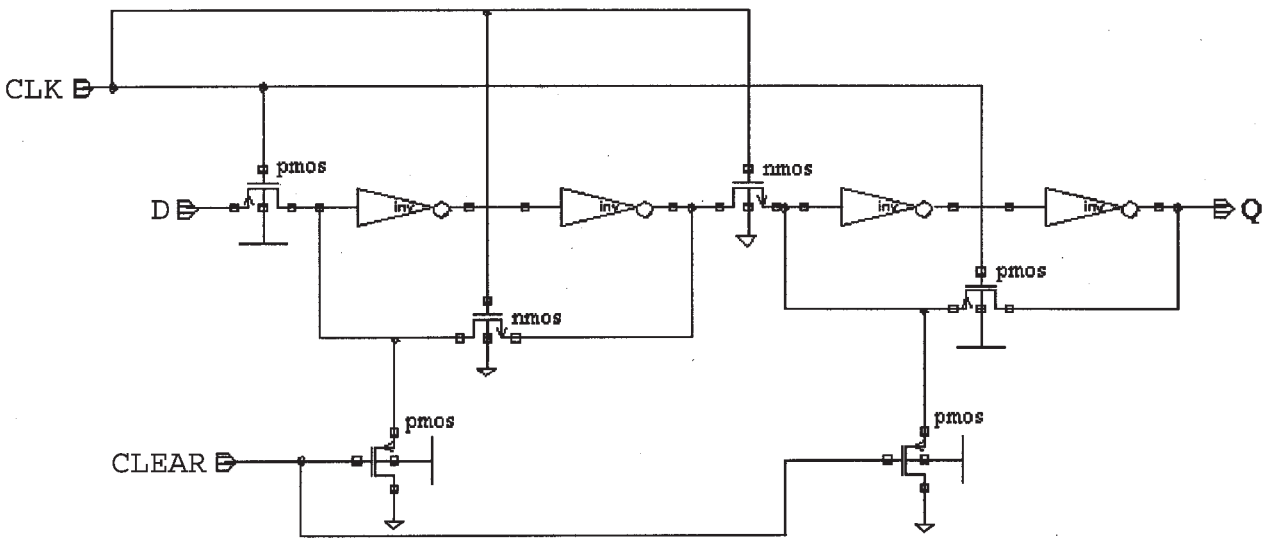

FIGURE 4 Schematic of DFF P_7.

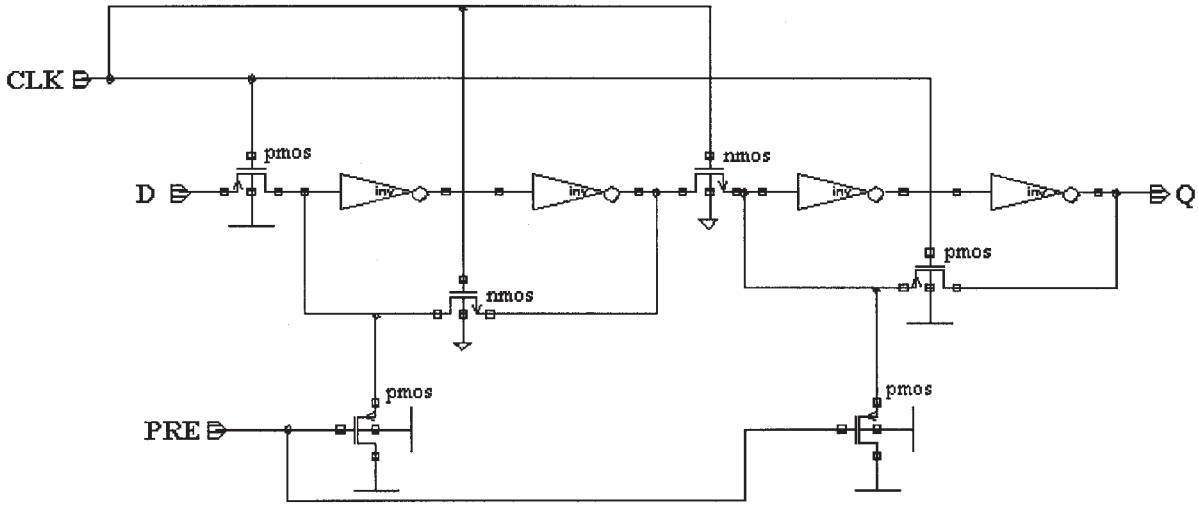

FIGURE 5 Schematic of $P_6 \sim P_0$ and P_X.

clock-triggered NMOS, while the second inverter pair loop is controlled by a clock-triggered PMOS. By contrast, the path from signal D to the first inverter pair is controlled by another lock-triggered PMOS, while the output of the first inverter pair to the input of the second inverter pair is controlled by another clock-triggered NMOS. Then, the input data, "D", will be latched at the falling edge of the clock, and the output data will be ready at the rising edge of the clock.

Design of Various DFFs

Though the area-saving design is our main focus, the sacrifice regarding delay (speed) should not be too large. Thus, the designs of DFFs are targeted on latching the input data at the falling edge, and delivering data at the rising edge. In order to achieve such a function, the DFFs used in Fig. 3 are categorized into three various designs.

(1) *DFF for P_7*: When CLEAR is low, the Q of P_7 is connected to GND. That is, the Q is cleared to be "0".
(2) *DFF for P_6–P_0 and P_X*: When PRE is low, the Q's of these DFFs are preset to be "1" because the PRE will turn on the connection between Q and VDD. The schematic diagram of these FFs are shown in Fig. 5.
(3) *DFF for B_7–B_0*: When PRE is low, Q is shorted to VDD to preset the DFF. When CLEAR is high, the

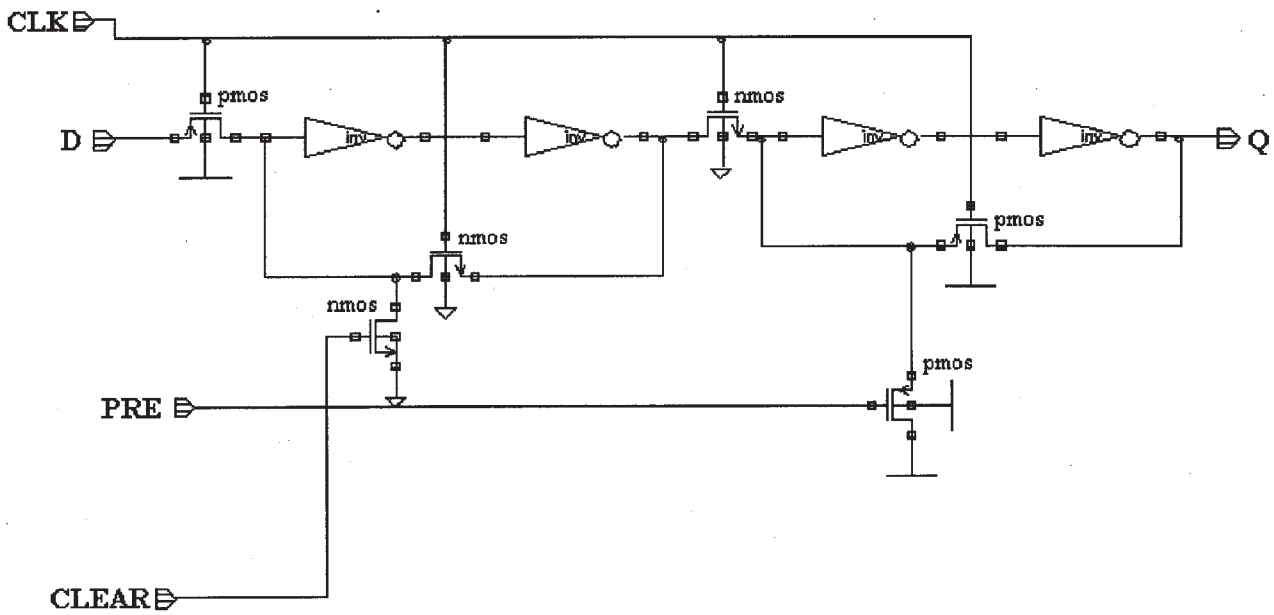

FIGURE 6 Schematic of $B_7 \sim B_0$.

TABLE I The hardware cost analysis of different ADCs (n is the number of conversion bits).

	Staircase [2]	Flash [3]	Resistor string [4,7]	Ours
# Cycle	2^n	1	2^n	n
# DAC	1	0	0	1
# OP-AMP	1	2^n	1	1
# Resistor	$2n+2$	2^n+2	2^n+2	$2n+2$
# DFF	n	n	n	$2n$

output of the first inverter pair is cleared to be "0" given clock = "1". The circuit of these DFFs is shown in Fig. 6.

Considerations of the Single-shot Conversion

a. The output Q_7 of DFF P_7 is generated as the top stripe in Fig. 2 when PREB is activated. The low pulse of Q_7 is also connected to the clear input of B_6–B_0 through an inverter to clear these DFFs.
b. The clear signal of B_7 which keeps the MSB of the conversion result is always grounded such that it will not be affected by any of the following conversion steps.
c. The output Q_i of each P_i, is connected to the input "D" of P_{i-1} to propagate a low pulse such that the waveforms of Fig. 2 can generate.
d. The output Q_i of each P_i is connected to the "CLK" and "PRE" of the corresponding B_i such that the resulted bit of the $(8-i)$th conversion step will be latched at the B_i DFF. Note that $i = 7\ldots0$.
e. The function of P_X is to keep the conversion result for an extra cycle for the purposes of observibility and testability. Another function is to feed a "0" to P_7 at the start of the entire conversion procedure.

Theoretical Analysis

Compared to prior ADC designs, [2–4,7], our proposed ADC possesses the area-efficient edge according to the theoretical analysis results tabulated in Table I.

The staircase approach and the resistor string approach generate a delay growing exponentially with n. On the other hand, the fast flash approach demands too many OP-AMPs and resistors that usually occupy too much chip area. Our design provides a reasonably fast solution for the embedded ADC (Table II) with the area penalty growing linearly with n.

SIMULATION AND IMPLEMENTATION

Chip Implementation

The proposed ADC design is implemented with UMC. 2P2M 0.5 μm CMOS technology. The design tools are CADENCE OPUS, DRACULA and HSPICE. The layout is shown in Fig. 7. The characteristics of this chip is tabulated as follows.

Notably, in order to prevent any possible noise coupled from digital circuits to the analog circuits, the guard ring is inserted around the analog part of the chip, which is also shown in Fig. 7. Meanwhile, the pin assignment is also given in Table III. The proposed design has been approved by CIC of NSC to be fabricated by UMC given the chip number: U05-88D-05u.

Speed (Delay) Simulations

Figures 8 and 9 show an example of conversion using the proposed ADC design. The former reveals the clear waveforms when the input voltage is close to the lower bound of the working range, while the latter shows the scenarios when given an input voltage close to the upper limit.

Comparison with Other Designs

Table IV tabulated a comparison between our proposed ADC design with other recently announced ADCs. Note that the measurement of "Area/Bit" indicates how much

TABLE II The characteristics of the ADC chip

	Data
Die size	$1.8 \times 1.8\,mm^2$
Core size	$850 \times 450\,\mu m^2$
Working range	0.15–3.85 V
Resolution	10 mV
Maximum clock frequency	8.0 MHz
Sample rate	1.0 Msamples/s
Power dissipation	41.8 mW at maximum clock frequency
Transistor count	103

TABLE III The pin assignment of the ADC chip

Pin	Function
CLK	External clock input
PREB (1 bit)	When low, the chip is reset
VREF	Reference voltage input for the DAC
VIN	The input voltage to be converted
Z7–Z0 (8 bits)	The converted byte-wise result
VDD, GND	Digital power pairs

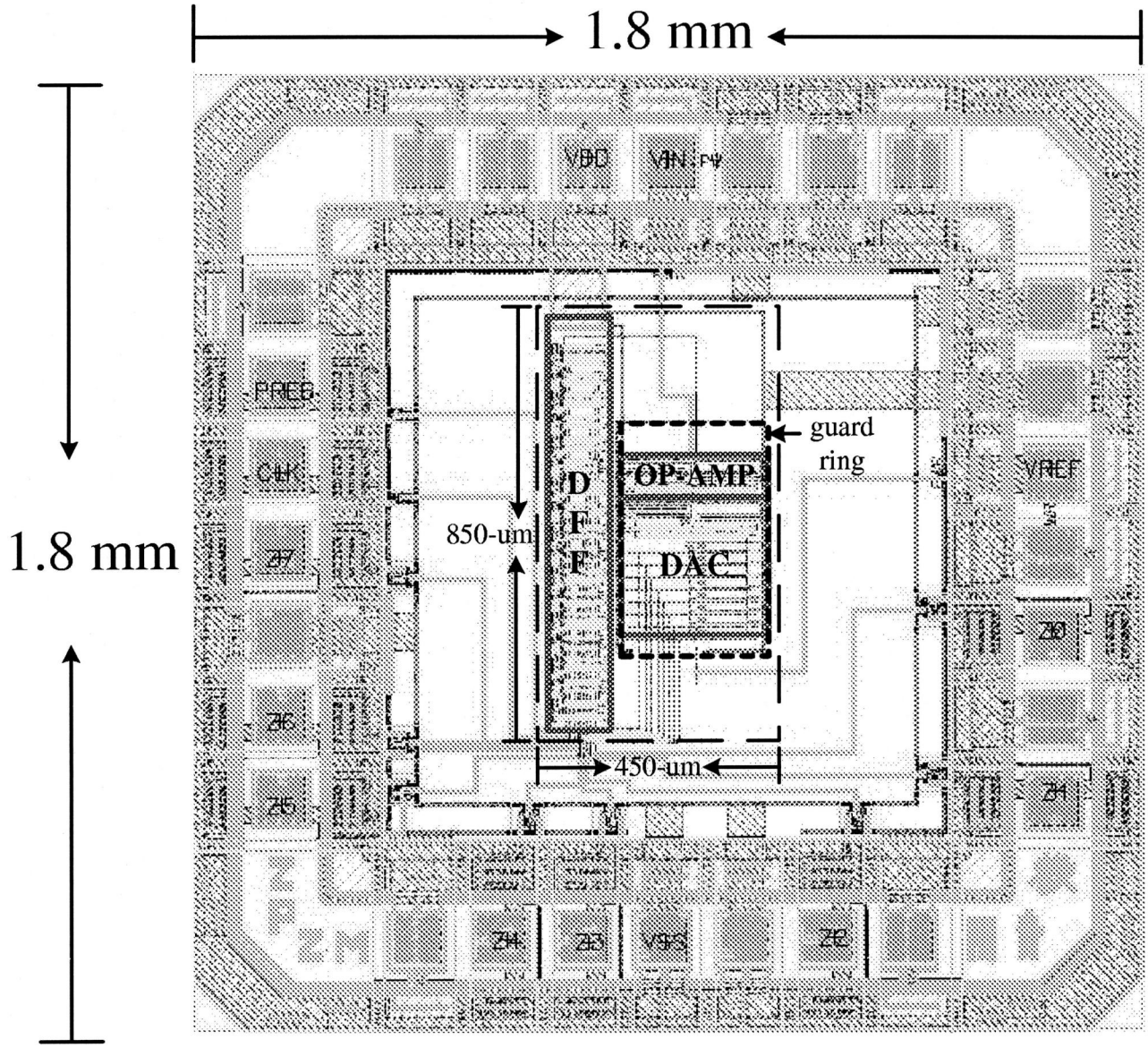

FIGURE 7 Chip layout.

area is required to convert a bit, which is considered an important factor in embedded ADC designs.

According to Table IV, our design indeed possesses the lowest "Area/Bit" ratio in this ADC chip design. The proposed ADC also has the second best power dissipation performance next to Nys's design [8].

TABLE IV The comparison of various ADCs

Name	Area (core, mm^2)	Power dissipation (mW)	Area/Bit
Jonsson's [5] (10-b)	2.7	NA	0.27
Jonsson's [6] (10-b)	22	660	2.2
Nys's [8] (19-b)	14	2.7	0.737
Bult's [1] (10-b)	1.2	1100	0.12
Ours (8-b)	0.3825	41.8	0.04781

Chip Testing and Measurement

The physical die photo of the proposed ADC chip is shown in Fig. 10. We used HP 1660 CP analyzer/pattern generator to test the chip. Figures 11 and 12 shows the measured results of the given input voltage 0.962 and 0.470 V, respectively. The results of A to D-conversion are 0011–1111 and 0000–1001 correspondingly. These results verify the correctness and functionality of our design.

CONCLUSION

The proposed binary searching design method not only provides a simple solution for embedded ADC circuits, but also shows superiority regarding area and power factors.

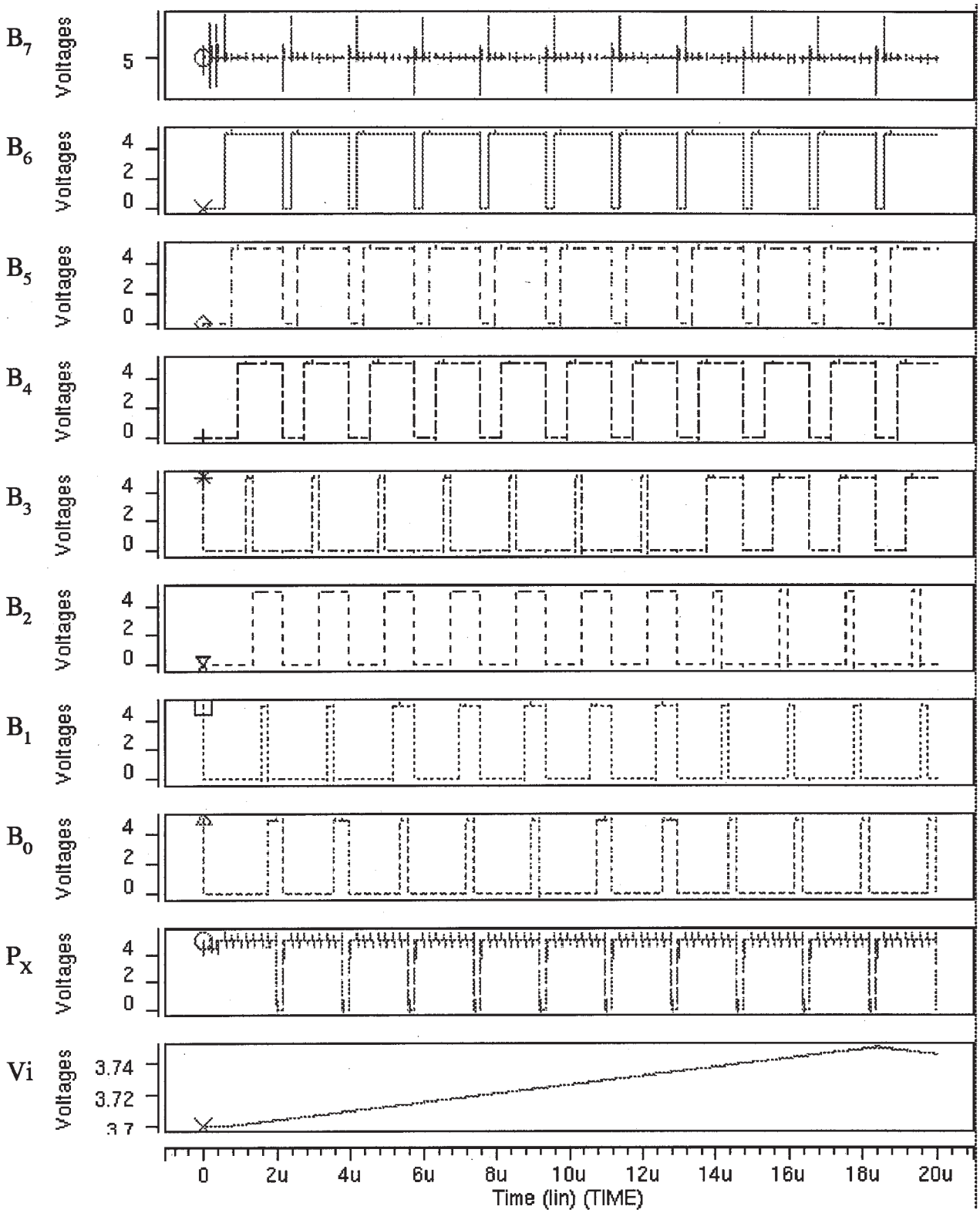

FIGURE 8 Simulation waveforms given V_i close to the upper bound.

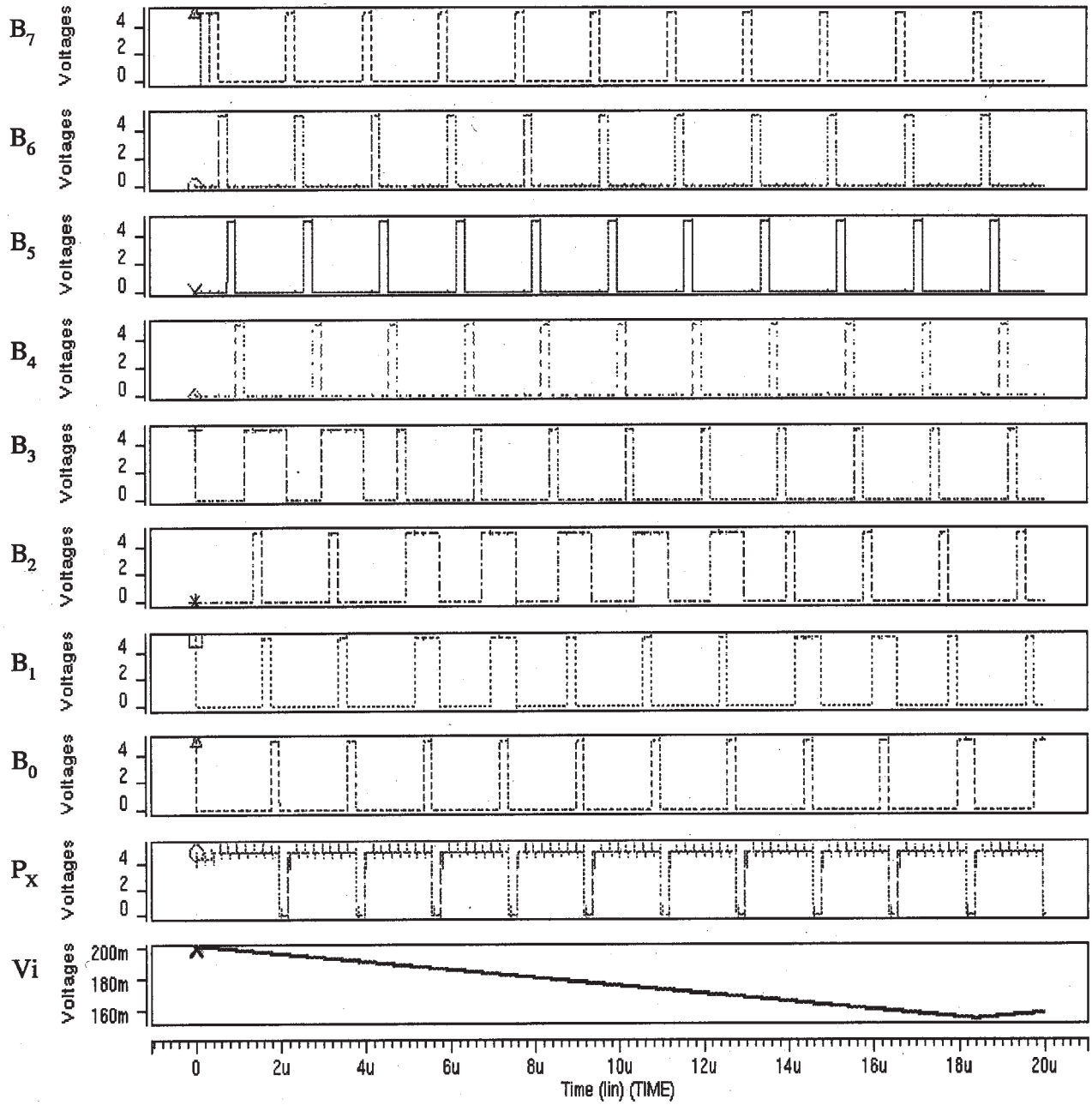

FIGURE 9 Simulation waveforms given V_i close to the lower bound.

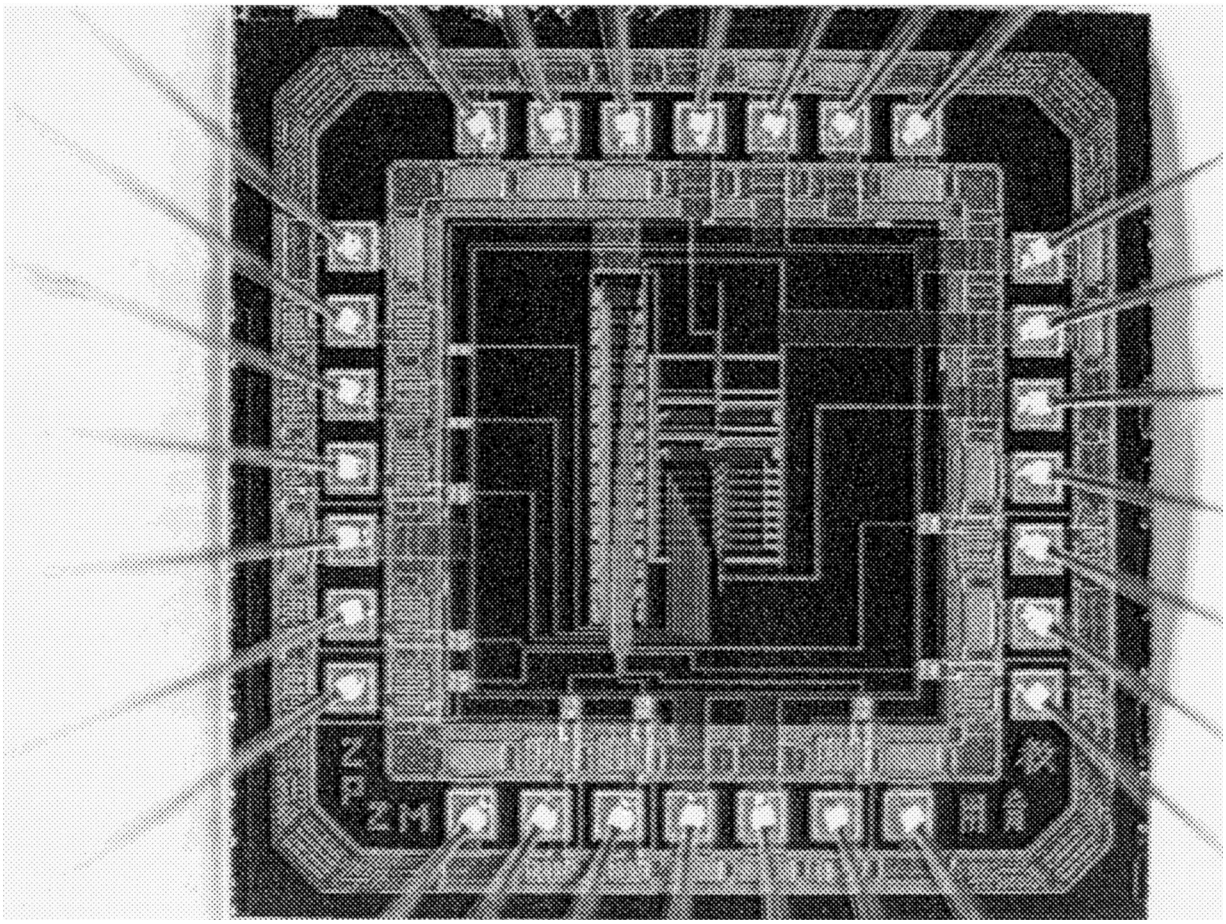

FIGURE 10 Die photo.

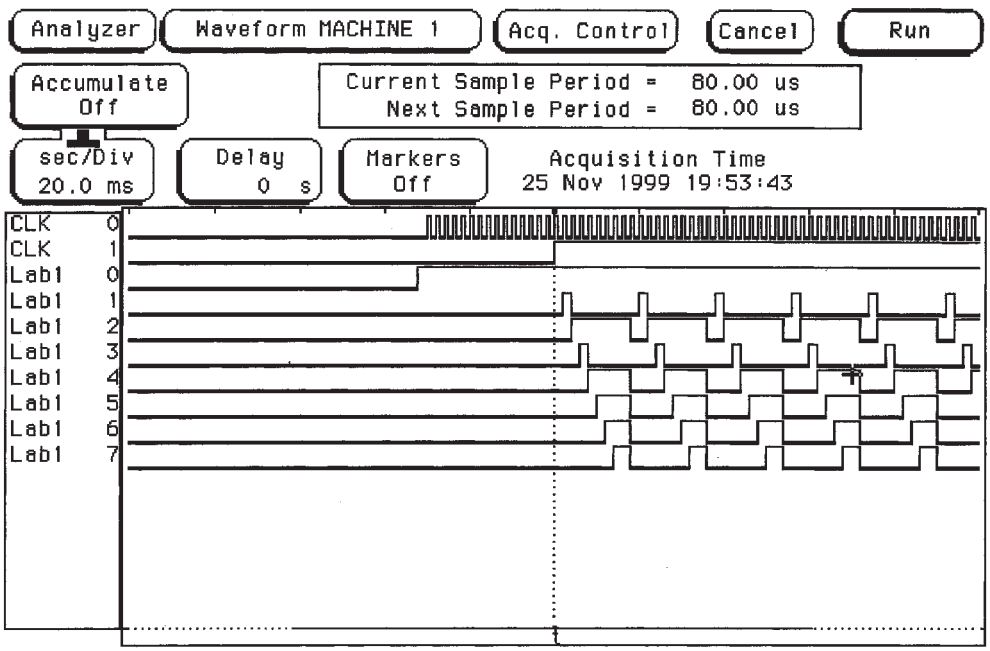

FIGURE 11 Measured result with HP 1660CP given $V_{in} = 0.962$ V.

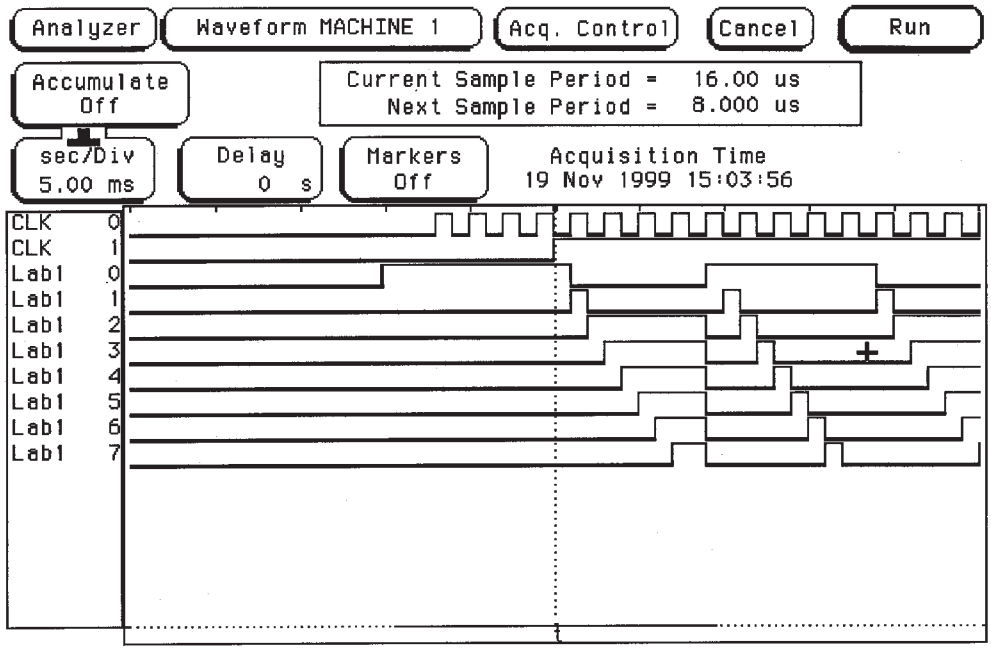

FIGURE 12 Measured result with HP 1660CP given $V_{in} = 0.470\,V$.

In addition, the design approach can be easily expanded to a wider data length when needed. The physical chip proves the proposed design.

Acknowledgements

This research was partially supported by Industrial Technology Research Institute under grant ITRI G4-88007-o and T2-89042-f, and National Science Council under grant NSC 87-2215-E-110-010 and NSC 88-2219-E-110-001.

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Authors' Biographies

Chua-Chin Wang was born in Taiwan, in 1962. He received the BS degree in electrical engineering from National Taiwan University, Taiwan, in 1984 and the MS and PhD degrees in electrical engineering from State University of New York, Stony Brook, in 1988 and 1992, respectively. Currently he is a Professor in the Department of Electrical Engineering, National Sun Yat-Sen University, Taiwan. His research interests include low-power logic and circuit design, VLSI design, and neural networks and implementations.

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Shao-Ku Huang was born in Taiwan, in 1962. He received the BS degree in power mechanical engineering from Mational Tsing-Hua University, Taiwan, in 1984 and the MS degree in aeronautics and aerospace engineering from National Cheng Kung University, Taiwan, in 1986. He was a manager in charge of mobile handset project of Computer and Communication Lab of Industrial Technology Research Institute during 1992 to 2000. Currently he is an executive director of Wireless Business Unit of Quanta Computer Inc. in Hsin-chu, Taiwan. His research interests include RF circuit and system design, VLSI design, and mixed-signal circuit implementations.