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Research Article

A Q-Enhanced 3.6 GHz, Tunable, Sixth-Order Bandpass Filter Using 0.18 μm CMOS

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An experimental filter was designed to operate at 3.6 GHz using mainstream 0.18 μm CMOS. In the design, the Q-enhancement technique was used to overcome the low-Q characteristics of the CMOS on-chip inductors. A sixth-order bandpass filter with a wide passband and a high image rejection was built by cascading three stages of second-order Q-enhanced filters. A combination of three biquads with offset in center frequency provides wider tuning frequency and bandwidth. This high-performance filter provides a 340 MHz tunable center frequency around 3.6 GHz, an image rejection of 50 dB and a tunable Q from 25 to 50 for a bandwidth adjustment from 95 MHz to 35 MHz. The filter achieves an 18 dB voltage gain while consuming 130 mW of power at 1.8 V DC supply. The chip occupies an area of 900×900 μm^2 including all the required bonding pads. The design provides a simple architecture to simplify tuning scheme for both frequency and bandwidth for practical use. The tunable ability of the design could be exploited in further study to be used as a channel-select filter in the gigahertz range.

1. INTRODUCTION

The rapid growth in wireless telecommunication systems necessitated research and development of monolithic bandpass filters for gigahertz radio frequencies. There has been great interest in building LC bandpass filters using monolithic inductors on silicon [1–7]. The drawback in the integration of these filters in a single chip is mainly due to the lack of high-Q on-chip inductors. Recent progress in IC technology highly improves performances of the CMOS RF components. The integration of filters in GHz range faces many hurdles such as the design of high-Q on-chip inductors and capacitors and in particular, the accurate high-frequency CAD models for on-chip passive components. In addition, the design of a wide tuning range and high-quality varactors in CMOS technology is also a great challenge [8].

This paper presents an approach and design of a tunable 3.6 GHz CMOS bandpass filter to achieve the following characteristics: low-noise figure, wide-tuning range, high-voltage gain, and high-linearity. The filter is designed as a second-order and then cascade to form a sixth-order filter with a tuning capability in both center frequency and quality factor. These tunings offer frequency selection and bandwidth adjustment. Power gain, noise figure, and particular linearity of the filter are also taken into considerations of the design.

2. TUNABLE BANDPASS FILTER DESIGN

The basic second-order bandpass filter includes an input transconsductor to interface with other devices, a tunable LC resonator to provide fundamental frequency and a Q-enhancement circuit to increase filter qualify factor. Two separate voltages are used to tune the filter frequency and Q. Figure 1 shows a block diagram and a simplified schematic diagram for the second-order BPF.

2.1. The input transconductor and the LNA

The input transconductor is used as an input stage for the filter. In this design, the input transconductor directly connected to a 50 Ω system. Such direct connection requires an impedance matching for power transfer from the external device to the gate of the input transistor. A source degeneration input transconductor shown in Figure 1(b) is used. This transconductor also acts as a low-noise amplifier (LNA) to reject part of the undesired bandwidth. This structure provides a good input impedance matching, a good power

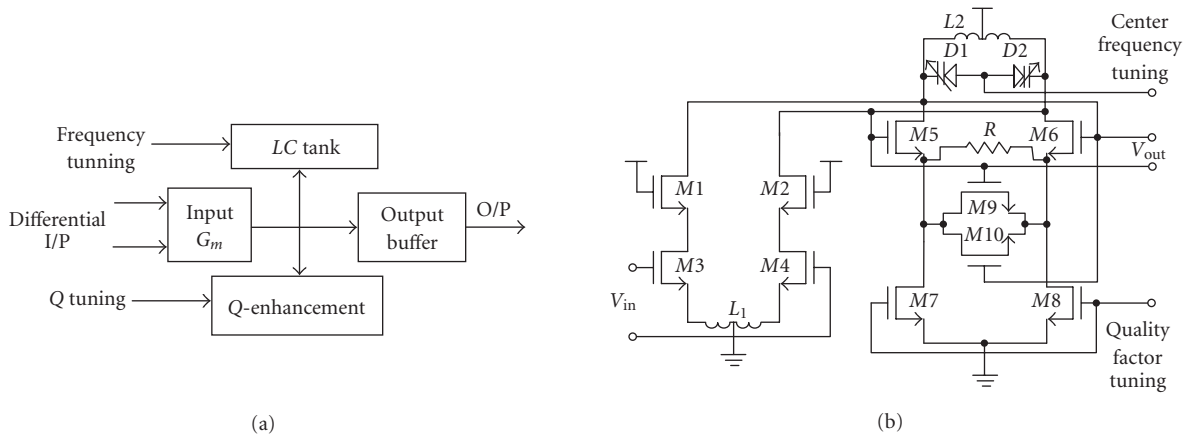

Figure 1: Block diagram and simplified schematic diagram of the second-order BPF.

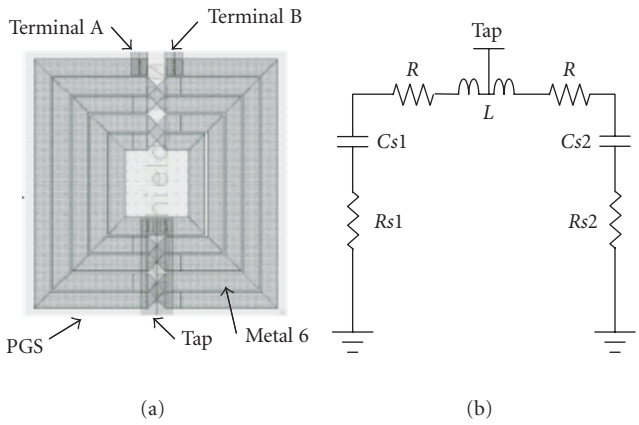

Figure 2: A center-tapped symmetrical spiral inductor and its model.

handing capability, a high linearity characteristic, and a low-noise figure. The impedance of this input transconductor can be controlled by careful design and layout of the inductor $L1$ and the gate-to-source capacitances of the input transistors. It has been known that the first stage requires a circuit with a noise figure as low as possible, therefore care has been taken in the design of this LNA. Note that the design employs the differential mode. This mode offers a stable reference point for the LNA (i.e., the other half circuit instead of the unreliable ground point due to parasitics of the single-ended mode). Another benefit of this mode is the linearity improvement by canceling some of the harmonics.

2.2. The LC resonator

The parallel LC circuit shown in Figure 1(b) is used as a second-order resonator. This tank circuit includes a pair of inductors and a pair of diode junction capacitors (varactors). In this design, a center-tapped symmetrical spiral inductor shown in Figure 2 is used.

This geometry provides symmetrical inductors in a single coil. The benefit of this configuration is that the inductors can be used in differential mode which is the topology of this design. Metal 6 (the top metal layer in the 0.18 μm CMOS technology) is used as wire because this thick layer of metal locates far from the lossy substrate. Metal 5 is used for interconnections between the turns. To further reduce substrate loss, a patterned ground shield (PGS) in metal 1 layer is formed underneath the inductor. This PGS also helps to further isolate the noise from the substrate [9]. This 5-turn inductor has a wire width of 8 μm, a turn spacing of 1μm, an inner radius of 16 μm, and an outer radius of 60 μm based on [10]. Figure 2 also shows the inductor model and its parameters are listed in Table 1. Structure of the p^+ to n-well junction varactor is an array of small junctions instead of a large junction. This arrangement occupies a smaller chip area and the sidewall capacitances increase the variable capacitance per unit area. This increment provides a better $C_{\max}/C_{\min}$ ratio for the tuning range of the resonator. The designed varactor consists of 8 junction array columns and 7 junction array rows with a width and length of 5.8 μm. Figure 3 shows a layout of the array varactor used in this design and its model. The model includes an n-well to p-substrate junction and side-wall capacitors. The inherent losses are represented by the series resistor and the parallel resistor. The series resistor represents the losses associated with the junction and the parallel resistor represents the lossy signal path through the p-substrate.

The junction capacitance, C_j, is a function of various parameters as follows:

$$C_{j(Vr)} = \frac{C_{j0}A_j}{\left(1 + V_r/\Phi\right)^{mj}}, \tag{1}$$

in which C_{j0} is the junction capacitance per unit area at zero voltage, A_j is the junction area, Φ is the built-in junction potential, and mj is a fitting process constant. This constant depends on the doping profiles for p^+ and n^- implantations. As indicated, this junction capacitance is a function of the reverse voltage (V_r) across the varactor. Changing this

Table 1: Inductor model.

Symbol	Component	Value
L	Inductor	2.042 nH
R	Serial parasitic resistor	4.3 Ω
Cs1	Inductor to substrate capacitor	45.81 fF
Cs2	Inductor to substrate capacitor	44.92 fF
Rs1	Substrate loss	3.314 Ω
Rs2	Substrate loss	4.376 Ω
Q	Quality factor	4.9
f_0	Resonance frequency	16.45 GHz

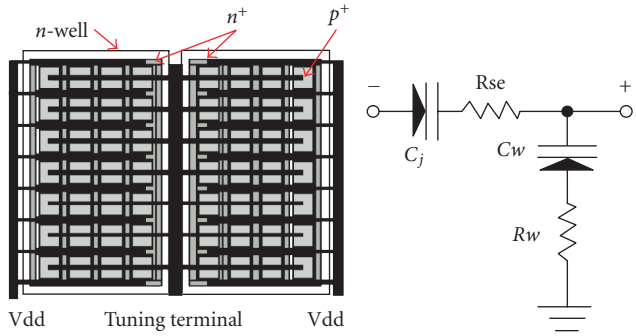

Figure 3: The designed varactor and its model.

voltage varies the capacitance of the tank circuit and eventually changes the tank resonance frequency.

The model above is used to simulate using advanced design system (ADS) simulator. The Q values of the varactor were found between 25 and 29 depends on its tuning voltage as shown in Figure 4. Simulation results also indicate a C_{max}/C_{min} ratio of 1.11 (C_{max}=2.825 pF, C_{min}=2.550 pF). As the low Q of the on-chip inductor and varactor inherent from CMOS, a Q-enhancement technique is employed in the design to increase the overall quality factor of the filter.

2.3. The Q-enhancement circuit

The basic function of the Q-enhancement technique is to add a negative conductance to the LC circuit to compensate the losses in the resonator. Serial parasitic resistor of the on-chip inductor, low Q diode junction capacitance, and lossy substrate are the main sources of loss in the LC tank. The inductor resistance usually dominates the loss. Detailed explanations on the losses and techniques to generate a negative impedance, $-G_m$, to reduce the loss can be found in literature such as [5, 11].

2.4. Design of the sixth-order bandpass filter

A wideband filter with good selectivity can be implemented with higher order filters; one way is to cascade several stages of the second-order filter [12]. Three stages of the second-order are coupled with capacitors to form a sixth-order filter

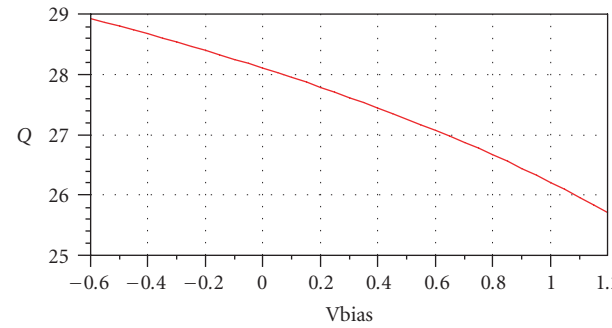

Figure 4: Q of the varactor as a function of its reverse bias voltage.

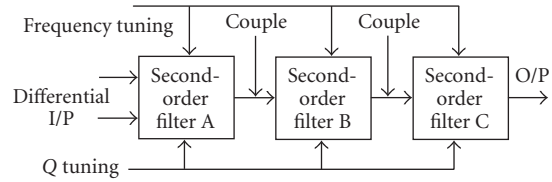

Figure 5: The sixth-order cascaded filter.

as shown in Figure 5. The stages are tuned to three different center frequencies. In this design, with a single tuning voltage, the first stage is tuned around 3.56 GHz, the second stage around 3.64 GHz, and the third stage around 3.60 GHz. As a result, the overall center frequency of the filter is at 3.6 GHz with a wider bandwidth. A simplified schematic diagram of this sixth-order filter is shown in Figure 6.

2.5. Tuning method

2.5.1. Frequency tuning

Frequency tuning of the second-order filter is implemented by varying the reverse voltage of the junction diode varactor. In the sixth-order filter, there are three stages that contain three different resonators. Each stage must be tuned to a different center frequency to provide an overall wider bandwidth. This can be only realized by tuning each stage separately. To simplify the frequency tuning scheme, an innovative method was used so that only one tuning terminal is used to tune all three center frequencies. In order to set the center frequencies apart to have a wide bandwidth, extra capacitances are inserted into the first stage and the third stage. The frequency of each stage is derived as

$$\omega_n = \sqrt{\frac{LC_{j0}A_j + LC_{xn}\left(1 + V_R/\Phi\right)^{mj}}{\left(1 + V_R/\Phi\right)^{mj}}}, \quad (2)$$

where C_{xn} is the extra capacitance added to the nth stage, the other parameters are as the same as in (1). The optimum numbers found for these capacitors are: C_{x1} = 35 fF, C_{x2} = 0, and C_{x3} = 25 fF. Figure 7 shows the center frequency of each stage with the inserted capacitances. With these values of capacitors, the center frequencies are spacing

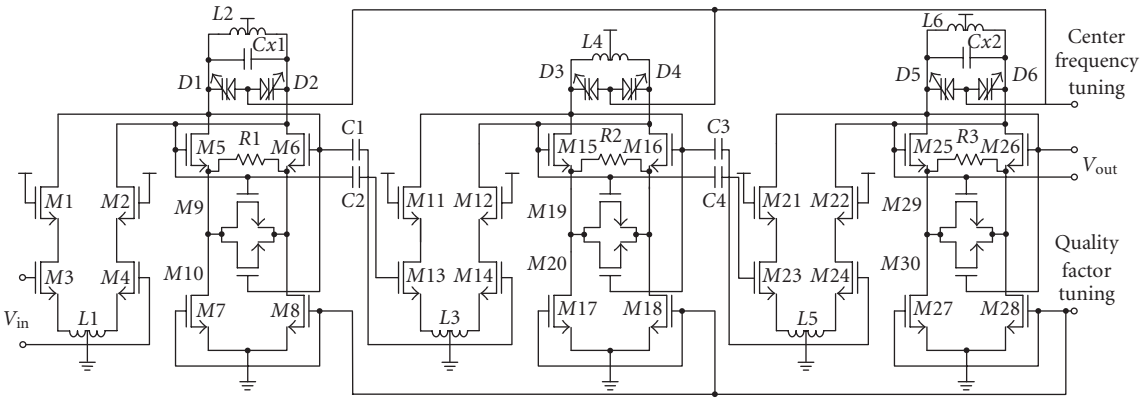

Figure 6: A simplified schematic diagram of the sixth-order BPF (bias circuits are not shown).

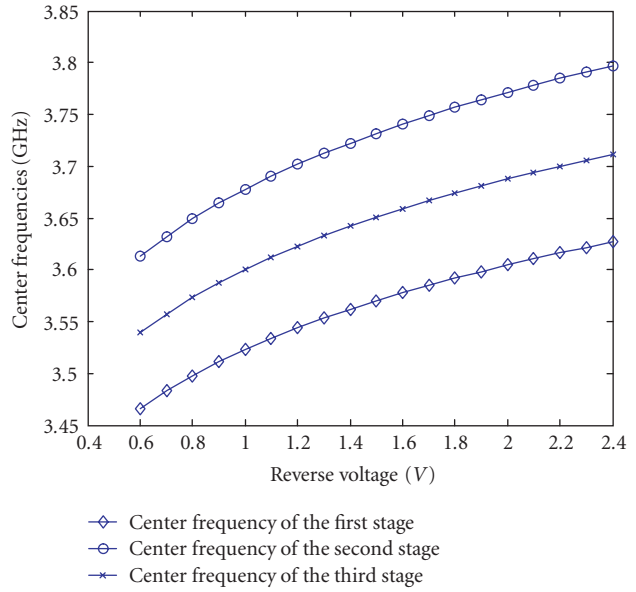

Figure 7: Center frequency of each stage versus tuning voltage.

around 75 MHz. This spacing provides a bandwidth between 100 MHz–150 MHz.

2.5.2. *Quality factor (Q) tuning*

Q tuning in each stage is implemented by changing the current of the cross-coupled transistors ($M5$ and $M6$) in the Q-enhancement circuit of Figure 1(b). This current is controlled by adjusting the bias voltage to transistors. The current changes the transconductance, hence, negative resistance is added into the overall impedance of the tank circuit. In order to make the combined passband ripple as small as possible, Q of the third stage is intentionally designed smaller than Q's of the first two stages by setting the tail currents, Ib, of the three stages to the following ratio: Ib1 : Ib2 : Ib3 = 1 : 1 : 0.8.

Table 2: Component values of the sixth-order bandpass filter.

Symbol	Value
$M1$, $M2$, $M11$, $M12$, $M21$, $M22$	$L = 0.18\,\mu$m, $W = 6 \times 2.5\,\mu$m
$M3$, $M4$, $M13$, $M14$, $M23$, $M24$	$L = 0.18\,\mu$m, $W = 6 \times 2.5\,\mu$m
$M5$, $M6$, $M15$, $M16$, $M25$, $M26$	$L = 0.22\,\mu$m, $W = 8 \times 10\,\mu$m
$M7$, $M8$, $M27$, $M28$	$L = 2\,\mu$m, $W = 6 \times 3.64\,\mu$m
$M17$, $M18$	$L = 2\,\mu$m, $W = 6 \times 4\,\mu$m
$M9$, $M10$, $M19$, $M20$, $M29$, $M30$	$L = 0.22\,\mu$m, $W = 4 \times 6\,\mu$m
$L1$, $L3$, $L5$	2.042 nH
$L2$, $L4$, $L6$	2.042 nH
$D1$, $D2$, $D3$, $D4$, $D5$, $D6$	$5.8\,\mu$m $\times 5.8\,\mu$m $\times 4 \times 7$
$C1$, $C2$, $C3$, $C4$	0.3 pF
Cx1	35 fF
Cx2	25 fF
$R1$, $R2$, $R3$	35 Ω

2.6. *Filter components*

As shown in Figure 6, the filter is implemented by cascading 3 stages of the second-order filter. The stages are coupled with coupling capacitors ($C1$ to $C4$). The LNA is the same in all stages. In order to optimize the gain distribution, the width to length ratios of the current source transistors to the stages are scaled to 1 : 1.1 : 1. Table 2 lists the component values of the designed filter.

2.7. *Linearity consideration*

Linearity of the Q-enhancement circuit is critical because the nonlinearity of this circuit greatly affects the overall filter linearity. There are several techniques to improve linearity. One is to add a source degeneration resistor, Rd, across the cross-coupled transistors of the Q-enhancement circuit [4]. G_m of the modified circuit now becomes

$$G_m = \frac{G_n}{1 + G_n \mathrm{Rd}}. \tag{3}$$

This source resistor reduces G_m, thus, improves circuit linearity. The drawback of this technique is that the resistor

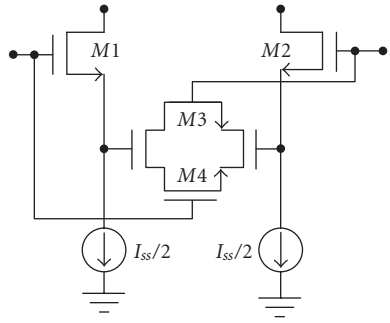

Figure 8: Triode-region biased transistors as a degeneration resistor [13].

consumes a substantial amount of power and degrades noise performance. The other technique is to use transistors biased in their triode regions as shown in Figure 8 in which $M3$ and $M4$ are the source-degenerated resistance [13]. As the input signal increases, the small-signal resistance of one of the two triode-transistors in parallel is reduced. The reduction in resistance attempts to increase transconductance. The action results in a partial canceling of the decreasing G_m value. The transconductance G_m of this modified circuit is derived and expressed as follows:

$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1 + 4k_3)\sqrt{k_1}}, \tag{4}$$

in which k_i is a constant depending on technology and size of the transistors, $k_i = K(W_i/L_i)$.

The designed filter utilizes both linearization techniques as shown in Figure 6 with resistors $R1$, $R2$, and $R3$ and the source-degenerated transistors operating in the triode region: $M9$-$M10$, $M19$-$M20$, and $M29$-$M30$. This design improves filter linearity with the trade-off in power consumption and degradation in noise performance.

3. RESULTS

3.1. Simulation results

All the simulations used the post layout extraction to have realistic parasitic values. Microcircuits of inductor and diode junction capacitor models were used. As shown in Figure 1, the DC voltage at the cathode terminal of the diode is near to the 1.8 V DC supply. The voltage swing in the LC tank is controlled to be under 400 mV. In order to keep the junction away from its forward biasing zone, the tuning voltage is restricted to a maximum of 1.4 V. In the simulation, the frequency tuning voltage is varied from −0.6 V to 1.4 V and the center frequency changed from 3.672 GHz to 3.519 GHz. Figure 9(a) shows simulation results of the center frequency versus tuning voltage. The Q tuning range depends on stability and pass band ripple of the filter. In the simulation, when Q was tuned over 50, the pass band ripple of the filter exceeded 0.5 dB. For a Q over 100, the filter became unstable due to its high gain. The maximum Q tuning range was chosen to be under 50 as shown in Figure 9(b).

Table 3: Simulation results of the sixth-order filter.

Parameter	$Q = 10$	$Q = 30$
Voltage gain	14 dB	30 dB
Noise figure	15 dB	10 dB
IIP_3	−12 dBm	−15 dBm
IP_{-1dB}	−28 dBm	−32 dBm
Image rejection	42 dB	60 dB
Power consumption	105 mW	120 mW

There is a relationship between the tuning of frequency and the Q of the filter. To change frequency, capacitance of the resonator must be adjusted; the changing in capacitance varies quality factor according to the following relationship:

$$Q = \frac{\omega_0}{\mathrm{BW}_{3\mathrm{dB}}} = R\sqrt{\frac{C}{L}}. \tag{5}$$

Therefore, in order to maintain a desired bandwidth, for every shift in frequency, the quality factor needs to be readjusted (i.e., changing R in (5)). Figure 10 illustrates the tuning ability of the filter using a combination of both tunings. For a reasonable high gain, the tuning range is about 140 MHz. When the gain is adjusted too high, the filter exhibits a narrow bandwidth but with an unacceptable ripple.

Figure 11 shows the bandwidth and gain tuning ability of the filter by changing the bias voltage. A bandwidth adjustment between 48 MHz to 125 MHz can be achieved. Figure 12 shows the noise performance of the 3 stages. The LNA affects overall noise figure of the filter. Obviously, as more stages are cascaded, more noise is added into the filter. The minimum noise figure can be achieved is around 14 dB at the target frequency.

Linearity of the filter is simulated using a two-tone test. By applying two sinusoidal signals of equal power P_{in} and different frequencies $f1$ and $f2$ to the filter, the output power spectra P_{out} at frequencies $f1$, $(f2)$, and P_{IM3} at $(2f2 - f1)$ and $(2f1 - f2)$ were measured. By plotting P_{out} and P_{IM3} versus input power P_{in}, the input referenced output 1dB compression point $IP_{1\mathrm{dB}}$ and the input referenced third-order intercept point IIP_3 were obtained. A summary of the simulation results at different Q of the sixth-order filter is listed in Table 3.

3.2. Circuit layout and fabrication

The filter was laid out using Cadence layout tools for Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS technology. This filter was designed for the 1.8 V DC supply. The total chip size is $0.9 \times 0.9\,\mathrm{mm}^2$ including 20 bonding pads. These are power supply, two control voltages for the Q tuning and for the center frequency tuning, analog inputs, and analog outputs. Three RF outputs from 3 stages are provided for testing purposes. Using three outputs, the filter can be used as second, fourth, or sixth order as desired and can be tuned to a narrower bandwidth. Figure 13 shows the layout and micrograph of the fabricated filter; the

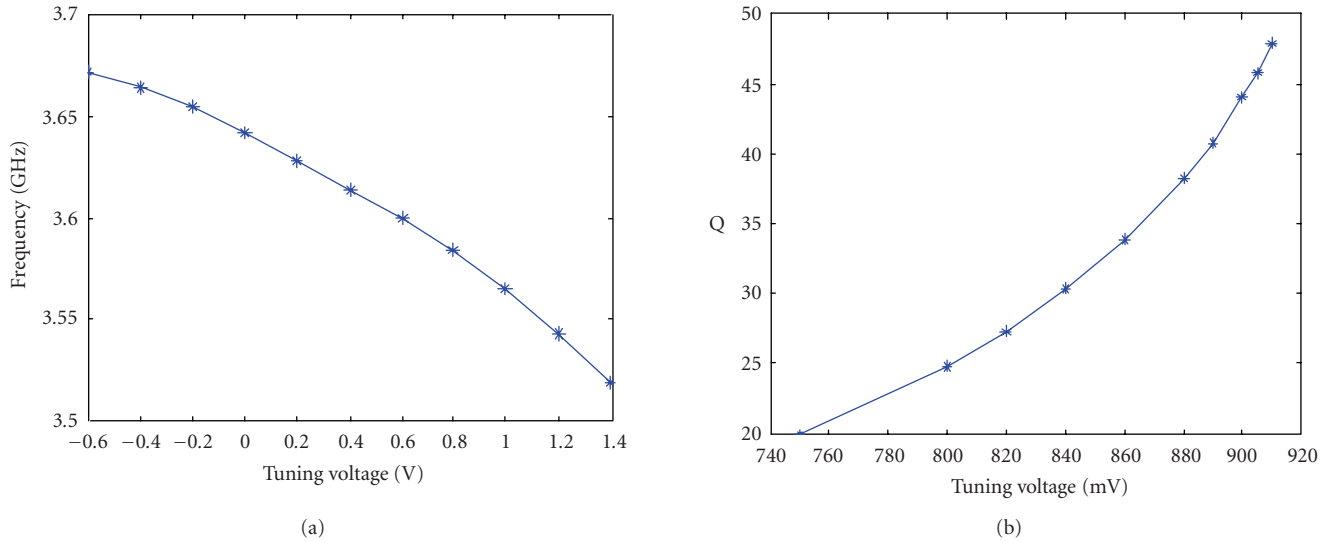

Figure 9: (a) Center frequency versus tuning voltage, (b) Q versus tuning voltage.

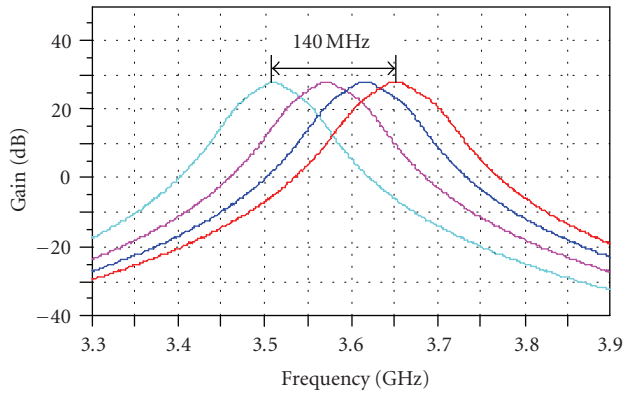

Figure 10: Center frequency tuning ability of the sixth-order filter.

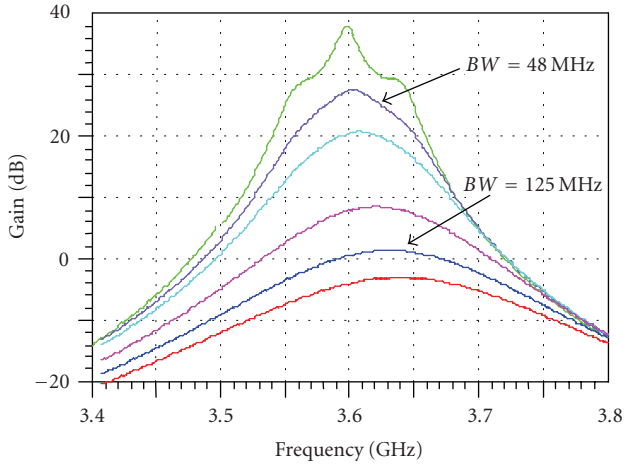

Figure 11: Bandwidth and gain tuning ability of the sixth-order filter.

symmetry layout and the surrounding power rings are clearly shown.

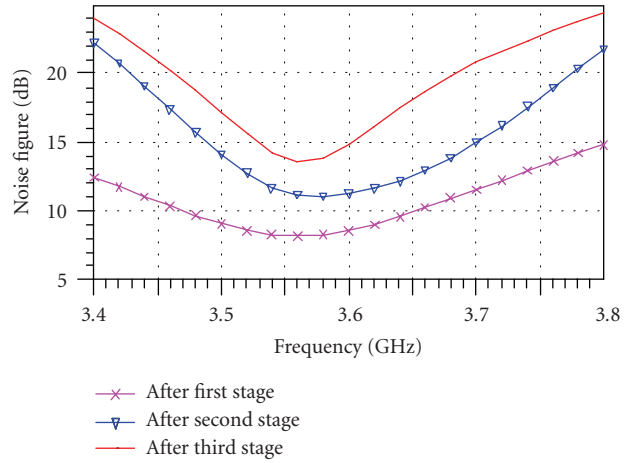

Figure 12: Noise performance at different stages of the filter.

3.3. Testing results

The IC was tested using the HP 8722 ES/ET microwave network analyzer and a spectrum analyzer. The filter was mounted on a PCB with appropriate supply and tuning voltages. The device under test was considered as a two-port network to measure its parameters. To determine frequency tuning range of the filter, the frequency tuning voltage was varied between −0.6 V to 1.2 V and the results were plotted and shown in Figure 14. The tuning of Q was required in this test in order to maintain the same bandwidth for every frequency setting. The frequency tuning is 300 MHz (3.54 GHz–3.88 GHz) which is much larger than the simulated result of 140 MHz. The difference may come from the inaccuracy of the varactor model and over-estimation of the fixed parasitic capacitances.

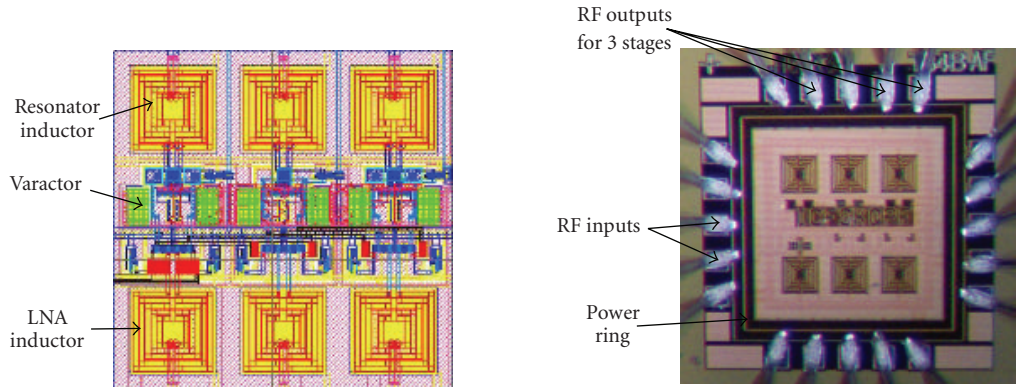

Figure 13: (a) Filter layout, (b) chip micrograph.

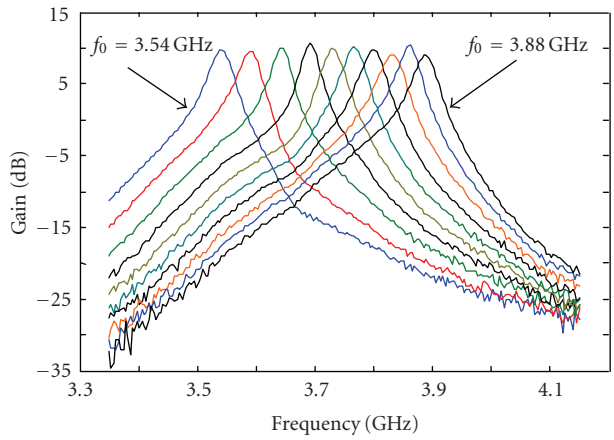

Figure 14: Frequency tuning measurement.

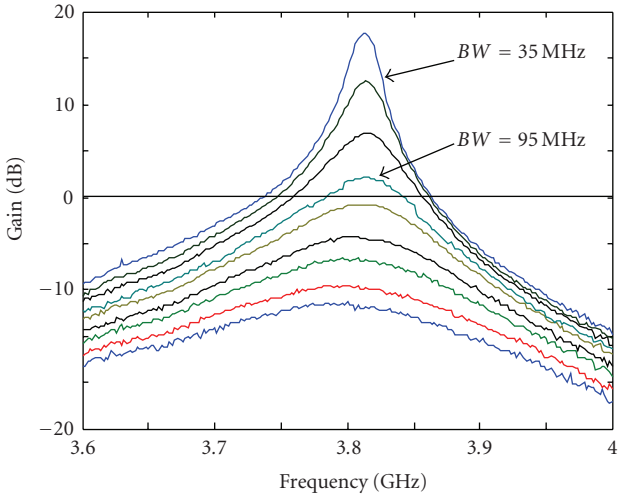

Figure 15: Bandwidth tuning ability measurement.

To determine the bandwidth tuning ability of the filter, frequency responses under different Q tuning voltages were measured and shown in Figure 15. The bandwidth of this filter can be tuned between 35 MHz to 95 MHz to be usable at its maximum center frequency of 3.8 GHz. This comes short from the simulated values of 48 MHz–125 MHz. By measuring the reflection coefficient, the input matching was determined and found to have a perfect match around 3.8 GHz. The other measurement results are reported in Table 4.

Table 4: Measured and simulated results of the sixth-order filter.

Parameters	Specification	Simulation	Measurement
Center frequency (GHz)	3.6	3.6	3.67
Gain (dB)	—	0–30	0–18
Frequency tuning range (GHz)	—	3.51–3.65	3.54–3.88
Bandwidth (Q tuning) (MHz)	100	48–125	35-95
IIP3 (dBm)	> -30	-29.5	-29
1 dB compr. (dBm)	> -45	-44	-33.5
Dynamic range (dB)	> 45	45.1	46.5
Image rejection at 500 MHz away ($-$dB)	> 50	50	50
NF (dB)	15	14.9	15.5
Power consumption at 1.8 V (mW)	—	117	130

A comparison of this design to previously reported works on on-chip bandpass filters is given in Table 5. The filter in this work uses the most advanced CMOS technology. As indicated, this filter operates at the highest frequency using the lowest supply voltage. In addition, both frequency and bandwidth are tunable while majority of the filters have both values fixed or self-tuned. The designed features of this filter provide an easy interfacing of the tuning signals for frequency and bandwidth adjustments. The designed inductor has the best Q among some of the previous designs. However, this filter consumes more power than the other filters

Table 5: A comparison of this design to other publications.

Parameters	[5]	[15]	[16]	[17]	[14]	This work
Year	1998	2001	2002	2003	2005	2003
Filter order	4	4	6	4	1	6
Center frequency (GHz)	0.85	1.9	2.1	1.8	2.45–2.85	3.54–3.88
Passband gain (dB)	0	0	0	9	23	0–18
Ripple in passband (dB)	< 2	1.6	0.7	< 0.5	N/A	< 1
Bandwidth (MHz)	18	150	60	80	70	35–80
Q of inductor	< 3	N/A	N/A	2.7	N/A	4.9
Dynamic range (dB)	61	63	63	42	142	46.5
1-dB compression (dBm)	−46	—	−13.4	−26	−15	−33.5
Current drain/pole (mA)	19.25	4.5	1.17	4	5	12
Supply voltage (V)	2.7	2.7	2.5	2.7	3	1.8
Technology (μm)	0.8 CMOS	0.25 Bi-CMOS	0.25 CMOS	0.5 CMOS	SOI CMOS	0.18 CMOS

listed in Table 5. For example, it uses 22 mW/pole compared to 15 mW/pole in [14]. Majority of the power is consumed by the 3 linearization resistors $R1$, $R2$, and $R3$ in Figure 6. This is a trade-off between power consumption and linearity. Another trade-off for a better linearity is the increase in NF of this design (15 dB) while the filter in [14] obtains an NF of 7 dB as the resistors in this filter are the sources of noise. In overall, the designed filter uses a simple tuning scheme for a wide bandwidth and achieves higher image rejection, larger tuning range, and much higher linearity compared to other filters.

4. CONCLUSIONS

A tunable bandpass filter was designed using the main stream 0.18 μm CMOS technology at the 3.6 GHz range. Three second-order filters were cascaded to form a sixth-order filter to have higher image rejection and wider bandwidth. The bandwidth and center frequency of the filter are tunable using a simple tuning scheme for practical applications. An innovative method was employed to set apart the center frequencies of the stages in order to obtain a wider bandwidth and a single voltage was used to tune all 3 stages. In addition, the bandwidth tuning requires only a single tuning voltage. The tuning scheme greatly simplifies the filter and makes it more applicable to commercial applications. The design employed inductive degeneration technique to minimize the noise at the input stage. Careful layout and design techniques were employed to develop better quality inductors in the CMOS technology. The causes of poor circuit linearity were identified and corrected to improve the filter performance. Test results show the frequency deviation and the inaccuracy of the tuning range in the fabricated filter compared to the simulation results. These errors may come from the inadequate accuracy in modeling of the inductors and varactors. This design shows new achievements in this research field: 3.6 GHz BPF using standard CMOS, high quality inductor, tunable center frequency and bandwidth, and high image rejection for a high gain filter. However, this filter suffers high-power consumption compared with other filters designed in the past because of the use of resistors to improve linearity; this problem must be fixed for portable applications. The tunable ability of the design seems useful to be investigated further for the feasibility of using this feature as a channel-select filter.

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