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Research Article

Performance Analysis of Trench Power MOSFETs in High-Frequency Synchronous Buck Converter Applications

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This paper investigates the performance perspectives and theoretical limitations of trench power MOSFETs in synchronous rectifier buck converters operating in the MHz frequency range. Several trench MOSFET technologies are studied using a mixed-mode device/circuit modeling approach. Individual power loss contributions from the control and synchronous MOSFETs, and their dependence on switching frequency between 500 kHz and 5 MHz are discussed in detail. It is observed that the conduction loss contribution decreases from 40% to 4% while the switching loss contribution increases from 60% to 96% as the switching frequency increases from 500 KHz to 5 MHz. Beyond 1 MHz frequency there is no obvious benefit to increase the die size of either SyncFET or CtrlFET. The $R_{DS(ON)} \times Q_G$ figure of merit (FOM) still correlates well to the overall converter efficiency in the MHz frequency range. The efficiency of the hard switching buck topology is limited to 80% at 2 MHz and 65% at 5 MHz even with the most advanced trench MOSFET technologies.

1. INTRODUCTION

Trench powerMOSFETsare widely used as both control and synchronous rectifier switches (CtrlFET and SyncFET) in buck converters for computer, telecommunication, and consumer applications [1–5]. Power MOSFETs usually account for most of the power losses, and often determine the overall efficiency of today's DC/DC converters. Over the past decade, the power semiconductor industry has significantly improved MOSFET performance, especially in terms of the figure of merit (FOM) of $R_{DS(ON)} \times Q_G$ [6, 7]. The analysis, modeling, and optimization of power MOSFET performance in synchronous buck converters have also become the focus of a significant amount of research work in the past few years [8–12]. The objective is to identify the optimum design of the CtrlFETs and SyncFETs that offer the highest converter efficiency. The previous work addressed this goal with varied levels of success, but several issues still remain open especially in light of ever-evolving DC/DC converter design requirements.

The $R_{DS(ON)} \times Q_G$ FOM is generally considered as the single most important indicator of MOSFET performance in DC/DC converters in the medium switching frequency range of 100 kHz to 1 MHz. As the switching frequency of buck converters increases to the MHz range to facilitate better converter transient response and smaller passive components, it is, however, not clear how closely the $R_{DS(ON)} \times Q_G$ FOM correlates to the overall converter efficiency, or whether or not a different FOM needs to be defined. Furthermore, the analysis on individual MOSFET power loss contributions, namely, conduction loss of the CtrlFET, conduction loss of the SyncFET, switching loss of the CtrlFET, diode loss of the SyncFET, and gate-drive losses of both the CtrlFET and SyncFET, was previously limited to the use of simple analytical equations based on approximations and assumptions [4, 8, 9, 11, 13]. These simple device models have only very limited accuracy [14]. More importantly, they are not capable of revealing or predicting the influence of variations in device structures or circuit operating conditions on each of the individual power loss terms. This is the essential

knowledge required for developing future generation power MOSFETs for high-efficiency and high-density buck converters. Lastly, the scope of the previous work on power MOSFET performance analysis was limited to the study of either one particular power MOSFET technology [4] or just a limited number of commercial parts [5, 15]. While offering useful information on how to select commercially available power MOSFETs for today's practical converter design, the previous work does not sufficiently address the perspectives and theoretical limitations of power MOSFET technology for future generation DC/DC converters operating with ever-increasing switching frequency, slew rate, and output current.

The purpose of this paper is to comprehensively investigate the performance perspectives and theoretical limitations of trench power MOSFET technology in synchronous rectifier buck converters over a wide range of operating conditions [16]. The MOSFET device structures under investigation include but are not limited to those manufacturable with today's semiconductor fabrication technology. The investigation was carried out with a mixed-mode device/circuit simulation approach. Device measurement data was also used to validate the physical device models. Various power loss contributions from the CtrlFETs and SyncFETs at different operating conditions were studied in detail. Several important observations were made which may shed some light on the development of future generation power MOSFETs, as well as the optimal utilization of today's power MOSFETs in buck converter applications.

2. METHODOLOGY

Although the efficiency of a buck converter is usually determined by directly measuring its input and output power, such an experimental approach proves very difficult to employ to characterize the individual power loss terms of the control and sync FETs in the converter. The actual current waveforms, and to a less extent, the voltage waveforms, of the power MOSFETs in a high-current, high-slew rate DC/DC converter are most likely disturbed by the measurement setup such as current probe loops, resulting in large distortions and measurment errors. The limited sampling rate of digital oscilloscopes often introduces some measurement errors as well. Modeling analysis approaches provide an alternative way of investigating power MOSFET performance in buck converters.

The previous work on power MOSFET performance analysis used simple analytical device models to calculate $R_{DS(ON)}$, Q_G, and other device parameters, and a set of simple analytical equations for power loss calculation [4, 8, 11, 13]. While these approaches provide a quick first-order estimation of converter efficiency, its accuracy is inevitably limited by the approximation and simplification made in the analytical models. Recently, Cavallaro et al. used a circuit simulator to estimate buck converter power losses using MOSFET behavior models which were derived from two-dimensional numerical device and process simulation [9]. It should be pointing out that the accuracy of converter power losses can be further improved by using a mixed-mode

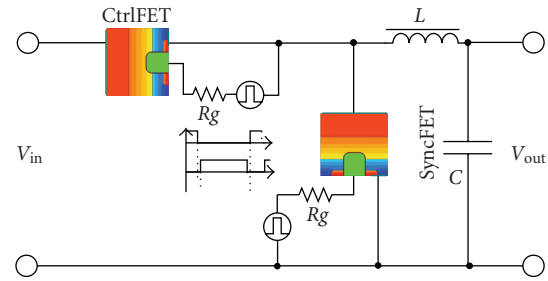


Figure 1: Mixed-mode DESISS simulations for DC/DC converter with numerical power MOSFET models.

device/circuit simulation approach with numerical MOSFET models being directly incorporated into circuit simulation. Furthermore, detailed information on various power loss contributions of the CtrlFETs and SyncFETs over a wide range of operating conditions can be easily obtained from the mixed-mode simulation.

In this paper, we used a physically based mixed device/circuit modeling approach to investigate the power losses of the MOSFETs under different operating conditions. "Virtual" power MOSFETs were first built using a two-dimensional numerical device simulation TCAD tool-DESSIS from Synopsis [17], and then placed into a 12 V-to-1 V, 20 A buck converter circuit for mixed-mode device/circuit simulation. Figure 1 depicts the concept of this approach. DESSIS numerically solves the Possion's equation, the continuity equations of electron and hole currents self-consistently, using a variety of physical models. It can be used to predict the electrical characteristics of arbitrary two- or three-dimensional semiconductor structures under user-specified operating conditions. It also offers SPICE-like circuit simulation capability combined with device numerical modeling capability, and provides a quick and inexpensive way of evaluating and optimizing circuit and device concepts. Unlike analytical or other SPICE models of power MOSFETs, the numerical device model, relying little on approximations or simplifications, faithfully represents the behavior of a realistic power MOSFET, and provides physical insights on device operation. Note that while this mixed device/circuit modeling method is suitable for our study of power MOSFET losses, it is not convenient to use for general circuit design purposes.

3. MODELING OF BASIC TRENCH POWER MOSFET

A basic trench MOSFET structure with a cell pitch of 2.5 μm is shown in Figure 2. To accurately reproduce the behavior of the trench MOSFETs in real circuit operation, we have carefully chosen the physical models and model parameters used in DESSIS simulation, such as carrier mobility and lifetime. The trench MOSFET model was validated by comparing to measurement data of real devices. Table 1 shows the electrical parameter comparison between the "virtual" trench power MOSFET and its real world counterpart. Reasonable agreement is observed.

Table 1: Comparison of simulated and measured electrical parameters of the basic trench power MOSFET.

Device parameters	Basic trench MOSFET	
	Modeled (type A)	Measured (IR6618)
BV_{DSS} @250 μA (V)	36.4	33
V_{TH} @250 μA (V)	1.35	1.7
$R_{DS(on)}$ @4.5 V (mΩ)	2.3	3.2
Q_G @4.5 V/15 V (nC)	43	45
Q_{GD} @15 V (nC)	15	15
Q_{rr} @100 A/μs (nC)	33.5	46

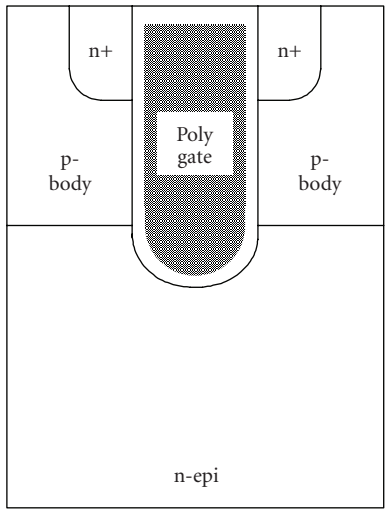


Figure 2: A basic trench power MOSFET structure (type A).

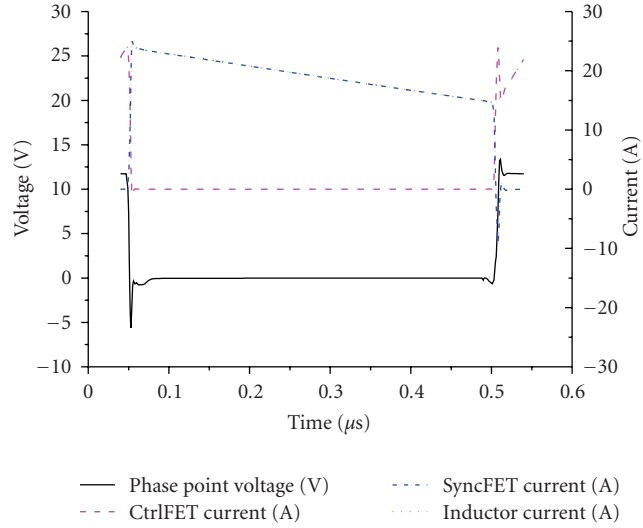


Figure 3: Switching waveforms at 2 MHz switching frequency.

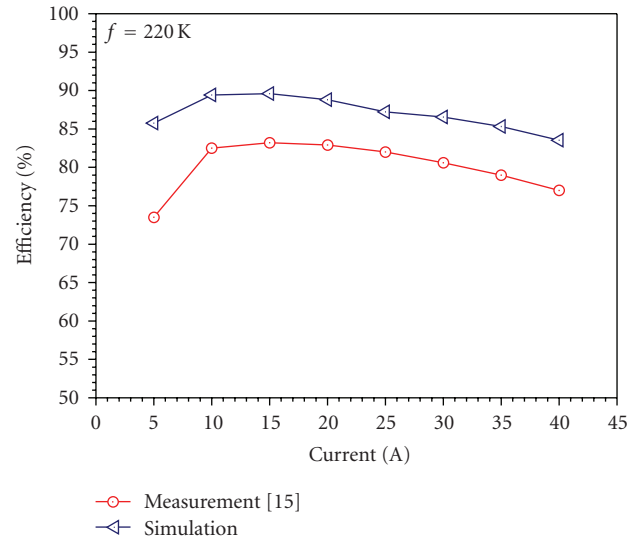


Figure 4: Load versus efficiency at 220 kHz switching frequency.

After the completion of MOSFET phsical models validation, a chip set ofvirtualCtrlFET and SyncFET is incorporated into the mixed-mode simulation of a buck converter circuit with an input voltage of 12 V and an output voltage and current of 1 V and 20 A, respectively, in Figure 1. The duty cycle of the buck converter was carefully adjusted to maintain the 1 V/20 A output. An $R_{DS(ON)}$ ratio of 4.3 was chosen between the CtrlFET and SyncFET. The issue of optimizing this $R_{DS(ON)}$ ratio is to be discussed in Section 5.

Figure 3 shows the typical switching waveforms of the simulated buck converter at a switching frequency of 2 MHz, which are very similar to typical measurement waveforms. In this paper, we define the individual loss terms as follows: CtrlFET conduction loss, SyncFET conduction loss, CtrlFET turn-on loss, CtrlFET turn-off loss, SyncFET body-diode loss, CtrlFET gate-drive loss, and SyncFET gate-drive loss.

Figures 4 and 5 compare the simulated and experimental converter efficiency as a function of the load current at the switching frequency of 220 kHz and 410 kHz, respectively. In this paper, we focused on the active component power dissipations, which account for 60%–90% of the total power loss in buck converters depending on operation conditions [15]. The power losses introduced by passive components like inductors and capacitors, often counting for 20–30% of total loss, are not included in our simulation study. At 220 kHz, the simulated efficiency is about 6.5% higher than the measured efficiency. The power losses introduced by the passive components contribute to this efficiency difference. The simulation results show the same trend as the measurend results in all load current range even with the difference due to the passive parasitics. The comparison between the simulation and experiment data at a switching frequency of 410 kHz also provides further validation of this methodology.

The mix-mode simulation also allows us to analyze individual power loss contributions of both SyncFET and CtrlFET in addition to converter overall efficiency. Figure 6 shows the individual loss terms of the MOSFETs at operating frequencies of 0.5, 1, 2, 5 MHz. We also compare the relative

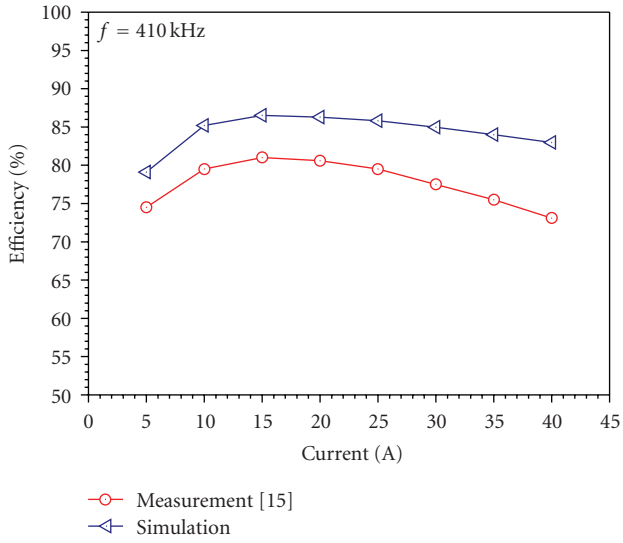


Figure 5: Load versus efficiency at 410 kHz switching frequency.

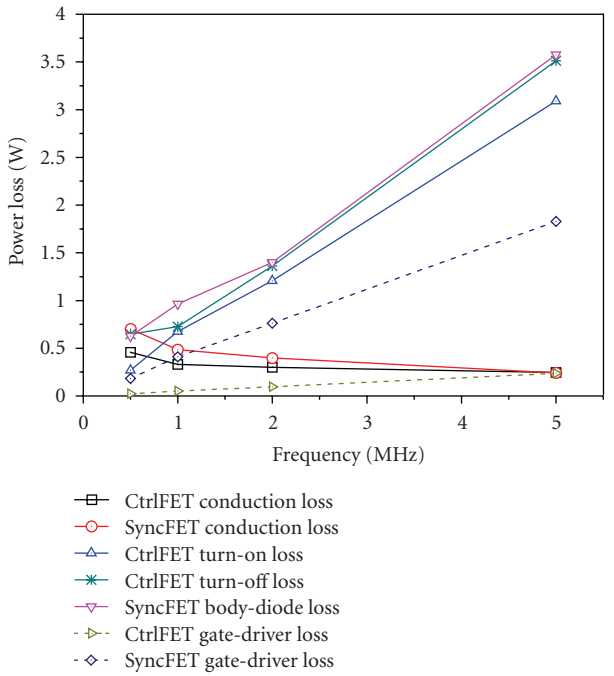


Figure 6: Individual power-loss terms versus switching frequency.

contribution of each power loss term at the switching of 0.5 MHz and 5 MHz at Figure 7. The following are observed.

(I) The gate-drive loss of the SyncFET becomes significant beyond 2 MHz operating frequency. At 5 MHz, the gate-driver loss is about 2 W, or roughly 14% of the total power loss.

(II) Conduction losses remain constant independent of switching frequency, and count for a small percentage of the total power loss in the MHz frequency range. At 0.5 MHz, the conduction losses account for 40%

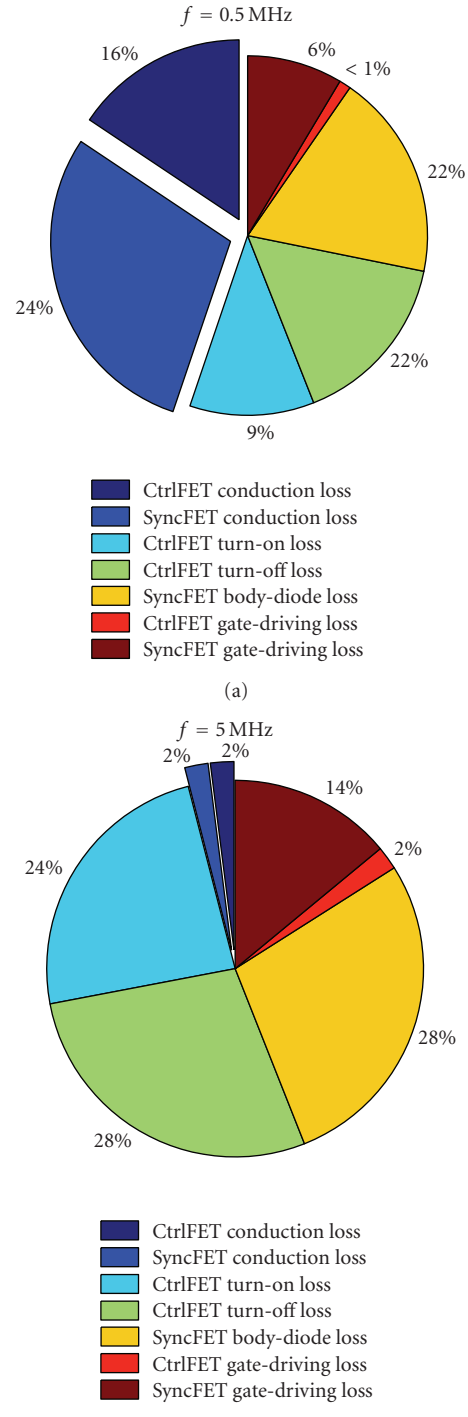


Figure 7: Contribution of power losses at switching frequency: (a) 0.5 MHz; (b) 5 MHz.

of total power loss, while they only account for 4% of total power loss at a switching frequency of 5 MHz.

(III) CtrlFET switching loss and SyncFET body-diode loss dominate the total power loss in the MHz frequency range, accounting for roughly 52% and 26% of the total power loss at 5 MHz. For the switching

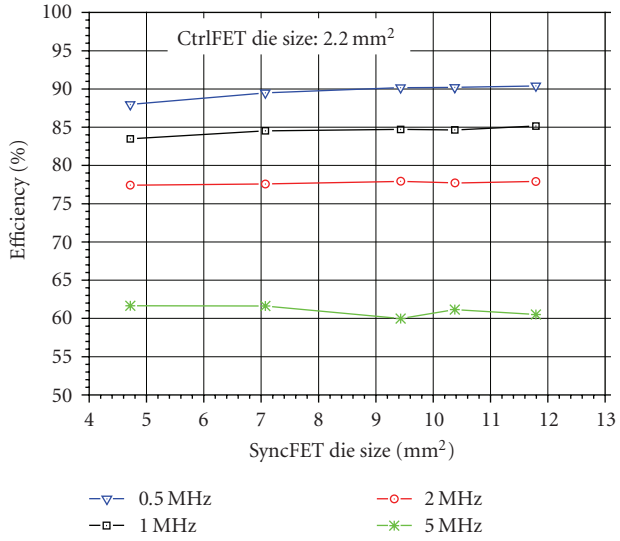


Figure 8: Converter efficiency as a function of the SyncFET die size.

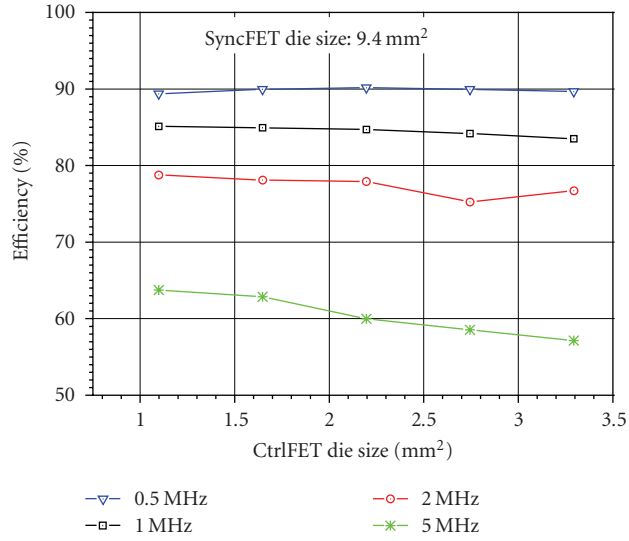


Figure 9: Converter efficiency as a function of the CtrlFET die size.

frequency of 0.5 MHz and 5 MHz, the total switching losses account for 60% and 96% of total power losses, respectively.

Since the individual loss terms are dependent on the sizing of both the CtrlFET and SyncFET [4]. Next, we will focus on the optimal sizing of CtrlFETs and SyncFETs for buck converter efficiency.

4. OPTIMAL SIZING OF CONTROL AND SYNCHRONOUS RECTIFIER MOSFETs

Selection of large-size MOSFETs may not necessarily lead to efficiency improvement since the MOSFET switching and gate-drive losses increase with increasing die size even though the conduction losses are reduced. Silicon cost is yet another factor that needs to be considered in MOSFET sizing. An optimal size exists for both the CtrlFETs and SyncFETs to provide a minimum total power loss.

Figure 8 shows the converter efficiency as a function of the die size of the SyncFETs given a fixed CtrlFET die size of 2.2 mm^2 at various switching frequencies. The direct observation is that there is no any efficiency benefit by incresing SyncFET die size as frequency beyond 2 MHz. For lower-frequency range, the SyncFET die size increase introduces subtle efficiency increase, which is very cost-consuming. For example, at 0.5 MHz, the increase of die size about 2.6 times just results in 2.5% efficiency improvement. For the frequency higher than 2 MHz, such as 5 MHz, the die size increase, in fact, introduces efficiency degradation. Figure 10 illustrates the individual loss terms at different frequencies, which helps to explain the above observations. The switching losses dominate at MHz frequency range, which increases when the switching frequency increases. As the die size increases, the conduction loss decrease is easily overshadowed by the increase of switching losses. This effect is even more significant for the CtrlFET die sizing. As Figure 9 shows that beyond 1 MHz frequency there is

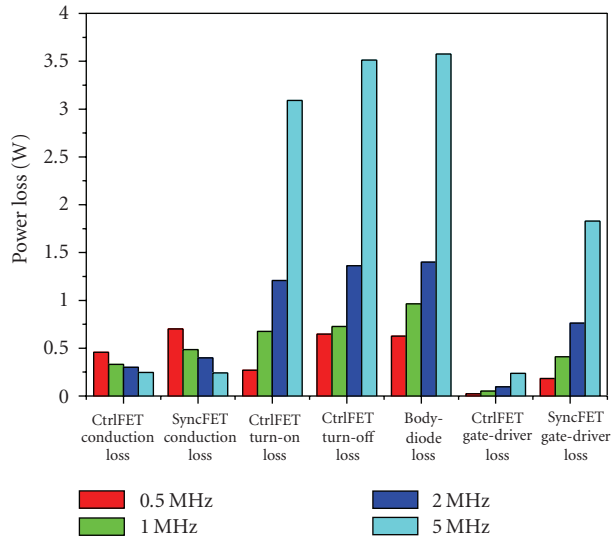


Figure 10: Individual loss-term comparison over 0.5 to 5 MHz.

already no benefit to increase CtrlFET die size. At 5 MHz, the increased die size introduces 7% efficiency degradation.

In this specfic case, for a fixed die size of 2.2 mm^2 of the CtrlFET, the optimal size of the sync-FET decreases from 11.8 mm^2 to 4.8 mm^2 when the switching frequency increases from 500 kHz to 5 MHz, indicating the increasing weight of switching losses at higher switching frequencies. The die size of 9.4 mm^2 seems to be a good choice for the SyncFET over the frequency range of 500 kHz to 5 MHz. For a fixed die size of 9.4 mm^2 for the SyncFET, the optimal size of the CtrlFET is about 1.1 mm^2. The increase in die size beyond 3.3 mm^2 only results in less than 1% improvement in efficiency at 0.5 MHz, making 1.1 mm^2 a good choice for the CtrlFET.

Furthermore, as shown in Figures 8 and 9, an optimum range instead of a single maximum point of MOSFET die size

Table 2: Comparison of trench power MOSFET technologies.

Type	Area factor	Ron (mΩ)	Ciss (pF)	Coss (pF)	Crss (pF)	Q_{rr} (nC)	Q_G (nC)	Q_{GD} (nC)	Ron*Q_G (mΩ*nC)	Ron*Q_{GD} (mΩ*nC)
Base structure (A)	1	9.4	1263	234	144	31.992	13.587	5.0	127.718	47
Thick bottom (B)	1.04	9.4	1230.8	212.2	109.2	28.14	10.505	4.2	98.747	39.48
Floating poly plug (C)	1.138	9.4	1410.3	227.3	118.9	36.296	11.7	4.5	109.98	42.3
Narrow trench (D)	1.106	9.4	1303	233	106.9	33.097	12.2	5.1	114.68	47.94
High density (E)	0.622	9.4	1546	126	105	18.096	13.685	4.8	128.639	45.12
Low density (F)	1.94	9.4	1318	428	240	57.257	19.24	11.3	180.856	106.22

exists to offer a maximum converter efficiency. If 1% or less efficiency degradation is acceptable, the size of the MOSFETs can be significantly reduced to reduce MOSFET costs. This is especially true at higher switching frequencies where the size of the SyncFETs and CtrlFETs can be reduced almost by 50%.

5. COMPARISON OF VARIOUS TYPES OF TRENCH MOSFETs

A number of structural variations of the trench power MOSFET technology have been developed or proposed in the past decade as shown in Figure 11. In this seciton, we conduct performance analysis on several advanced trench MOSFET structures. This may shed some light on how to improve future power MOSFET design. Note that some of these device concepts are still in research stage instead of full-scale production. We have included these device structures into our study to address the issue of performance perspectives and theoretical limitations of both today's and future generation trench power MOSFET technologies in synchronous rectifier buck converters over a wide range of operating conditions, especially in the MHz frequency range.

Figure 11(a) shows a trench MOSFET structure with a thickoxide layer at the bottom of the trench to minimize Q_{GD} [3, 18]. Figure 11(b) shows a trench MOSFET cell with an ultranarrow trench width to minimize Q_{GD} by reducing the effective gate-drain overlap area [2]. Figure 11(c) illustrates a trench MOSFET structure with a floating poly shield below the gate polysilicon trench refill [19]. The objective of these advanced trench MOSFET concepts is to further improve the $R_{DS(ON)} \times Q_G$ FOM. In order to obtain a reasonable comparison between different technologies, the above structures have the same pitch size as the basic trench power MOSFET. Figures 11(d) and 11(e) show a high-density trench MOSFET cell with a cell pitch of half of the basic structure [1] and a low-density trench MOSFET with a double cell pitch size of the basic structure, respectively.

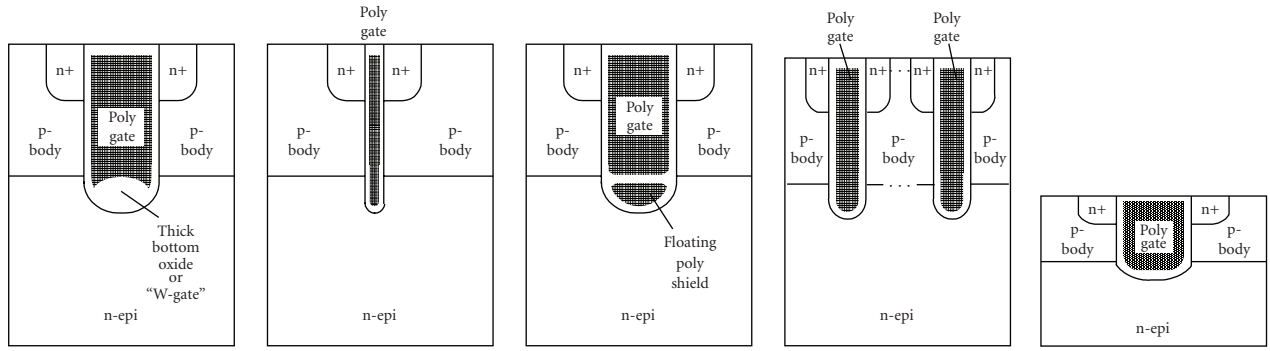
Table 2 lists the major device parameters of all SyncFETs being scaled to have the same $R_{DS(ON)}$ of 9.4 mΩ. To obtain this requirement, different die sizes are used for different technologies as shown in Table 2. It is observed that only the high-cell density MOSFET technology (Type E) significantly reduces specific $R_{DS(ON)}$ at the expense of a large increase in both specific Q_G and FOM of $R_{DS(ON)} \times Q_G$. Type E also provides the minimum Q_{rr} among all the MOSFET technologies because less die size is requred to maintain the same $R_{DS(ON)}$. The thick bottom oxide (Type B) achieves the highest FOM, which effectively reduce the specific $Q_G(Q_{GD})$ with only a subtle specific $R_{DS(ON)}$ penelty. The floating poly-plug MOSFET structure (Type C) reduces specific Q_{GD} with a penalty on specific $R_{DS(ON)}$. The narrow trench MOSFET (Type D) effectively improves the FOM compared with the basic structure, but does not provide much benefit compared with Types B and C. The low-density MOSFET (Type F) obviously has the worst FOM. It can be predicted that Type F has the worst performance among all these technologies.

A ratio 4.3 : 1 is assumed between the SyncFET and CtrlFET for all the trench MOSFET technologies. All six chip sets of the "virtual" trench MOSFETs listed in Table 2 are evaluated in the 12 V-input, 1 V/20 A-output buck converters. It is assumed that the CtrlFET and SyncFET are fabricated using the same device technology in our current study even though it is possible or perhaps even advantageous to mix trench and lateral MOSFETs in the buck converter chip set.

Figure 12 compares the full load converter efficiency among the six MOSFET technologies at various switching frequencies. As we predicted, the low-density chip set provides worst efficiency performance over the whole frequency range. The thick bottom chip set offers the best performance in MHz frequency range. As shown in Table II, the thick bottom MOSFET has the lowest Q_{rr} and Q_{GD} for the same $R_{DS(on)}$. At 5 MHz, the thick bottom chipset provides 10% higher efficiency than the low-density chipset.

We also compare the individual power loss terms of these two chip sets at a switching frequency of 2 MHz in Figure 13 to further discuss the large difference in efficiency. The conduction losses of both CtrlFET and SyncFET are almost the same as they have the same $R_{DS(on)}$ while there is a large difference in the switching losses due to the difference in the Q_{rr} and Q_G parameters. It is well known that a smaller Q_G provides faster switching speed. With the thick bottom and the low-density MOSFETs exhibiting a Q_G of 10 nC and 20 nC, respectively, the thick bottom MOSFET has much smaller CtrlFET turning-off loss, which is directly proportional to the switching speed.

Smaller Q_G also offers smaller gate-driver power loss. This is also observed in Figure 13. The low-density chip set requires much larger gate-driver power losses. At even higher frequencies, the gate-driver power requirement will be a major problem. Smaller Q_G will definitely be required.



(a) Thick bottom oxide (b) Ultranarrow trench (c) Floating poly plug (d) High-cell desity (e) Low-cell desity

Figure 11: Various trench power MOSFET structures: (a) Type B: thick-bottom-oxide design; (b) Type C: ultranarrow trench design; (c) Type E: floating-polyplug design; (d) Type E: high-cell density design; (e) Type F: low-cell density design.

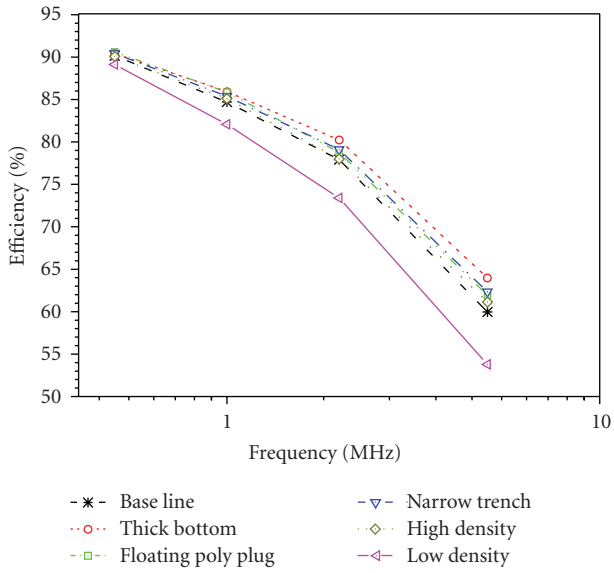


Figure 12: Efficiency versus switching frequency for different trench MOSFET technologies.

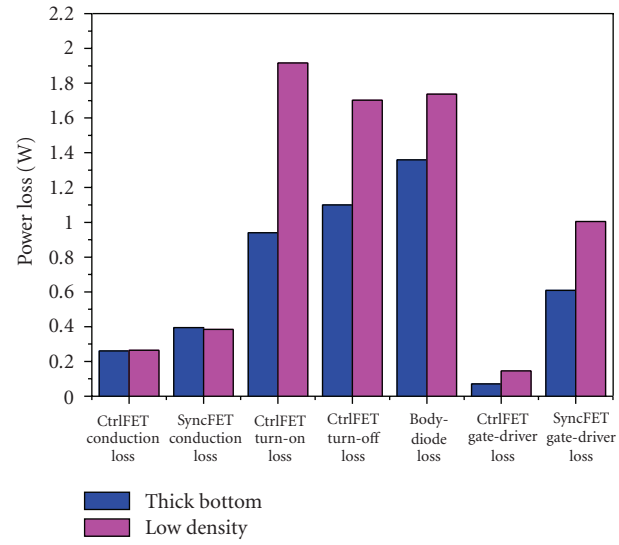


Figure 13: Efficiency versus switching frequency for different trench MOSFET technologies

The reverse recovery of the body diode of the SyncFET induces not only the loss on the body diode of SyncFET itself but also the turn-on switching loss of the CtrlFET. The thick bottom SyncFET has a 28 nC Q_{rr} while the low-density SyncFET has 58 nC Q_{rr}. As shown in Figure 13, the body-diode loss of the thick bottom SyncFET is lower than its low-density counterpart.

Considering the CtrlFET turning-on loss, the large difference between the two types of MOSFETs is due to the difference in both Q_{rr} and Q_G parameters. Larger Q_{rr} of the low-density MOSFET introduces larger reverse recovery loss, and its larger Q_G introduces larger switching loss as shown in Figure 13.

It should be noted that smaller Q_G may not always lead to overall performance improvement of the buck converter. As the gate charge of the trench power MOSFET being further reduced with new fabrication technology, the turn-on current slew rate *di/dt* of the CtrlFET may further increase, resulting in an increase in the reverse-recovery current of the SyncFET body diode, and subsequently an increase in the turning-on switching power loss of the CtrlFET and the body-diode loss of the SyncFET. Under certain circumstances, the reduction of gate charge of the MOSFET becomes counter-productive, and leads to higher switching power losses.

The $R_{DS(ON)} \times Q_G$. FOM is generally considered as the single most importantindicator of MOSFET performance in DC/DC converters in the medium switching frequency range of 100 kHz to 1 MHz. As the switching frequency of buck converters increases to the MHz range to facilitate better converter transient response and smaller passive components, it is, however, not clear how close the $R_{DS(ON)} \times Q_G$ FOM correlates to the overall converter efficiency, or whether or not a different FOM needs to be defined. Figure 14 shows DC/DC converter efficiency as a function of FOM of $R_{DS(ON)} \times Q_G$ at 1, 2, and 5 MHz switching frequency.

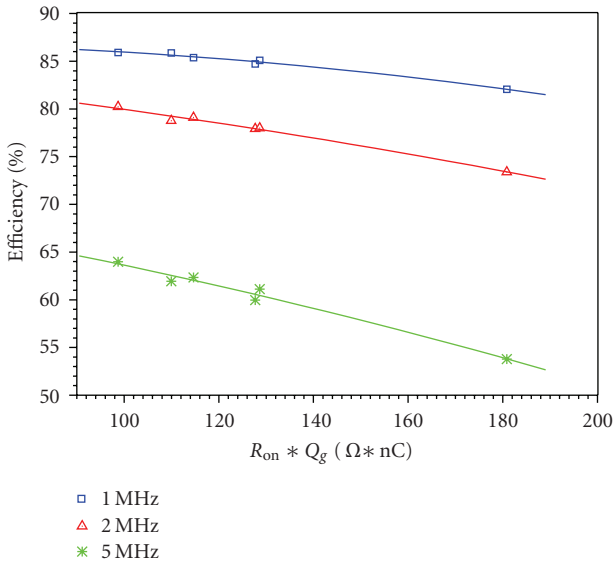


FIGURE 14: FOM $R_{DS(ON)} \times Q_G$ of trench power MOSFETs.

Different data points in Figure 14 may represent different trench MOSFET technologies. The $R_{DS(ON)} \times Q_G$. FOM seems to correlate well with the converter efficiency even in the MHz operating frequency range.

6. CONCLUSIONS

In this paper, we have comprehensively investigated the performance perspectives and theoretical limitations of trench power MOSFETs in synchronous rectifier buck converters over a wide range of operating conditions. Several trench MOSFET technologies are investigated using a mixed-mode device/circuit modeling approach. Individual power loss contributions from the CtrlFETs and SyncFETs and their dependence on switching frequency between 500 kHz and 5 MHz are discussed in detail.

It is observed that going from 0.5 MHz to 5 MHz, the conduction loss contribution decreases from 40% to 4% while the switching loss contribution increases from 60% to 96%. Under hard switching operation condition, the buck converter efficiency is limited to 80% at 2 MHz and 65% at 5 MHz even with the most advanced trench MOSFET technology.

For the base technology we studied, beyond 1 MHz frequency, there is no obvious benefit to increase the die size of either SyncFET or CtrlFET. For 5 MHz, given a constant die size of SyncFETs, the die size increase of CtrlFETs actually introduces obvious efficiency degradation.

For different trench technologies, the technology,which has the lowest Q_G, provides smallest gate-driver losses and the smallest CtrlFET turning-off losses. On the other hand, smaller Q_G gives faster switching transition, which may introduce larger reverse recovery loss due to large di/dt. Basically, there is a tradeoff between faster switching transition and smaller reverse recovery loss. The technology, which has lowest Q_{rr}, theoretically provides the best reverse recovery loss under the same CtrlFET current slew rate.

In order to give good indication on trench MOSFET design for MHz frequency operating range, we obtain the $R_{DS(ON)} \times Q_G$ FOM. The simulation results show that this FOM still correlates well to the overall converter efficiency.

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