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Research Article

Development of Silicon Photonics Devices Using Microelectronic Tools for the Integration on Top of a CMOS Wafer

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Photonics on CMOS is the integration of microelectronics technology and optics components to enable either improved functionality of the electronic circuit or miniaturization of optical functions. The integration of a photonic layer on an electronic circuit has been studied with three routes. For combined fabrication at the front end level, several building blocks using a silicon on insulator rib technology have been developed: slightly etched rib waveguide with low (0.1 dB/cm) propagation loss, a high speed and high responsivity Ge integrated photodetector and a 10 GHz Si modulators. Next, a wafer bonding of silicon rib and stripe technologies was achieved above the metallization layers of a CMOS wafer. Last, direct fabrication of a photonic layer at the back-end level was achieved using low-temperature processes with amorphous silicon waveguide (loss 5 dB/cm), followed by the molecular bonding of InP dice and by the processing in microelectronics environment of InP μsources and detector.

1. INTRODUCTION

Silicon-based photonics has generated an increasing interest in the recent year, mainly for optical telecommunications or for optical interconnects in microelectronic circuits. The development of elementary components (I/O couplers, modulators, passive functions, and photodetectors) has achieved such a performance level that the integration challenge of silicon photonics with microelectronics has been discussed [1] in the literature and products have been announced in the near future [2]. The rationale of silicon photonics is the reduction of the cost of photonic systems through the integration of photonic components and an integrated circuit (IC) on a common chip, or in the longer term, the enhancement of IC performance with the introduction of optics inside a high-performance chip. To achieve such a high level of photonic function integration, the light has to be strongly confined in submicron waveguides with a medium ($\Delta n \sim 0.5$) to large ($\Delta n \sim 2$) refractive index contrast between the core and the cladding. Most of these studies have relied on the use of SOI substrates because they are accepted for CMOS technology. When one wants to integrate a CMOS circuit with some photonic functions in order to build a photonic integrated circuit on CMOS (PICMOS), the question of how to combine the photonic with the electronic parts is raised. The goal of this paper is to illustrate some routes and challenges of PICMOS in conjunction with presenting some technical achievements of our laboratories.

In the world of silicon photonics, different approaches of integration have been developed. The stand-alone one was pioneered by Bookham. It is comparable to silica on silicon technology, which today is in production whereby the silicon substrate acts only as a convenient and cheap substrate, but with the difference that the waveguiding layer is made on silicon. This technology, with waveguide dimensions typically in the μm range, is used by Kotura for their different products and also by INTEL for the demonstration of silicon building blocks. The rationale of highly integrated photonics

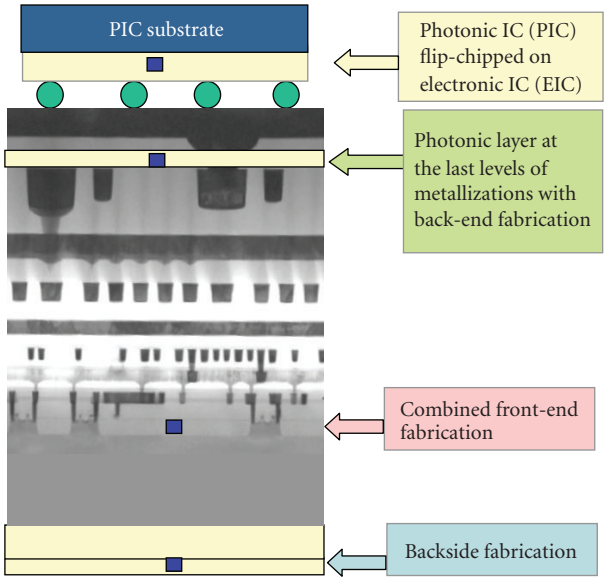


Figure 1: Integration routes.

is the reduction of the cost and the increase of performances by merging the photonics and the control electronics part. Different integration technology routes are presented in Figure 1. Each one has its own merit and will be discussed in the next sections. One can fabricate a photonic only integrated circuit (PIC) and connect the electronic and the photonic part either by state of the art flip-chip technique or by full wafer copper bonding which is in development. Fabrication of a photonic layer at the back side of the electric integrated circuit (EIC) can be envisaged and developed. However, connections through the substrate (100 to 200 μm thick typically) limits the frequency operation to MHz range. In this paper, deeper integration is considered with operation in the GHz domain with the EIC:

(i) a combined front-end fabrication: the photonic devices are at the transistor level which corresponds to the "full" integration;

(ii) the second route is often called 3D integration and relies on wafer bonding where a fully or partially processed photonic wafer is mounted on an almost finished CMOS wafer;

(iii) the third approach is to fabricate the optical layer with back-end technology at the metallization levels.

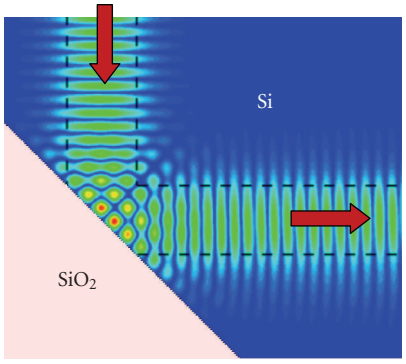
2. COMBINED FABRICATION

The integration of optical functions which are compatible with microelectronic process technologies presents new and interesting potentialities for integrated circuits. However, a monolithic integration of dissimilar functions still remains a difficult technological challenge. The company Luxtera chooses the combined front-end fabrication route for the production of 10 Gb/s transceiver. The chip is fabricated almost completely within a freescale 0.13 μm CMOS wafer fabrication and the electronic driver circuit are directly integrated aside the photonic circuits. With a combined integration scheme, the new components (waveguides and optoelectronic components) can be fabricated at the beginning of the IC process at the transistor level. Starting with the substrate, photonics components need a separation of larger than 1 μm between the waveguide core (thickness between 200 nm and 400 nm for a submicron waveguide) and the silicon substrate to avoid light leakage. On the contrary, CMOS technologies are based on either a bulk-type substrate or an SOI-type with thin buried oxide (BOX) and silicon layer (150 nm Si on 400 nm BOX decreasing to 60 nm Si on 150 nm BOX). As the thickness of the BOX is defined by the photonic parts, either a modified CMOS technology has to be developed using an SOI substrate with at least 1 μm thick BOX and a 200 nm thick silicon layers, localized thick BOX substrates under the photonic components can to be used. An analysis of the process steps for both technologies reveals that high temperatures ($\approx 1000^\circ$C) are necessary for the STI, implant activation as well as for the optimization of waveguide losses. Medium temperature ($\approx 700^\circ$C) steps are used for gate oxide, implant anneal, and for active photonic layers like SiGe/Si and Ge epitaxy, and lower temperature for metallizations on both. So mixing steps for the electronic and the photonic parts in order to avoid redundant steps is possible on an optical SOI substrate, leading to a photonic SOI technology (PSOI). For this goal, we developed a SOI technology with 1 μm BOX and 400 nm silicon thickness.

2.1. Passive circuitry

Passive optical circuits need low-loss optical structures to get enough optical power at each output to ensure light detection with an acceptable bit error rate. Strong light confinement is obtained either by partial etching of the silicon film leading to rib geometry or by full etching of the silicon film down to the buried oxide to get strip geometry. The highest compactness is achieved with single-mode strip waveguides which require a width smaller than 500 nm for height lower than 220 nm and allow very low crosstalk between waveguides distant from 1 μm. However, the main limitation is the difficulty to reduce propagation loss due to the side-wall roughness induced by the lithography and etching processes. Slightly etched submicron rib SOI waveguides are much less sensitive to scattering losses due to low interaction between optical mode and side-wall roughness [3]. Propagation losses as low as 0.1 dB/cm have been obtained using processes steps to reduce the roughness. These processes consist in a 10 nm thermal oxidation at 1100°C, followed by a desoxidation, and followed again by a second oxidation. Vacuum hydrogen annealing can also be used to reconstruct the silicon edges before thermal oxidation. The height and width of the rib waveguides were 380 nm and 1 μm, respectively, and the etching depth was 70 nm. However, with a constant thickness of 380 nm, different pairs of width and etching depth can lead to monomode operation.

Compact 90° turns using slightly etched SOI rib waveguides can be made by etching silicon down to the BOX to obtain a mirror facet at the angle between two perpendicular



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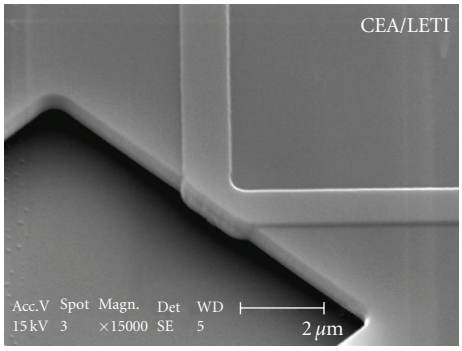
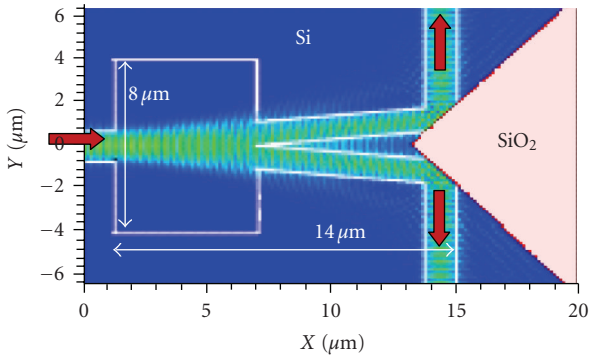


(b)

Figure 2: Etched mirror for 90° turn of rib waveguides: FDTD calculation of the field amplitude and scanning electron microscope (SEM) view after removal of the silicon oxide.



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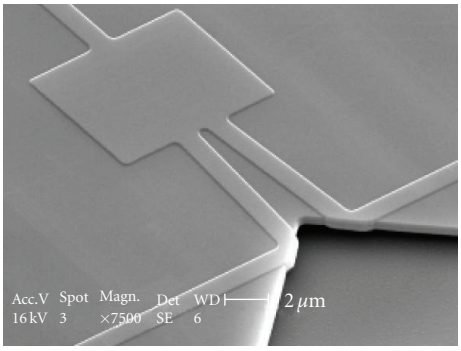

(b)

Figure 3: T-splitter for rib waveguides: 3D-FDTD calculation of the field amplitude and SEM view after removal of the silicon oxide.

waveguides (Figure 2). The theoretical loss determined from three dimensional finite difference time domain (3D-FDTD) numerical calculations is 0.1 dB, and the measured value is under 0.5 dB. The main issue to overcome for lowering this loss relies on the ability to etch anisotropically and without roughness the 380 nm down to the box. Low loss and compact T-splitters can be made by collecting the light in two waveguides after it has diffracted in a wider slab region (Figure 3). It occupies an area of 8 μm per 16 μm and is much more compact than a rib MMI splitter (118 × 13 μm). 3D-FDTD simulations give excess losses lower than 0.2 dB at 1.31 μm for each branch, which is confirmed experimentally with a measured value of 0.5 dB. Furthermore, a broadband efficiency, ranging at least from 1.3 μm to 1.6 μm, is obtained as well as temperature independence.

Shallow single-mode SOI rib microwaveguides are a promising solution for photonic integrated circuits, especially if an optical distribution to a large number of outputs is required. Experimental demonstrations of a 1 to 16 optical distribution [4] and an optical division equivalent to optical distribution from one input to 1024 output points [5, 6] have been demonstrated.

The interface between nanophotonic devices and a single-mode fiber is a real challenge due to their optical mode mismatch. In order to inject light anywhere on an optical circuit and to test optically the wafer, we developed diffraction grating couplers using etched grooves of the same depth than the rib etching on the top of the silicon layer. The surface gratings have been fabricated (Figure 4) and characterized for the +1 diffraction order at an operating wavelength of 1.31 μm for the TE polarization. At the resonant angle, a coupling efficiency higher than 60% has been measured under the grating. The resonance angle and the wavelength tolerances have been evaluated to 3° and 20 nm, respectively. The grating coupler is followed by a taper, and about 80% (loss < 1 dB) of the input power at 1.31 μm is coupled into submicron rib waveguides [7]. By engineering further, the grating (silicon thickness, etching depth, etc.) insertion lower than 1 dB in the 1530–1560 nm wavelength range can be achieved.

2.2. Modulated source

With the combined fabrication route, integration of a light source is the weak point. Silicon sources have to be proven and get sufficient maturity. Integration of InP components before the metallization is not thermally compatible. So before any integration of the source, a continuous external light source can be coupled via an input-output coupler (surface grating or edge coupler) to the waveguide circuitry of the circuit. To make the silicon photonics worthwhile, the optical signal has to be encoded to ensure information

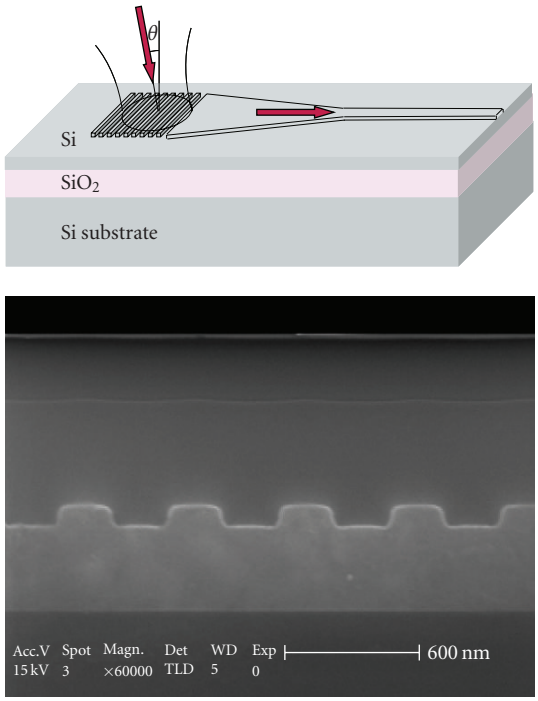

Figure 4: Scanning electron microscope view of a surface 1D grating.

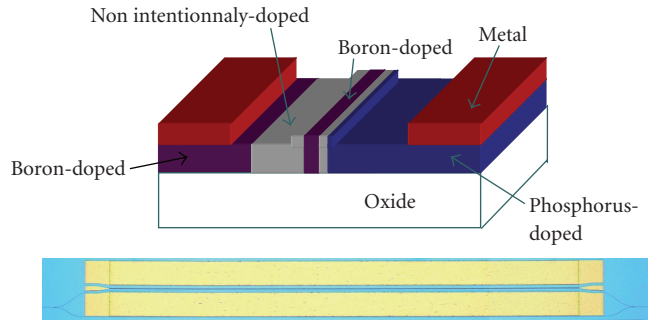

Figure 5: Cross section of the phase shifter structure integrated into a rib silicon-on-insulator waveguide and optical microscope view of the modulator.

transmission at frequencies larger than 10 GHz. Impressive progresses have been obtained in the recent years on several ways investigated for high-speed optical modulation in Si or Si-based devices: electro-optical effects in strained silicon [8] or SiGe superlattices [9], quantum confined Stark effect in silicon-germanium/germanium quantum wells [10, 11], Franz Keldysh effect in GeSi diode, [12], carrier concentration variations in silicon [13–18]. The mainly used possibility to make a high-speed optical modulator is to use index variations by free-carrier concentration variations. A lot of silicon-based optical modulators made for several years are based on free-carrier concentration variation using injection, accumulation, or depletion of carriers. Each structure is integrated in an SOI rib waveguide and the refractive index variation induces a phase shift of the guided wave. An interference device such as a Mach-Zehnder interferometer, Fabry-Perot microcavity, or microring resonator is used to convert the phase modulation into an intensity one. The best published results are summarized in Table 1.

For several years, vertical carrier depletion structures have been proposed by IEF [18, 19], using either SiGe/Si modulation doped quantum wells or all Si structures, placed in the intrinsic region of a PIN diode and integrated in an SOI rib microwaveguide. Holes introduced by thin highly-doped P+ layers in the Si barriers are confined in the intrinsic region of the pin diode at the equilibrium state. When a reverse bias is applied to the diode, the electrical field sweeps the carriers out of the active region due to band bending. Hole concentration variations are responsible for refractive index variations. The intrinsic response time allows operation at frequencies higher than 10 GHz. The performance of the modulators is also dependant on the access resistance, in series with the reverse-bias pin diode capacitor. The challenge is to get low optical losses and low RC constants in Mach-Zendher or Fabry-Perot interferometer configurations. The variation of the effective index due to carrier depletion has been measured at few$\cdot 10^{-4}$ at 1.55 μm for a 0 V to 6 V reverse voltage bias variation. After optimization of such structure, the obtained factor of merit ($L_\pi \cdot V_\pi$) is lower than 1.3. This vertical approach of depletion modulator was followed recently by Liu et al. [16] and Gardes et al. [17] and the 40 Gb/s operation obtained proves the high frequency capacity of the depletion solution. However, the fabricated modulator of this kind requires numerous doped epitaxy and implantation steps and it would be a real challenge for a combined fabrication.

So in the aim of reducing the complexity of the fabrication, we proposed hereafter a structure based on a horizontal pin diode which has a simpler technological process without any epitaxial steps. The optical loss is reduced as the optical mode has a weak interaction with the P+ and N+ doped regions of the diode. A good overlap between the carrier density variation zone and the guided mode is obtained leading to high effective index change. In comparison with vertical diodes [15–18], the capacitance of the diode is reduced, that is favourable to high-speed operation and low electrical power dissipation.

A schematic view of the device cross-section is shown in Figure 5. The silicon rib waveguide width is 660 nm, the rib height is 400 nm, and the etching depth is 100 nm leading to a single mode propagation of the guided mode at 1.55 μm wavelength. A P+ doped layer (10^{18} cm^{-3}) is inserted in the intrinsic region of the pin diode which acts as a source of holes. The P and N doped regions of the pin diode have doping concentrations close to 10^{18} cm^{-3}. Metallic contacts are deposited on both sides of the waveguide, a few microns apart to reduce optical loss.

The silicon modulator is based on an asymmetric Mach-Zehnder interferometer (Figure 5). The phase shifter is inserted in both arms over a length of 4 mm, and electrodes are used to bias one arm. Waveguide splitters are star couplers with a reduced area ($10 \times 2\,\mu$m^2). To ensure high-frequency operation, RC time constants have to be

Table 1: State of the art of silicon-based optical modulators.

Modulator type	λ (μm)	$V_\pi L_\pi$ (V·cm)	Bandwidth or time constant	Extinction ratio (dB)	Insertion loss (dB)	Labs
Franz Keldysh effect in Ge diode	1.647	no		7.5	2.5	S. Jongthammanurak, Group IV photonics, ottawa (2006)
Quantum confined Stark effect (QCSE) in Ge/SiGe quantum wells	1.55 at 90°C	no		Absorption coefficient contrast >3		Kuo and al, IEEE JSTQE, 12 (6) p1503 (2006)
Carrier injection in lateral PIN diode	1.55		12.5 Gbit/s	>9		Q. Xu et al., Optics express, 15 (2) p 430 (2007)
MOS capacitance	1.55	7.7	1 GHz			A. Liu et al., nature 427, 615–618 (2004)
		3.3	10 Gbit/s	3.8	10	L. Liao et al., optics express 13, 3129–3135 (2005)
Carrier depletion (vertical PN diode)	1.55	4	30 GHz (40 Gbit/s)		7	Liu and al optics express, 15 (2) p660, (2007)
Carrier depletion (Doped modulation of vertical Si PIN diode)	1.31 1.55	3.1 (exp)	Time constant ~ 1ps (Theory)			D. Marris-Morini et al., optics express, 14 (22) 10838 (2006)
Carrier depletion (Doped modulation of all Si lateral PIN diode)	1.55	5	10 GHz		5	This work
Carrier depletion (Doped modulation of all Si lateral PN diode)	1.55	3	9 GHz	6	3	T. Pinguet Group IV photonics Tokyo 2007
Carrier depletion (four terminal p^+pnn^+ vertical device)	1.55	2.5 (theory) birefringence free	Time constant <7 ps (Theory)		2	F. Y. Gardes et al., optics express 13 (22), 8845–8854, (2005)

minimized. The capacitance of the device was evaluated using small-signal simulations. The diode capacitance per unit length varies from 2.3 to $1.8 \cdot 10^{-16}$ F/μm for reverse biases from 0 V to -10 V. To ensure operating frequency above 10 GHz, the serial resistance of the device should be lower than 70 Ω/mm. Doped regions and silicide are thus used to form ohmic contacts and to achieve such a low resistance. Coplanar waveguide electrodes are designed to obtain characteristic impedance around 50 ohms taking into account the capacitance of the pin diode.

The modulator was fabricated on an undoped 200 mm SOI substrate with a 1 μm thick buried oxide (BOX) layer, a 400 nm crystalline silicon film, and a 100 nm silica hard mask on top. A 100 nm-wide slit is etched in the hard mask using 193 nm deep-UV lithographic patterning and reactive ion plasma etching. Double ion implantation and annealing are then performed to obtain a thin slit doped layer on the whole thickness. Waveguides are patterned with DUV lithography and HBr etching. Implantation for N+ and P+ area are performed followed by another annealing. It is worth to note that these implantation steps could be common to the source and drain fabrication. Finally, Ti/TiN/AlCu/Ti/TiN metal stack was deposited onto the wafer and electrodes were patterned and etched down to the SiO_2 layer. The used processes are fully compatible with SOI CMOS technology and could be transferred in high-volume microelectronic manufacturing.

The experimental setup uses a tunable laser around 1550 nm. A linearly polarized light beam is coupled into the waveguide using a polarization-maintaining lensed-fiber. The output light is collected by an objective and focused on an IR detector. Electrical probes are used to bias the diode. Very low values of the reverse current ($-2\,\mu$A at -10 V) have been measured that ensures low electrical power dissipation in DC configurations. The insertion loss was measured at about 5 dB. DC extinction ratio is around 14 dB from 0 to -10 V. To evaluate the modulation phase efficiency, a figure of merit is usually defined as the product $V_\pi L_\pi$, where V_π and L_π are the applied voltage and the length required to obtain a π phase shift of the guided wave, respectively. The

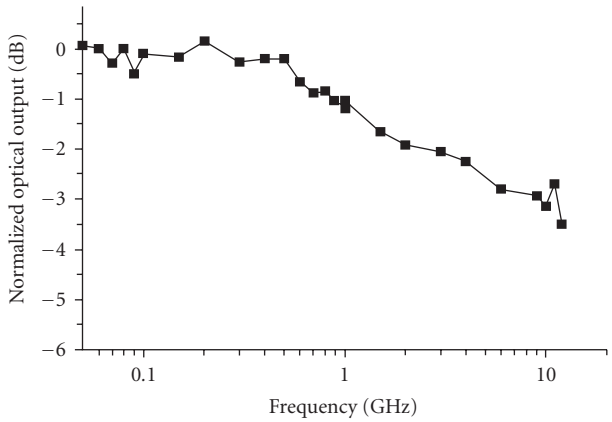

Figure 6: Normalized optical response of the Si modulator integrated in rib SOI waveguide with optical 3 dB-bandwidth of about 10 GHz.

obtained value $V_\pi L_\pi$ is equal to 5 V·cm. The normalized optical response of the modulator is reported in Figure 6 for a DC bias of −5 V. A 3 dB cutoff frequency of ∼10 GHz is measured on a Mach-Zehnder interferometer using 4 mm-long phase shifters.

Several ways improvement can be considered. Design optimizations of the RF travelling wave and optical waveguide are required to increase the modulation bandwidth to some tens of GHz. Progress in modulation efficiency are also possible: $V_\pi L_\pi$ product as low as 1 V·cm is theoretically predicted with the proposed structure, thanks to the good overlap between the optical mode and the doped region in the middle of the waveguide where carrier depletion occurs. The proposed structure has a large potential for the realization of high performances integrated high-speed modulators. Optical loss is reduced as the rib waveguide is not entirely doped, and the reduced-capacitance is favourable for high speed and low electrical power consumption. The fabrication can be combined with processing steps of CMOS transistors.

2.3. Germanium photodetectors

High-speed photodetector is one of the key building blocks and a large wavelength range of detection from 850 nm to telecom standards (1.55 μm) is necessary. These components have been available for several years from the III/V semiconductor technology on InP and GaAs wafers. Nevertheless, the integration of these devices on large wafers within the mainstream silicon technology requires hybrid integration approach [20, 21]. The used material requires high absorption for broadband telecommunication wavelengths. Within the group IV material, silicon is transparent at the telecommunication wavelengths ($\lambda > 1.2\,\mu$m) making it unsuitable for photodetection from 1.31 μm to 1.55 μm. While pure Germanium is a promising candidate as a broadband photodetector. Furthermore, germanium has a direct energy bandgap of 0.8 eV and is compatible with the CMOS technology.

Despite large lattice mismatch between Ge and Si, which is about 4.2%, previous works have shown that epitaxial growth of high-quality germanium layers on silicon can be achieved using reduced pressure chemical vapor deposition (RP-CVD) or ultrahigh-vacuum chemical vapor deposition (UHV-CVD). The germanium film was grown by RP-CVD on SOI substrates. After the growth of a thin buffer layer (50 nm) at low temperature (400°C), a Ge layer in the range of about 300 nm is typically grown at 700°C. The first layer enables to avoid three dimensional growths. After a thermal annealing at 750°C of the stack, the threading dislocations density is in the range of $5\cdot10^6/\text{cm}^2$. Spectroscopic ellipsometry measurements confirmed the absence of silicon diffusion as the thickness values of the various layers are close to the nominal ones.

The measured Ge layer absorption coefficients are close to 10 000 cm^{-1} and 5000 cm^{-1} at 1.31 μm and 1.55 μm, respectively. The strain-induced Ge bandgap narrowing allows detection to 1.6 μm with fairly large internal quantum efficiency. Hall measurements indicated that the layer was P-type, with a hole mobility close to $1300\,\text{V}\cdot\text{cm}^{-2}\cdot\text{s}^{-1}$ and a residual carrier density smaller than $10^{16}\,\text{cm}^{-3}$. Pump-probe experiments using a femtosecond laser have been carried out and have shown carrier lifetimes much higher than carrier collection times. Then the recombination rate of the photogenerated carriers is very low.

Much work has been focused on vertical illumination Ge photodetectors and impressive results with frequency up to 39 GHz have been obtained [22–24]. We focused mainly on integrated photodetectors coupled to a silicon rib waveguide. We investigated different technology schemes for the integration of Ge photodetectors with the silicon rib waveguides described in Section 2.1. The introduction of the germanium absorbing layer has been considered by a direct coupling of the light from the SOI waveguide into germanium. 3D FDTD simulation shows that in this case 95% of the light was absorbed in 4 μm length PD (Figure 7) leading to short photodetectors with possible reduced capacitance in the 10 fF range. However, this increased efficiency is balanced by the need of etching a recess in the 380 nm thick waveguide. For reliability of the process and due to the needed tolerance of the partial etching of silicon, the recess was etched with a SiO_2 mask to a safe 60 nm ± 10 nm thickness. Selective epitaxy was performed and filled the recess without any cavity between the output of the waveguide and the germanium layer. A SiO_2 cladding was deposited after germanium annealing before the fabrication of diodes (Figure 8). Three kinds of diodes have been studied: a metal-Schotkky-metal (MSM), a lateral PIN, and a vertical PIN.

The MSM structure needs an intrinsic Germanium and the formation of Schottky contacts on the Germanium surface. The surface contacts were dry etched in the SiO_2 before used in microelectronics. I–V curve for different designs showing the nonlinear behavior of Schottkky contacts were obtained. The electrode spacing is 1 μm. Figure 9 presents optical and electron scanning microscope views of the integrated photodetector. The measured dark current for such a photodetector is rather high, that is, 30 μA/μm at 6 V. That is

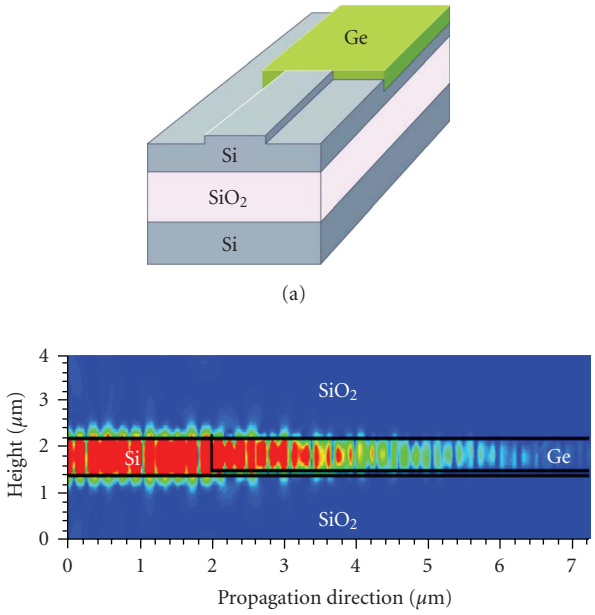

Figure 7: Ge photodetector integrated into a rib silicon-on-insulator waveguide and a 3D-FDTD calculation of the electric field profile amplitude in a longitudinal cross section of the photodetector.

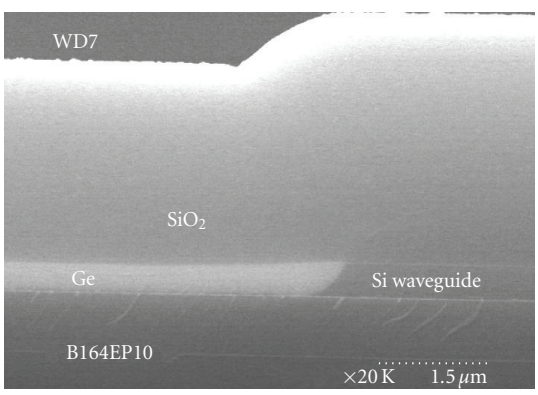

Figure 8: RP-CVD germanium epitaxy in a recess at the output of a silicon rib waveguide.

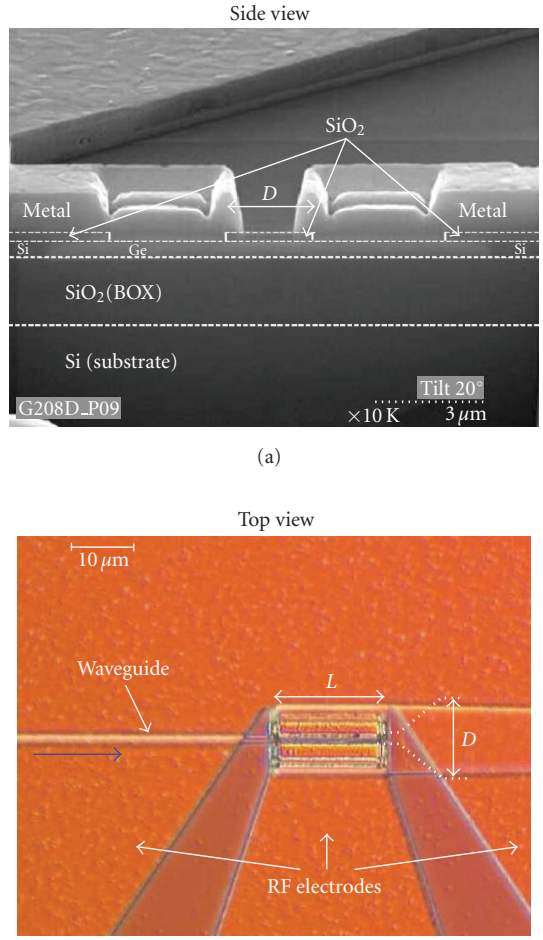

Figure 9: Optical microscope (Top view) and Scanning electron microscope (side view) images of the Ge on Si MSM photodetector integrated in slightly etched SOI rib waveguide.

mainly due to the Schottky barrier height, the dislocations in Ge layer and the metallic contacts. The responsivity of the 10 μm long integrated Ge on Si photodetector is as high as 1 A/W at 1.55 μm wavelength [25]. Bandwidth characterizations of MSM Ge on Si photodetectors have been carried out using two kinds of experimental setup at $\lambda = 1.55\,\mu$m: time response measurements and opto-RF measurements. The normalized responses at 6V bias obtained for both experiments at 1.55 μm, are reported in Figure 10. With opto-RF experiments, the -3 dB bandwidth is close to 25 GHz at 6 V bias. For time response experiments, the convolution between a Gaussian profile which characterizes the acquisition system response and a double exponential response give an intrinsic response time of the Ge on Si photodetector of about 19 picoseconds, which corresponds on a cutoff frequency of about 23.5 GHz at 6 V bias (Figure 10).

The fabrication of vertical PIN photodiode relies on selective epitaxy of in situ P doped layer, followed by intrinsic germanium and N doped layer. P doping with Boron during RP-CVD epitaxy was achieved with $1\cdot10^{19}$ at/cm^3. In situ, N doping epitaxy with a steep profile is a challenge as phosphorus is migrating easily. Deposition of N doped polysilicon on top of the intrinsic Ge is an alternative way. However, epitaxy with a high $1.5\cdot10^{19}$ at/cm^3 doping level, leading to 1.3 m$\Omega\cdot$cm resistivity, has been performed for upper contact of the photodetector. In order to contact the P layer at the bottom of the Ge layers, precise etching of Ge for bottom contacting is mandatory for submicron devices. With an AMAT centura machine using RIE etching with Cl2 gazes, a steep profile ($>80^\circ$) was achieved without any roughness. An SiO_2 cladding was then deposited and opened for contacting the P and N area. The Ti/TiN/AlCu metallization completed the formation of the pads (Figure 11). Depending

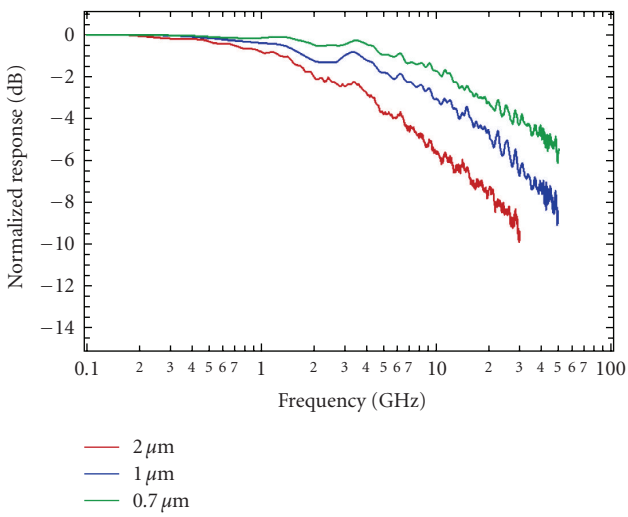

Figure 10: Normalized opto-RF responses at 6 V bias obtained for separation of 2 μm (red), 1 μm (blue), 0, 7 μm (green).

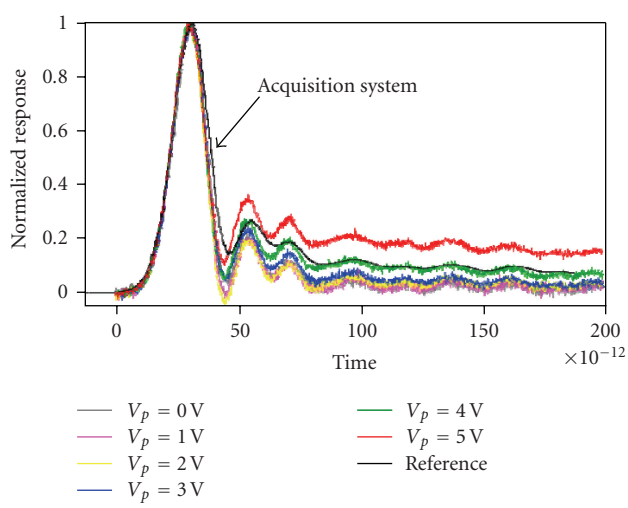

Figure 11: Femtosecond pulse response of an integrated vertical PIN.

of the length of the photodiodes, the dark current is in the nA range. The bandwith exceeded 35 GHz which was the limit of our test equipment (Figure 11).

2.4. Light generation

As efficient modulators can be performed, a CW light source is needed. Different options are followed: light is coming from an external InP laser connected with I/O couplers to the passive circuitry of the chip. This required efficient couplers and expensive packaging. In a second option [2], the laser source is flip-chipped and the emitted light is collected vertically via a surface grating coupler. Compared to the first option, the packaging is reduced and the integration is increased. The third option would be to process InP source after transistor fabrication, but it is rather difficult due to thermal budgets needed for the combined fabrication. The Graal option would be to process a silicon source. Despite the fact that SiO_x-Er layers are a good candidate for such silicon lasers, amplification and lasing have still to be demonstrated in an efficient way. So for a combined fabrication, light generation is really an issue with poor integration.

In conclusion, the results described here above show that a large variety of passive photonic devices except sources can be implemented on SOI substrate by means of CMOS technology. However, as the microelectronic process is very mature, the introduction of a new photonic part in a large CMOS foundry requires a lot of effort for changing the process. Low and medium scale IC foundries are more suitable to accept such modifications as they can differentiate their process and address new markets. However, this combined fabrication is fixed for one CMOS technology and not compatible with other CMOS technologies (SiGe, sSOI, GOI, etc.). As an example, a typical 130 nm CMOS technology ready for 10 G components may be not suitable for 40 G devices.

3. SOI PHOTONICS AND CMOS WAFER BONDING

Using the wafer bonding technique, one can introduce a photonic layer at some level in the processing steps of CMOS. Since the first metal layers are too densely packed and thin, introduction at the upper metal layers must be considered. For example, after the fabrication of metal 4 in advanced MOS process, the planarized surface has been coated with a deposited oxide. On another substrate, a photonic part is fabricated with silicon waveguides and electro-optical components. After cladding with oxide and planarisation of the optical wafer with CMP, perfect cleaning of both wafers facilitates their molecular bonding at room temperature. However, one of the flaws with this approach lies in the alignment between the electrical and the photonic parts which today can be as much as $\pm 2\,\mu$m. Therefore, the design rules for the subsequent metal layers have to take this alignment margin into account. After bonding, grinding and chemical etching of the backside of the Si optical wafer a flat surface of thermal oxide remains on the top of the PICMOS circuit. Some subsequent process steps are needed to electrically connect the electrical and photonic parts which involve etching through the top layer to contact the electrical circuit below. This technique is often called 3D heterogeneous integration because the CMOS part is separated from the photonic part without any silicon surface waste at the transistor level. With this approach, any microelectronics technologies can be used for the electrical parts and III–V components can be embedded in the photonic layer.

We have performed two demonstrations of this concept in collaboration with TRACIT Technology. On SOITEC optical SOI, we have processed a silicon rib network with cavities filled with Ge. After an SiO_2 cladding deposition, the optical wafer was carefully polished and bonded to a CMOS wafer before substrate removal (Figure 13). An SEM cross-cut observation revealed no interface between the two SiO_2

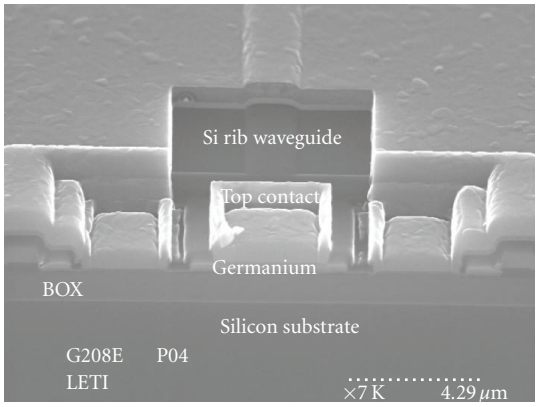

Figure 12: SEM view of a PIN vertical PD.

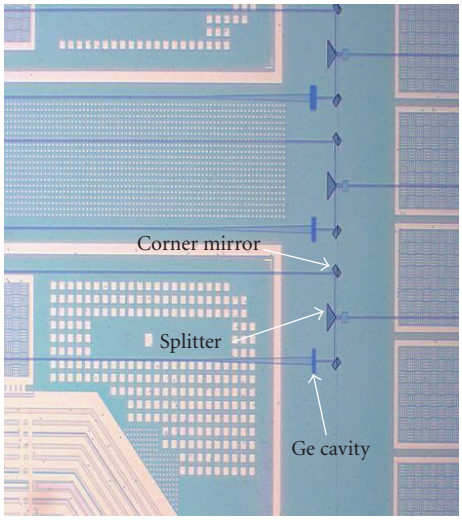

Figure 13: Rib waveguides with splitters, corner mirrors, rectangular cavities filled with germanium on a CMOS at level M4.

layers and no degradation of either the metal or the photonic layers (Figure 14).

This wafer bonding technique is a very promising way to integrate a photonic layer into a CMOS technology. The wafer bonding technique is mature and the intraconnections (3D techniques) are well addressed by the electronics community. The PIC can use all the components for the combined fabrication and integrate InP sources by die to wafer bonding. The EIC can use any new electronics technology and can be tested before the wafer bonding as well as the PIC. However, the main challenge that needs to be faced is the bonding cost issue compared to the combined fabrication.

4. HETEROGENEOUS INTEGRATION

As long as temperature is constrained so that it must not exceed 400°C, a photonic layer can be defined above the transistors and the dielectric/metallic levels. The obvious way to introduce such a photonic layer is to treat it as an

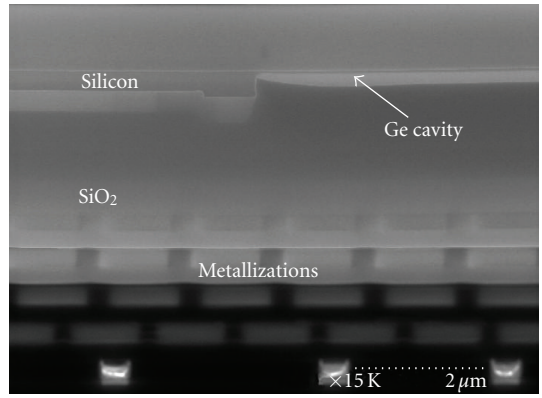

Figure 14: Cross-cut of a CMOS wafer with metal levels and a bonded photonic layer with rib waveguides and rectangular cavities filled with germanium.

additional metallic layer on top of most of the layers that have been used for the electrical interconnect. For the passive circuitry, we developed hydrogneited amorphous silicon layer which have a high contrast index. For the active parts, such as the introduction of copper for electrical interconnect, new materials like low temperature III–V compounds can be introduced on the wafers in a dedicated part of the CMOS clean room. After a CMP planarization and surface preparation, QD or MQW layers on top of an InP substrate are bonded on the wafers without precise alignment to fabricated aSi waveguides. The InP substrate of these die is then removed by chemical etching and further processing steps are performed which lead to sources and detectors connected to the metallic interconnects of the integrated circuit.

4.1. Amorphous silicon waveguide fabrication

As the area of a CMOS circuit can range from 1 cm^2 to 2 cm^2, increasing the refractive index contrast between the cladding and the guiding medium leads to more compact devices. With silicon oxide and silicon films, this is achieved with a value of 2, however, the losses have to be minimized. As with monocrystalline silicon on SOI, the high index difference allows the simultaneous use of refractive compact components and photonic crystal components for wavelength functionality. Amorphous silicon films were deposited by a capacitively coupled plasma reactor, with an RF excitation frequency (13.56 MHz). The power can be tuned from 30 to 1200 W and the operating pressure can be varied from 0.2 mtorr to few torr. All films were deposited at temperatures lower than 400°C to avoid damage to the interconnect layers. TEOS was used as precursor for oxide deposition and silane/H_2 mixture for the amorphous silicon. Sheet optical guided losses at the full after level during process were measured using a prism coupling technique (METRICON 5010) at 1.3 μm and 1.55 μm. By optimizing the H_2/Silane ratio in the deposition chamber, silicon films with losses as low as 0.2 dB/cm at 1.55 μm after 350°C annealing were deposited on silicon wafers covered with

1 μm TEOS. DUV 193 nm or 248 nm lithography with or without hard mask and HBr silicon etching were used to define the waveguide and basic passive functions for optical links (Figure 15). A thick 1 μm SiO_2 TEOS oxide was deposited to provide an upper cladding. Measurements were performed at a spectral range between 1.25 to 1.65 μm. Results are compared to previous SOI waveguides data [26]. The propagation losses decrease when the width of the waveguide increases and for a guide of width 500 nm (limits to have a monomode waveguide), there is only a dip towards the wavelength of 1380 nm. The losses are comparable to that of an SOI waveguide. We can notice that for this a:Si waveguide, the losses are, respectively, equal to 5 and 4 dB/cm for the wavelengths of 1300 and 1550 nm. We can consider that these losses are essentially due to the diffraction phenomenon due to the side wall roughness of the waveguide. For the waveguide of 800 nm width, the losses become very weak, lower than one dB/cm for wavelengths close to 1300 nm, and tend toward the values of a planar waveguide for both types of waveguides (with or without thermal annealing of 350°C), this shows that the material has a good stability in time. Experimental results of the basic building blocks obtain on the amorphous silicon are in a good agreement with those of the SOI technology. The μbends of 2 μm radius exhibited only negligible losses (0.04 dB/μbend) for all the spectral range. Measurements on a very compact size of $2 \times 4.2\,\mu m^2$ MMI devices give an extra losses of 1 dB at $\lambda = 1.3\,\mu$m (the design wavelength), a spectral range at 1 dB of 500 nm and the imbalance

between the two output is lower than 0.5 dB for all the spectral range. The most important features for amorphous silicon circuitry is the easy possibility to pile up layers and, therefore, to open new designs concepts or to ease designs such as crossings or coupling. As an example, in Figure 16, a aSi surface gratings is formed on top a aSi/SiO_2 Bragg mirrors for an increase in the coupling efficiency with a fiber.

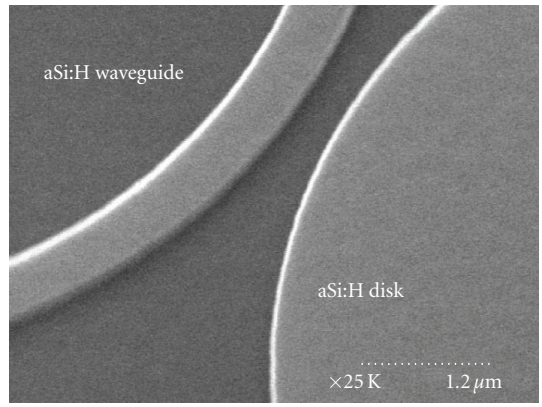

Figure 15: Amorphous Si waveguide with resonating disk.

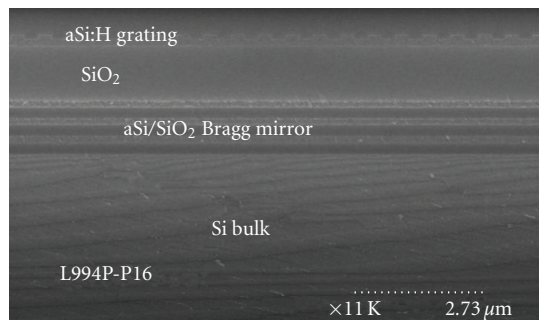

Figure 16: Cross-cut of an amorphous Si gratings on top of a Bragg mirror made of an:Si/SiO_2 alternate layers.

4.2. Die to wafer bonding of InP sources

Even with the latest development on active silicon photonics, III–V components remain more efficient for light-matter interaction. However, the cost of wafers and processing on small diameter wafers leads to rather expensive components. Integration of InP components coupled to passive optical functions on top of a CMOS requires a new approach which is different from the flip-chip solution. The first issue would be to enable integration of InP-based laser heterostructures on top of an IC. Another objective was to be able to process the InP-based components in the same way as the CMOS transistors in order to reduce the cost of the introduction of III–V components. As passive components can be efficiently developed with SiN or Si technology, only the active components require an InP technology. One should note that photonic sources or other active devices should exhibit low power consumption, and a small footprint, and should also operate at high speed. For all of these reasons, the needed devices should be as small and integrated as possible. This means that the InP-based components occupy a very small surface on a large CMOS circuit. Therefore, our approach consists of dicing an InP wafer with all the heteroepitaxial layers, bonding the die to the required places, removing the back of the InP die in order to only leave the active thin films attached to the CMOS wafer, thus enabling processing of InP components on a dedicated 200 or 300 mm fabrication line. To mount the die, molecular bonding was selected because good bonding quality can be achieved without any additional adhesive materials [22, 23]. In fact, the presence of the bonding material could inhibit efficient optical coupling. Furthermore, molecular bonding satisfies the requirements better in term of thermal conductivity and dissipation, transparency at the device working wavelengths and mechanical resistance.

Surface morphology and chemistry are critical to the bonding quality. Prior to bonding the die, the surfaces must be flat and uniform. The required flatness and uniformity can be obtained by use of CMP. The additional role of CMP polishing is to adjust the thickness of the silicon dioxide cladding layer in order to satisfy the optical coupling conditions. The surfaces were carefully cleaned and hydrated in the chemical solution and bonding can occur spontaneously when the prepared wafers are made of silicon. A complete physical model of such a molecular bonding was proposed and presented by Stengl et al. [27] and Gősele et al. [28]. As these materials are of dissimilar nature, one possible way

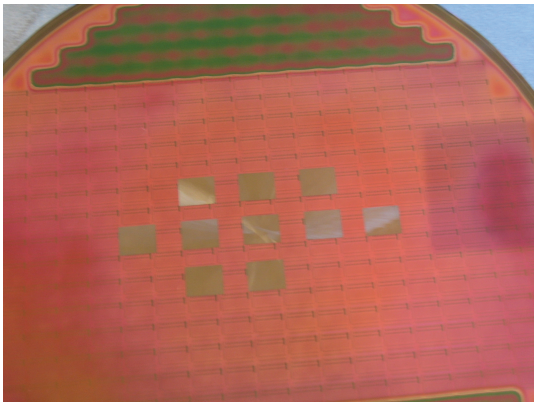

Figure 17: Silicon wafer with InP-bonded dice after InP substrate removal.

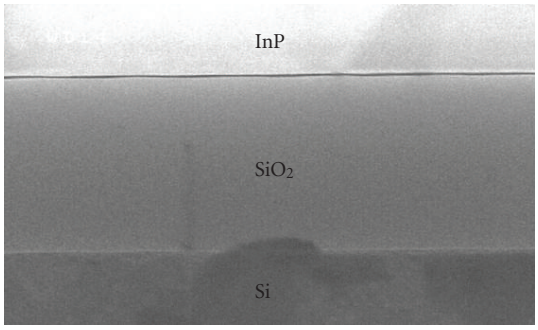

Figure 18: SEM cross-cut at the bonding level.

to achieve their assembly is to deposit a silicon dioxide or a silicon nitride layer on each surface.

Using this molecular bonding approach, we have successfully performed the heterogeneous integration of 50 mm InP wafers on silicon and also InP die containing an epitaxial layer stack with multiple quantum wells (MQWs). The CMOS wafer with SiO_2 top cladding was polished to reach a low roughness, cleaned in deionized water, and then dried. A silicon dioxide layer is deposited and then processed on InP (100) epiready substrate using electron cyclotron resonance plasma. Thanks to this preparation, the bonding of the both InP/SiO_2 and CMOS/SiO_2 wafers is similar to that achieved for Si/SiO_2 on Si/SiO_2 bonding. Further details on InP-on-Silicon wafer bonding have been described elsewhere [26]. The dice were obtained by mechanical dicing of 360 μm thick InP substrate containing an epitaxial heterostructure and a thin silicon dioxide layer. The smallest die size we have bonded is $1 \times 1\,\text{mm}^2$. A pick and place apparatus can be used to mount the InP die onto the silicon substrate. The bonding itself occurs spontaneously at room temperature; however, an annealing at 200°C for several hours reinforces adhesion. Mechanically thinning the die down to 20 μm was performed after bonding without degrading the remaining bonded material quality. Next, the remaining InP substrate and the sacrificial InGaAs layer can be chemically and selectively backetched. We mounted the 360 μm thick InP dice including MQW on the optical

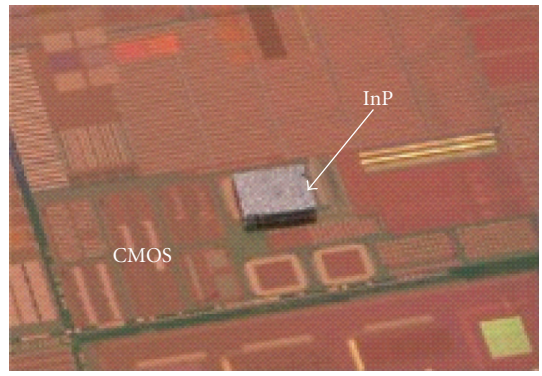

Figure 19: $1.2 \times 1.2\,\text{mm}^2$, 200 μm thick InP die-bonded on an optical layer on a CMOS substrate.

layer transferred onto a 200 mm diameter CMOS processed wafer [29] as shown in Figure 19. The InP dice were placed on specific locations where InP devices are needed. The additional postbonding technological steps such as polishing show that the assembled InP dice on the Si substrate can endure many kinds of mechanical maltreatment without debonding. The bond strength between the die and the substrate was measured using die shear testing equipment. The obtained shear strength is of 5 MPa ± 1.4 MPa for $1\,\text{mm}^2$, 360 μm thick InP dice. Using this approach in another experiment, $InAs_{0.65}P_{0.35}$ 6 nm thick single quantum well (SQW) confined between 120 nm thick InP barriers were deposited locally on the 200 mm wafer and this resulted as a localized epitaxy of II–V material.

4.3. Fabrication of InP microsources with microelectronics tools

The concept chosen was to define a cavity in the III–V material which is evanescently coupled to silicon waveguides located underneath. Whispering gallery modes (WGMs) of microdisks resonators are efficient solutions for low threshold microlaser fabrication. The concept chosen was to define a cavity in the III–V material which is evanescently coupled to underneath silicon waveguides. Whispering gallery modes (WGMs) of microdisks resonators are efficient solutions for photon confinement as they exhibit low mode volumes and high-quality factors. In a previous paper [30], the coupling of such μdisks to silicon waveguides has been described so we have only reported the main results here. The active heterostructure with MQW was designed to emit at 1.5 μm and was grown by molecular beam epitaxy (MBE) on a 2-inch InP wafer. After molecular bonding, 5 μm diameter microdisks were patterned with alignment accuracy better than ± 200 nm to the waveguides by reactive ion etching, using a CH_4:H_2 plasma. The quality of the final devices relies heavily on two main parameters: the ability to control the silica bonding thickness between the microdisk and the waveguide, and the ability to align properly the microdisk with the collecting waveguides. Figure 20 presents a top view of a final device. In the injection axis, the pumping light was generated by a pulsed 780 nm laser diode (duty-cycle of 10%

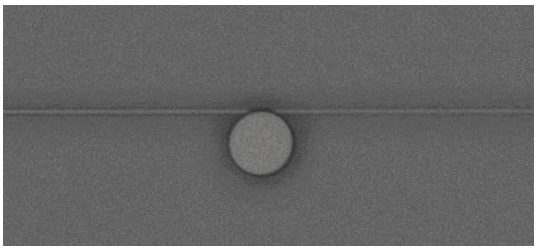

Figure 20: SEM top view of an InP μdisc perfectly aligned to a silicon waveguide.

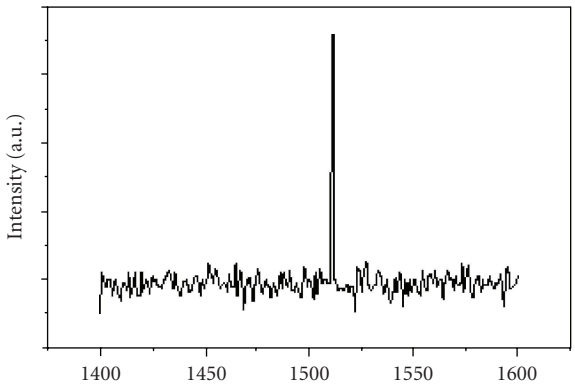

Figure 21: Spectrum of the guided light collected at the cleaved facet.

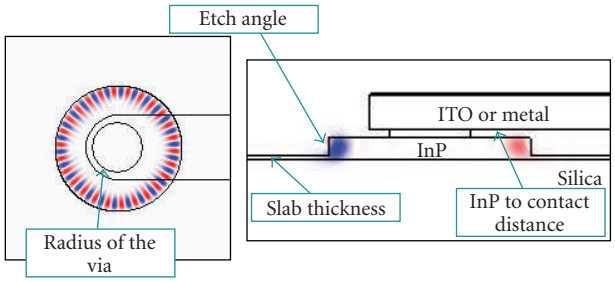

Figure 22: Main parameters for the design of the microlaser coupled to a silicon waveguide.

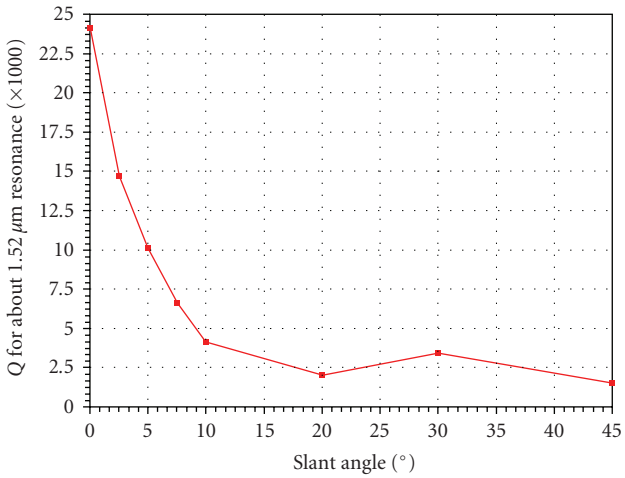

Figure 23: Evolution of Q for the 1.5 μm nearest mode for a 2.5 μm radius InP μdisk (0.545 μm thick) in silica with a 100 nm slab.

with a repetition rate of 200 nanoseconds), and focused onto the sample by using a ×10 IR microscope objective lens. The guided light was collected by a ×20 IR microscope objective lens, with the signal coming from a cleaved facet of the sample which was partially analyzed by the spectrometer, and partially used to display an IR image. Analysis of the radiated light from a coupled microdisk shows that laser emission is maintained although light coupling into a waveguide induces additional losses. The spectral analysis of the guided light (Figure 21) reveals the same spectral features as the radiated light in terms of wavelength and linewidth. With 300 nm separation of the μdisk to the silicon waveguide, the coupling efficiency is higher than 40%.

Fabrication of an electrically driven μlaser was then studied and consists in μdisks with a vertical P-I-N junction.

Two technologies were considered. The first one followed during the PICMOS project was to process samples with conventional InP technology after the ebeam lithography of the μdisk aligned to the silicon waveguide. This led to the first lasing device on silicon [31, 32], then to the first μlasing device coupled to a silicon waveguide [33], and finally to the demonstration of a full link in silicon [34, 35]. The second one developed in this paper concerns the fabrication of the μdisk using 200 mm microelectronics tools at CEA-LETI.

To process a vertical InP PIN diode (Figure 28) in the form of a μdisk connected at the bottom level and at the top level in the center, optimization of the main parameters design was necessary (Figure 22). The electromagnetic properties of a microdisk were first analytically calculated in an approximate 2D approach and afterwards precised with 3D FDTD. Figure 23 reported the sharp decrease of the quality factor with the increase of the slope edge for a disk with a slab. The mode is attracted in the slab region where it leaks. This gives a challenge for the etching of InP stack. We studied also the geometrical properties of the top contact, keeping in mind that high-quality factors must be achieved. Top contact that can be made of metal or ITO (Indium Tin Oxyde), has a major influence on the laser behavior: a too small contact results in inefficient electrical injection while a too large one strengthen optical losses due to metal or ITO absorption. The thickness of the InP-doped slab which is mandatory for defining the bottom contact is the result of a partial etch of the membrane constituting the microdisk. Too low, the contact is poor, but the quality factor is high. Too high, the contacts are good, but the quality factor decreases as the confinement is reduced. The process started by a contamination analysis of the 200 mm wafers after the bonding step and the InP substrate removal as it was not performed in the same clean room. Then a special decontamination of the rear face of the wafers was performed, in order to avoid any contamination of the chucks of the clean rooms equipment. An SiO_2 hard mask of 100 nm was deposited by PECVD. Microdisks were defined with 248 nm DUV lithography. A special attention has to be

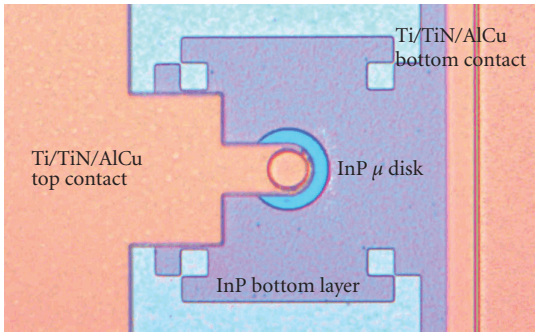

Figure 24: Optical top view of a micro disk.

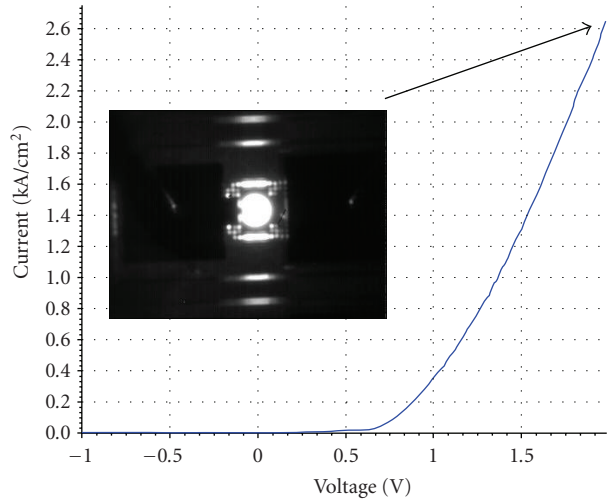

Figure 25: PIN characteristic for Ti/TiN/AlCu contacts.

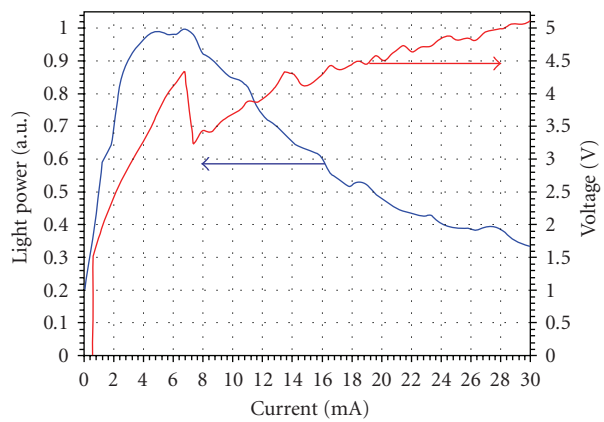

Figure 26: Light power emission at room temperature (in blue) and voltage (in red).

made on the focus, due to the presence of the dice on limited area of the wafer. The hard mask is then etched with InP as stopping layer. The partial etching was performed with ICP equipment using HBr reactive ion etching. A second lithography step followed by an InP etching defined the slab necessary for the bottom contact. Then 1.5 μm SiO_2 TEOS, that is, a low index and electrical isolating material, was deposited in place of the BCB used for planarization in the PICMOS demonstration. Chemical mechanical polishing (CMP) was then performed to get a planar surface with 400 nm separation with the upper surface of the InP disk. This distance between the membrane, where modes are propagating and the absorbing contacts were optimized for ITO contacts to get the highest Q. However, higher value could be useful with more absorbing material. As the P contact requires very high doping, which increases optical absorption, the studied structures use a tunnel junction to get two N contacts. Even if gold-based contacts have well known properties on InP, CMOS processes are not compatible with such a metal (except for back-end metallization) because of contamination risks. Ti/TiN/AlCu contacts were an alternative solution since we can get a low resistive contact. TLM measurements were performed on a trial InP wafer with a 500 nm thick $5 \cdot 10^{18}$ cm^{-3} N+Si doped layer and showed that the contacts were ohmic types. So top and bottom electrodes were formed by openings the SiO_2 to the bottom and upper InP N-doped surface and by patterning the electrodes after the Ti/TiN/AlCu deposition. Figure 24 shows the final device. Light emission in continuous wave (CW) electrical injection at room temperature was observed, but optical characterization proved that no structure was lasing, even in pulsed mode. The electrical threshold was determined to 0.7 V. Emitting light is possible under electric power as high as 150 mW, without reducing too much the light power. Maximum light emission is obtained at 30 mW. Lateral roughness and the etching slant are two critical parameters to get efficient resonators. Considering the real slab thickness that was 400 nm for a membrane of 1 μm, FDTD proved that these first samples with 45° slanted edges could not get higher quality factors than 500 what is too low to reach lasing mode.

Some devices with large area were tested as photodetectors (Figure 28), even their shapes did not match with a beam coming from a fiber vertically to the substrate. With the cross-cut of Figure 27, the TiAlCu were contacted with P and N-type layers, giving a PIN diode without the tunnel junction. The dark current at −1 V was quite low (1 nA) for a surface of 900 μm^2. This low value can be explained by passivation of the slanted edges with HBr etching. With a surface illumination at 1.55 μm, the sensitivity was measured in the range of 10 mA/W. This resulted from the very thin absorption layer. So by changing the active layers to more absorbing ones like InGasAs with a thickness up to 1 μm, the sensitivity can be largely improved to the A/W range, while keeping low dark current. So, arrays of III–V photodetectors can be processed on 200 mm wafers with microelectronics' tools.

Therefore, basic elementary building blocks for the demonstration of a laser source coupled to a silicon waveguide and photodetectors have been demonstrated and fabrication is possible on a 200 mm Si fabrication line. However, more studies such as optimization of the etching process, investigations of temperature dependency, power

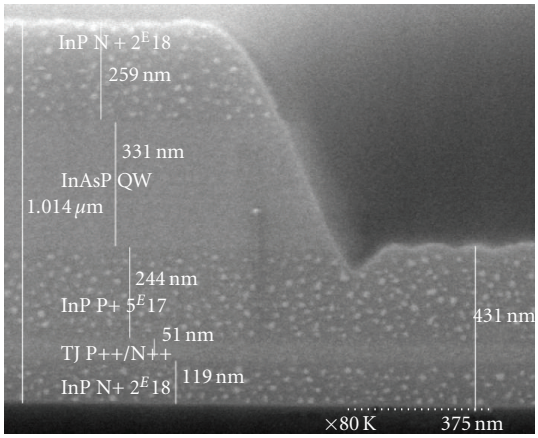

Figure 27: SEM slice view of a micro disk.

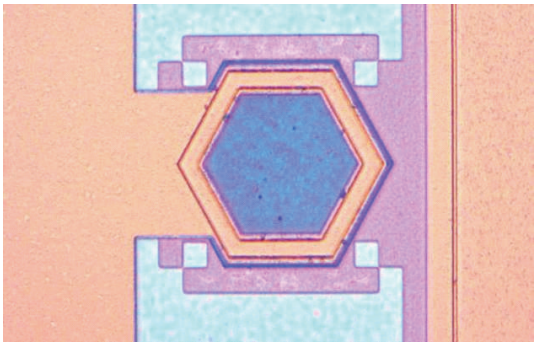

Figure 28: Hexagon used for photodetection.

range, and so on have to be performed before they can be used in applications.

5. CONCLUSION

Several different approaches for making the integration of a photonic layer on a CMOS circuit have been reported: the hybridization of photonics on top of a CMOS, a combined fabrication at the front end level, the wafer bonding of SOI photonic circuit at the back-end level, and an embedded photonic layer between metallization have all been performed and some results have been presented. These different approaches lead to different technologies with their own merits and drawbacks. Depending of the applications and the associated volumes of fabrication, the system designers would be able to choose the best way to make their desired system if the necessary building blocks were available. We have presented for each approach some technology routes to the achievement of these building blocks: for combined fabrication, a silicon rib technology was developed with low 0.1 dB/cm losses, 35 GHz Ge photodetectors, and 10 GHz Si modulators. A wafer bonding of an SOI wafer with silicon rib waveguide and cavities filled with Ge or with photonic crystals was achieved above metallization of a CMOS wafer. With the back-end level approach, direct fabrication of a photonic layer was achieved with low-temperature processes. Low-temperature waveguide technologies with amorphous silicon (loss 5 dB/cm) were developed. The molecular bonding of InP dice and the fabrication of InP microdisks using microelectronics tools base demonstrate that III–V μsources can be developed on silicon substrates. A 40% coupling was achieved to a stripe silicon waveguide, but only LED mode was demonstrated with electrical injection, due to poor InP etching. Clearly, the improvement and development of such photonics building blocks need to be carried on for the development of photonic integrated CMOS chip (PICMOS).

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