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Research Article

Choice of a High-Level Fault Model for the Optimization of Validation Test Set Reused for Manufacturing Test

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With the growing complexity of wireless systems on chip integrating hundreds-of-millions of transistors, electronic design methods need to be upgraded to reduce time-to-market. In this paper, the test benches defined for design validation or characterization of AMS & RF SoCs are optimized and reused for production testing. Although the original validation test set allows the verification of both design functionalities and performances, this test set is not well adapted to manufacturing test due to its high execution time and high test equipment costs requirement. The optimization of this validation test set is based on the evaluation of each test vector. This evaluation relies on high-level fault modeling and fault simulation. Hence, a fault model based on the variations of the parameters of high abstraction level descriptions and its related qualification metric are presented. The choice of functional or behavioral abstraction levels is discussed by comparing their impact on structural fault coverage. Experiments are performed on the receiver part of a WCDMA transceiver. Results show that for this SoC, using behavioral abstraction level is justified for the generation of manufacturing test benches.

1. INTRODUCTION

New efficient methods have emerged to design analog, mixed and RF (AMS & RF) or hybrid integrated circuits (ICs). Nowadays, the test of these ICs is becoming a crucial challenge for manufacturers. The trend toward miniaturization imposes to develop more and more integrated systems. Thus, electronic components are becoming systems-on-chip (SoCs) or systems-in-package (SiPs). This increasing complexity forces designers to define new design methodologies adapted to these complex systems with shorter time-to-market (TTM) and lower manufacturing cost constraints. However, the problem is not only to achieve short TTM but also to control the quality of final products. In fact, this growing complexity and the multiphysics systems integration increase the production testing difficulties and the test costs. In one hand, the SoC complexity involves low testability (i.e., low component parameters controllability and observability). In the other hand, new component natures (RF, mechanical,...) and their relative manufacturing processes involve fault modeling difficulties. Currently, the production test of AMS & RF SoCs is often performed by using a subset of the manually generated characterization test stimuli. Then, the evaluation of this subset is empirically made.

This paper relies on a method to evaluate and to generate a manufacturing test set from an initial characterization test set [1]. This method is performed on a Wireless SoC (WSOC) thanks to high-level fault injection and simulation techniques. The increasing SoCs complexity involves high transistor level simulation times for AMS & RF systems. In some cases, it is even impossible to simulate the whole system at the transistor level. This problem can be partially solved by describing the electrical system with higher description level (behavioral or functional level) rather than transistor level. So, when it becomes impossible to simulate faulty descriptions at low level, we propose to use functional or behavioral level descriptions. The aim of this paper is to define the most adapted abstraction level to measure the quality of a WSOC manufacturing test set. Obviously, there is a trade off between the qualification accuracy and the computation time.

In the first part, the fault injections and simulation techniques with functional, behavioral, and transistor description level are presented. The definitions of the faults models

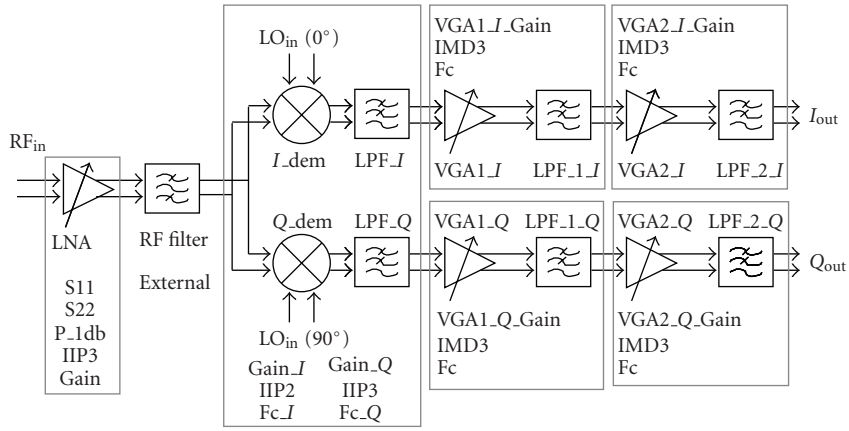

Figure 1: WCDMA receiver part (RX).

used to validate circuits at several abstraction levels are given. Then, the different descriptions of the WCDMA system applied to validate our method are presented. In the fourth section, our PLAtform for system qualification with mixed and analog signals (PLASMA) is detailed. Then, results provided by PLASMA for the receiver part of the WCDMA transceiver with functional and behavioral level are compared. Finally, the accuracy of functional and behavioral fault coverage is compared with structural fault coverage. This last step justifies the choice of behavioral level for the qualification of production testing.

2. HIGH-LEVEL FAULT MODELING AND FAULT INJECTION IN PLASMA

Faults injection and simulation techniques can be performed on models described at all abstraction levels. Obviously, the choice of the abstraction level is always a trade off between model accuracy and computation time. Modeling level used for the qualification of production test set must be close to physical level because manufacturing defaults are made of physical parameters modifications (oxide thickness, length, width, etc.). Thus, transistor fault modeling level, based on parameter variations of low-level components (inductor, capacitor, resistor, or transistor) is generally the most adapted for the test set generation applied on analog circuits. However, due to too high simulation times, this level is not adapted for the simulation of complex SoCs. So, we propose to use higher abstraction level descriptions to perform the manufacturing test generation. These high-level descriptions of the WSoC already exist because they have been developed and validated during the top-down design flow. The functional level is used for the development of the SoC architecture by converting system specifications into functional blocks. The behavioral level is used for the description of the system with more details than the previous level, in particular electrical effects (nonlinearity, coupling effects, impedances mismatching, etc.). The behavioral level allows fitting blocks interfaces by describing the system with more accuracy. This level has led to the standardization of behavioral languages like VHDL-AMS [2].

PLASMA interacts with the Mentor Graphics' ADvance MS RF VHDL-AMS simulator to perform the test set evaluation. So, PLASMA inherits all the characteristics of this simulator. It means that fault injection can be done

(i) on multilevel abstraction systems (i.e., transistor, behavioral, functional levels),

(ii) on multilanguage descriptions (Spice, VHDL-AMS, VHDL),

(iii) on multinature systems (analog, digital, RF, etc.).

In PLASMA, the fault model is made of only a single and small variation of one parameter in the original description. We call this faulty description a mutant. We assume that a huge modification of the description has little chance to appear during the design and the manufacturing processes. However, if this kind of fault appears, it should be easy to detect.

3. WCDMA SYSTEM

The studied system is the receiver part of a wideband code divided multiple access (WCDMA) transceiver. WCDMA is a technology used for third-generation cellular systems (3G). The frequency range down-link (bases station to user equipment) or receiver part is [2110–2170 MHz]. The modulation defined in the WCDMA standard is a classical IQ modulation based on two signals: I "in-phase" component of the waveform, and Q represents the "quadrature" component. WCDMA standard specifies several parameters: maximal and minimal output power, maximal power out of frequency band, adjacent channel leakage ratio (ACLR).

Figure 1 presents the architecture of the receiver part (Rx). It is a classical architecture made of low-noise amplifier (LNA), external surface acoustic wave (SAW) RF filter, mixers, base-band voltage gain amplifiers (VGA), and internal filters. Digital registers (not illustrated in Figure 1) control the LNA and VGA gains. These registers permit to control the receiver parameters; they can be used to control the system during validation [3].

Table 1: Limits of amplifier parameters.

Parameters	Typical value	Minimum	Maximum
Gain	13.85 dB	11.85 dB	15.85 dB
S11	−14.47 dB		−10.25 dB
S22	−6.1 dB		−1 dB
IIP3	−0.24 dBm	−5.03 dBm	
IIP1	−8.84 dBm	−18.4 dBm	

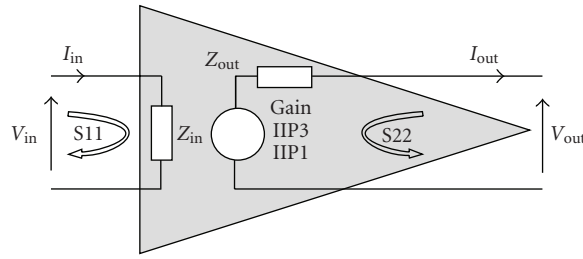

Figure 2: Behavioral model of LNA.

3.1. Functional model

In the top-down design flow, the architecture is first described at the functional level. The system functional specifications are budgeted into several functional blocks. Functional model does not implement electrical equations but only analytical relations between input and output (gain, transfer function, etc.). For example, functional description of LNA is only made of gain parameter; its specified values are presented in the first line of Table 1. The functional description of WCDMA receiver part is written with the VHDL-AMS language.

3.2. Behavioral model

In the following, the behavioral model of the LNA is presented in order to figure out this modeling level. In behavioral modeling, two classes of parameters, functional and electrical parameters, are defined. The choice of these parameters follows the verification plan [4]. The verification plan begins by identifying particular area of concern in the design. For example, if an area of concern is the loading of one block on another, the plan specifies that impedance matching must be modeled. In our case, the amplifier model is made of one functional parameter, the power gain (Gain), and several electrical parameters: input and output impedances (Z_{in}, Z_{out}), S parameters (S11, S22), compression point at 1 dB (IIP1), third-order intermodulation distortion (IIP3) (Figure 2). Table 1 specifies the limits of several parameters. Each parameter is defined by a typical value and with one or two worst-case values (minimum and/or maximum admitted values). For example, the gain is specified by two limits because both limits are significant; the other parameters have only one significant limit.

The other blocks of the system are also modeled following the verification plan with a few additional parameters: IIP2 (second-order intermodulation distortion), DC offset, and cut off frequency. Figure 1 gives a parameters list for each block. Finally, the receiver part is modeled by only 23 functional and electrical parameters (Figure 1). These parameters are the most significant parameters in the system design. Obviously, our qualification process could be also applied on a description involving additional parameters. The entire WCDMA transceiver is modeled with VHDL-AMS language.

3.3. Transistor-level model

In this study, the transistor-level description is considered to be the reference because it is close to the physical level. Then, we assume that this level allows us to evaluate the quality of our test set optimization. Only LNA has been described at the transistor level (Figure 3) because it would be too time-consuming to simulate the entire system at the transistor level. So, our evaluation is only realized on LNA functional, behavioral, and transistor-level parameters. LNA is particularly interesting because numerous behavioral parameters have been defined for this component. But, the transistor-level evaluation should also be realized for each block in the system. The simulation of the transistor-level LNA description embedded into the system is possible using the multiabstractions simulation technique. It means that simulations are realized using several abstraction levels for the different blocs in the systems: in this case, only the LNA is described at the transistor-level and the other blocs are described at the behavioral level. The simulations are realized with the Mentor Graphics' ADvance MS RF simulator. In addition, the Mentor Graphics behavioral VHDL-AMS library's CommLib RF [5] has been used.

The 2.1 GHz LNA circuit given in Figure 3 includes an amplification stage based on a cascode structure. The advantage of this architecture is to decrease noise and to improve linearity. Input and output matchers are added for the impedance matching.

4. PLASMA: PLATform FOR SYSTEM QUALIFICATION WITH MIXED AND ANALOG SIGNALS

PLASMA is an automatic test set qualification and generation platform which uses fault injection and simulation techniques. The fault simulation technique relies on the comparison of the simulation results of fault-free and faulty circuits (Figure 4). Faulty and fault-free descriptions are simulated with the same vectors. When the comparison of fault-free and faulty circuits simulation results involves a difference, the fault has been both activated and propagated toward one or more primary outputs; we say that the fault is detected. Although PLASMA contains an automatic stimuli generator, only test set qualification part and optimization will be discussed in this paper. The optimization involves the reduction of the initial test set by identifying and saving only the vectors which detect a fault.

4.1. Fault-free models definition

Fault-free descriptions are simulated with predefined input vectors. These descriptions provide simulation results which

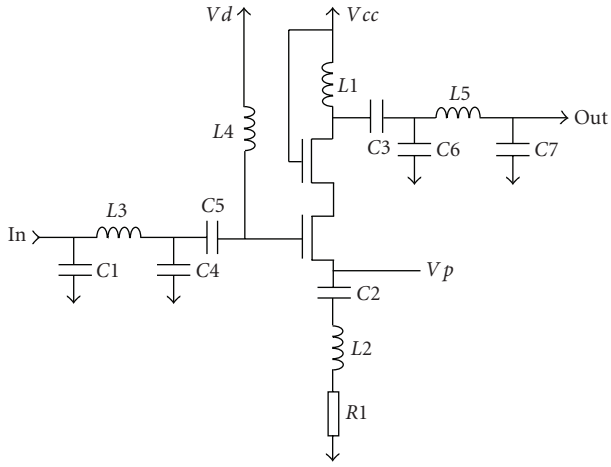

Figure 3: Structural model of LNA.

are "good" measurement values and which allow us to define fault-free measurement ranges. The comparisons with faulty circuits results are only possible thanks to these fault-free measurement ranges. Fault-free descriptions are defined as descriptions with parameters values within the specification ranges. Most popular methods to define a fault-free population sample are: Monte Carlo (MC) analysis and worst-cases combinations [6–8]. In our case, fault-free circuits simulations are performed using MC analysis and the statistical distributions of each behavioral parameter. For example, these distributions can be known by MC of transistor-level macrocomponents. We do not take into account correlations between two or more parameters. The number of fault-free simulations is decreased by drawing fault-free models with a predefined statistical distributions and by computing the statistical characteristics (i.e., the average μ and the standard deviation σ) of each result. The number of fault-free simulated models is increased as long as μ and σ variations are not negligible. Finally, the fault-free measurement ranges are defined in order not to reject fault-free circuits so the limits are computed at 6σ.

4.2. Faulty models definition

In part II, the fault model has been defined as a variation of one parameter. The original abstraction level for which PLASMA has been developed is the behavioral level. Obviously other abstraction levels can be managed by PLASMA. In the following, we will show that the best results are achieved with the behavioral level. Mutants are generated by translating one parameter of the original description to a value outside of its specifications, but the definition of this faulty value is difficult. When this value is too close to specifications limits, the fault is hardly detectable because circuit robustness and simulator accuracy mask it. When this value is too far from the fault-free detection limits, the fault is easily detected but it is also less realistic and it could be detected by most of stimuli.

The detection limit of the faulty value is fixed by simulating successive faulty values. The first value is defined far from the specification limits (but within minimal and maximal admitted faulty value limits defined bellow), then a dichotomy algorithm allows PLASMA to determine the faulty detection limit. During the detection limit computation, we define a faulty circuits range ("Faulty circuits" grey area Figure 5). This range is made of faulty circuits that have a probability to appear. Out of this range, the fault is very infrequent. The maximal and minimal admitted faulty parameter values $P_{\max\_\text{fault}}$ and $P_{\min\_\text{fault}}$ are computed with tolerance ranges (minimal and maximal specified values): $P_{\max\_\text{fault}} = P_{\max} + 5(P_{\max} - P_{\text{typ}})$. The fault detection limit is computed for every mutated parameter and every qualified vector. Relative parameter coverage (RPC_{Pi}) qualifies this detection limit for the Pi parameter; RPC is defined in

$$\text{RPC}_{\text{Pi}} = 1 - \frac{P_{\text{fault}_{\text{Pi}}} - P_{\max_{\text{Pi}}}}{P_{\max\_\text{fault}_{\text{Pi}}} - P_{\max_{\text{Pi}}}}, \quad (1)$$

where $P_{\text{fault}_{\text{Pi}}}$ is the detection limit P_{lim} for the Pi parameter represented in Figure 5, $P_{\max\,\text{Pi}}$ the maximum limit of Pi specification ranges, and $P_{\max\_\text{fault}\text{Pi}}$ the maximal faulty value possible for Pi.

When the detection limit equals to the specification limit, then the RPC is 100%. The closer this detection limit is from the specification limits, the higher is the RPC. The test set optimization is realized by saving for each Pi the vector that leads to the highest RPC.

5. TEST SET OPTIMIZATION FOR WCDMA RX PART BASED ON FAULT SIMULATION DESCRIBED AT HIGH ABSTRACTION LEVEL

5.1. Generation of the initial test set

During the design of complex electrical systems, a verification plan must be defined. This plan defines how to validate the design. This plan leads to the definition of test benches. These test benches are made of vectors which aim to validate system within all configurations (Gain, Offset) and with different input signals characteristics (frequency, power). For example, these vectors or stimuli verify the values of the programmable gains, the IIP3, the IIP2, and so forth. Generally, this manually generated test set is assumed to be adapted to the complete verification of the specifications. The aim of PLASMA is to evaluate and to optimize this test set.

The validation test set is made of stimuli with single tone signals applied on the RF_{in} input and the RX LO_{in} input (Figure 1). Signals are defined by frequency, power, and phase. The stimuli are also made of control parameters: gains configuration controlled by digital registered inputs. In the following experimental results, a test set made of 98 manually proposed single tone vectors is evaluated. These test benches have been optimized with PLASMA.

5.2. WCDMA functional and behavioral faulty descriptions

Faulty descriptions of WCDMA receiver are defined as presented in part II. The number of faulty descriptions is

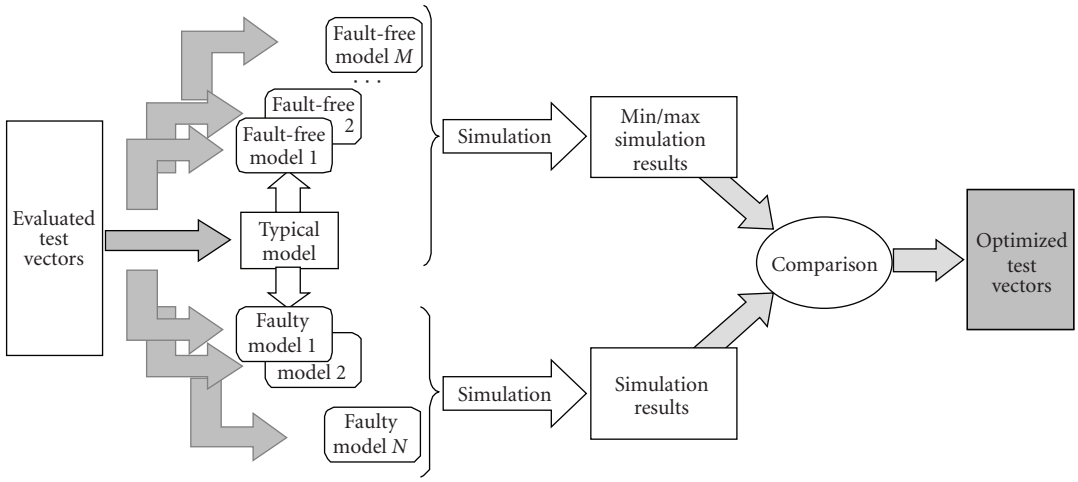

Figure 4: Test vector qualification & optimization.

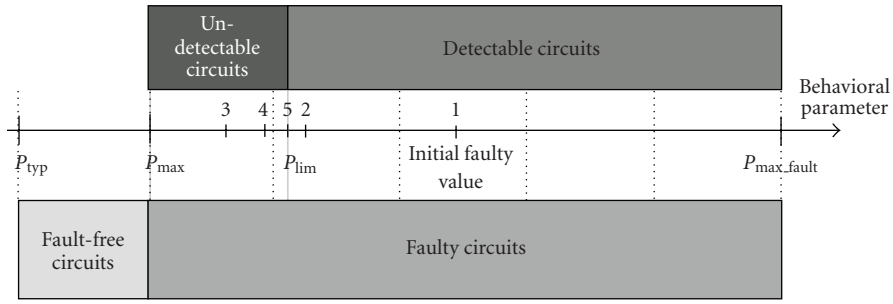

Figure 5: Definition of faulty value.

fixed by the number of parameters used in the original description. When one of these parameters is specified by two limits (e.g., the gain in Table 1), two mutants are generated on this parameter: a first one for the low limit and a second for the high limit; when it is specified by one limit (e.g.: IIP3), only one mutant is generated.

Due to this consideration, in a functional fault simulation approach, the receiver part of WCDMA SoC is modeled by 12 functional parameters (Gains and cutoff frequencies); it involves the generation of 24 faulty models. Behavioral description made of 23 behavioral parameters implies the generation of 36 behavioral faulty models because a few parameters are defined by only one limit.

5.3. Optimization results

The simulation has been realized with ADMS RF from Mentor Graphics on a 3 GHz Pentium-4, with 1 GB RAM, running a Linux operating system.

98 validation vectors have been optimized with our PLASMA tool. A first compaction is performed with the functional description and a second with the behavioral description (Table 2).

Over 24 functional mutated parameters, 18 have been detected by the 98 validation vectors during the entire dichotomy process. Then, the mutation score is 75% and the total computation time is about 11 hours 46 minutes. With the functional description, the average RPC computed with all functional parameters equals 65.6%. Each vector of the 98 initial test vectors detects at least one functional faulty parameter but after compaction, only 2 vectors are kept to achieve the same RPC. Hence, the number of predefined stimuli can be divided by 49.

During the optimization with the behavioral description, 92 vectors (out of 98) are qualified as redundant vectors because they do not increase the final RPC value (87.8%). The simulation time needed to perform this optimization at the behavioral level is 17 hours 39 minutes. The behavioral faults which have not been detected concern the variations

Table 2: Compaction, MS, average RPC, and simulation time comparison.

	Functional fault model	Behavioral fault model
Compaction rate	2/98 ⇒ 49x	4/98 ⇒ 24.5x
Mutation score	18/24 = 0.75	32/36 = 0.89
Relative parametric coverage	65.6%	87.8%
Simulation time	11 h 46 min	17 h 39 min

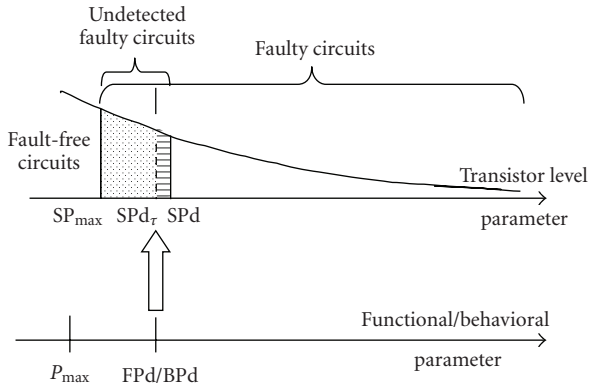

Figure 6: Detection limit of structural parameter.

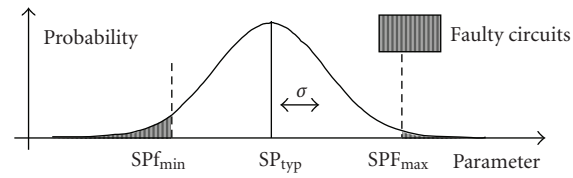

Figure 7: Capability process definition.

of S22, or IIP3 parameters. S22 variation is not detected due to the system robustness which masks its impact. In addition, our test vectors which only consist of single tone signals are not relevant for the detection of the IIP3 mutation. IIP3 mutants could be detected by a test set adapted to their activation and propagation in the system.

We observe that the simulation of our predefined test set at the behavioral abstraction level involves a high value of the average RPC. In addition, the comparison between functional and behavioral simulations shows that at the behavioral level simulation time is increased by about 50%. Now, we want to qualify and to compare, at the transistor level, these two optimized sets of test vectors.

6. EVALUATION OF FUNCTIONAL AND BEHAVIORAL FAULT MODELING FOR MANUFACTURING TEST

6.1. Principle of fault modeling evaluation

In the previous part, the results of the validation test set optimization have been shown, the efficiency of this optimization for manufacturing test is evaluated in this part. The advantage of our optimization technique based on high-level faults injection is the time reduction to qualify system test vectors; but is this fault modeling efficient for manufacturing test? The evaluation will be provided by making a comparison with a fault model described at a lower abstraction level: the transistor fault model. In the next section, the first analyzed high abstraction level is the functional level and then the behavioral level is analyzed.

The first stage of this evaluation is the computation of the *structural faulty parameter detection limit* (SPd) (Figure 6). This value is the limit that would be obtained if a transistor faulty description was used; we assume that it is the reference. SPd is computed with our PLASMA tool using a transistor-level description of the LNA only. In fact, in order to decrease the simulation time, only LNA is described at this transistor level (the other blocs are described at the behavioral level). Moreover, we only simulate compacted test set determined in Section 5.2.

The second stage of the evaluation is the comparison between structural and high-level faulty parameter detection limits. This comparison is only possible if the two detection limits are given at the same abstraction level. Thus, the *functional faulty parameter detection limit* (*FPd*) and the *behavioral faulty parameter detection limit* (*BPd*) computed during the optimization (Section 5.2) must be translated to structural parameter detection limits (SPD$_T$) (Figure 6). The conversion is performed by simulating each macrocomponent at the transistor level. In our case, this evaluation is only performed on the LNA. Thus, several test benches are used to measure the LNA functional parameters (Gain) or behavioral parameters (S11, IP1, etc.). The detection limits of high-level parameters FPd and BPd are converted to structural level SPd$_T$ by determining the single parametric deviation that involves at least one high-level parameter going out of its detection limits. But the comparison between SPd and SPd$_T$ is not enough because the same error between two different parameters has not the same impact on the final test quality. Thus, instead of comparing SPd and SPd$_T$, our high-level testing approach will be evaluated by comparing the number of undetected faulty circuits estimated with our approach with the number of undetected faulty circuits induced with transistor-level fault model.

During the design of system, engineers can estimate the distribution of parameters values. The capability process (CPk) (2) is a statistical parameter that allows designers to qualify the robustness of the structural parameters according to both the process and the device specifications. Parameters are assumed to have a Gaussian distribution and the CPk is defined by

$$\mathrm{CPk} = \frac{\mathrm{Min}\left((\mathrm{SP_{typ}} - \mathrm{SPf_{min}}); (\mathrm{SPf_{max}} - \mathrm{SP_{typ}})\right)}{3\sigma}, \quad (2)$$

where SP$_{typ}$ is the typical value of a parameter defined in the specifications, SPf$_{max}$ and SPf$_{min}$ are specified limit values, σ is the standard deviation (Figure 7).

The probability to produce a faulty circuit (hatched area) can be computed with the CPk values. Some faulty circuits are not detected (the darkest area in Figure 5) by the test vectors. These undetected circuits are present due to the system robustness, the measuring device accuracy or due to stimuli not adapted to the detection. Obviously, we aim to decrease this undetected number by finding the most relevant stimuli. In our case, the SPd value for each transistor parameter involves mutants which are not detected with the optimized test set. The number of these mutants is represented by the union of dotted and hatched areas in Figure 6. The dotted area is the number of undetected mutants estimated with high abstraction level descriptions. The hatched area (between SPd and SPd$_T$) represents the

Table 3: Structural parameter detection limits (SPds) computed.

	Structural specifications				Evaluation at structural level		Evaluation at functional level			Evaluation at behavioral level		
	Structural parameter	Typical value	Limit value	Faulty circuits (PPM)	Detection limit of structural parameter SPd	Undetected faulty circuits with SPd (PPM)	Detection limit of translated functional parameter SPd_T	Undetected faulty circuits with SPd_T (PPM)	Error of undetected faulty circuits (%)	Detection limit of translated behavioral parameter SPd_T	Undetected faulty circuits with SPdt (PPM)	Error of undetected faulty circuits (%)
Resistance (Ω)	*R*1 Max	2,500*E*+00	3,250*E*+00	7,944*E*−01	3,254*E*+00	8,791*E*−02	X	7,944*E*−01	88,93	3,253*E*+00	7,111*E*−02	2,12
Capacitor (F)	*C*3 Max	1,000*E*−12	1,100*E*−12	7,944*E*−01	1,100*E*−12	8,785*E*−02	X	7,944*E*−01	88,94	1,100*E*−12	7,099*E*−02	2,12
	*C*6 Max	1,400*E*−12	1,540*E*−12	7,944*E*−01	1,541*E*−12	8,794*E*−02	1,543*E*−12	3,220*E*−01	29,46	1,541*E*−12	7,111*E*−02	2,12
	*C*7 Max	1,000*E*−11	1,100*E*−11	7,944*E*−01	1,100*E*−11	8,802*E*−02	1,106*E*−11	6,324*E*−01	68,53	1,100*E*−11	7,116*E*−02	2,12
Inductor (H)	*L*1 Min	1,000*E*−06	9,500*E*−07	7,944*E*−01	9,498*E*−07	8,788*E*−02	1,149*E*−07	7,944*E*−01	88,94	9,498*E*−07	7,113*E*−02	2,11
	*L*1 Max	1,000*E*−06	1,050*E*−06	7,944*E*−01	1,050*E*−06	8,819*E*−02	X	7,944*E*−01	88,90	1,050*E*−06	7,099*E*−02	2,16
Transistor	LM_X2 Min	2,400*E*−07	2,360*E*−07	7,944*E*−01	2,360*E*−07	8,819*E*−02	X	7,944*E*−01	88,90	2,360*E*−07	7,143*E*−02	2,11
	LM_X2 Max	2,400*E*−07	2,567*E*−07	7,944*E*−01	2,568*E*−07	8,790*E*−02	3,663*E*−07	7,944*E*−01	88,93	2,567*E*−07	7,119*E*−02	2,10
	WF_X2 Min	1,000*E*−05	9,900*E*−06	7,944*E*−01	9,900*E*−06	8,802*E*−02	X	7,944*E*−01	88,92	9,900*E*−06	7,116*E*−02	2,12
	WF_X2 Max	1,000*E*−05	1,200*E*−05	7,944*E*−01	1,201*E*−05	8,793*E*−02	1,660*E*−05	7,944*E*−01	88,93	1,201*E*−05	7,108*E*−02	2,12

number of faulty circuits that are assumed to be detected with high-level qualification but which are not detected.

In the case of Figure 6, the high-level evaluation is a little bit too optimistic because a few circuits defined with high-level description as "detected faulty circuits" are not really detected (as shown with transistor fault model). This mistake is due to the fact that, in the high-level descriptions, the effects of parameters correlated variations are not modeled. In fact, our fault model is based on a single functional or behavioral variation but a modification of one structural fault leads to the variations of several high-level parameters.

6.2. Simulation results

Simulation results are presented in Table 3. The four first columns "(Structural specifications)" detail the specifications of the LNA transistor-level description: typical values, limit values, and the probability of occurrence of faulty circuits (computed with CPk).

Columns entitled "Evaluation at structural level" present the SPd values and the probability of undetected faulty circuits obtained during the analysis of WCDMA RX part with the LNA described at the transistor level and the other blocks described at the behavioral level. For all parameters, this number is equal to 0.088 PPM. This value is always the same because the number of faulty circuits is fixed by designers at 0.79 PPM for each parameter and faulty parameters are always detected during the 10 dichotomy loops. This number will be different if we use more dichotomy steps. This iteration number has not been increased because it is already close to the specified limit value (0.5% of the specified limit).

The other columns show the detection limits computed with high-level simulations and translated to the structural level (SPd_T). They are first obtained with the simulations of functional descriptions and then with behavioral level description. The errors made on the estimation of undetected faulty circuits computed with high abstraction level are presented on the grey columns. These values qualify the accuracy of using high-level descriptions.

The behavioral analysis shows that the SPd_T limits are very close to the SPd reference limits (ex: $R1$:SPd $= 3.254\,\Omega$ and $\mathrm{SPd}_T = 3.253\,\Omega$). Hence, the error on the estimation of the undetected faulty circuits is only 2%. With functional descriptions, results are really bad. For example, a variation of the resistance $R1$ does not lead to the modification of LNA Gain ($\mathrm{SPd}_T = X$). Therefore, the error made on the undetected faulty circuits estimation is far from undetected faulty circuits computed with structural simulations (88%). For the inductance $L1$, the variation involves a variation of the LNA gain ($\mathrm{SPd}_T = 11{,}5\,\mathrm{nH}$) but the value is very far from specification limit value that leads a number of detected circuits close to 0. Thus, the error on undetected faulty circuits is important (88%). In the best case ($C6$ capacitor), the error on the estimation is 29% but this error is again too high.

The errors achieved by functional fault simulations are too important. On the contrary, in our case study, errors involved in by behavioral simulations are acceptable. Therefore, we can conclude that behavioral fault modeling can be adapted to the qualification and the optimization of manufacturing test set. However, the efficiency of the behavioral model is directly linked to the accuracy of the original behavioral description which can vary through the verification plan definition.

7. CONCLUSION

In this paper, a test generator (PLASMA) has been presented and evaluated. In the proposed strategy, the validation test benches developed by designers to verify subblocs parameter specifications are reused. We show that reusing these test benches for the production testing is relevant. Generally the number of validation test benches is huge, so we propose to optimize them thanks to a high-level fault injection method. The optimization has been applied with functional and behavioral fault models. We assume that the detection of high abstraction level faults allows the detection of numerous physical defects. This assumption is verified by comparing simulation results generated with the high-level fault models and the transistor fault model. The metric used to evaluate our high level fault model accuracy is the number of un-detected faulty circuits. This metric qualifies the efficiency of the test stimuli. Results show that the numbers of undetected mutants is almost the same with a behavioral or a structural fault model but is different when we use functional fault model. These results have been obtained for the faults detection of an LNA embedded in a complete WCDMA receiver. In our case, the functional description is not adapted to the qualification of production test set. On the contrary, behavioral level description is interesting because it decreases test set qualification time and involves a good test set optimization.

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