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Research Article

Developments in Gigascale Silicon Optical Modulators Using Free Carrier Dispersion Mechanisms

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This paper describes the recent advances made in silicon optical modulators employing the free carrier dispersion effect, specifically those governed by majority carrier dynamics. The design, fabrication, and measurements for two different devices are discussed in detail. We present an MOS capacitor-based modulator delivering 10 Gbps data with an extinction ratio of ~4 dB and a pn-diode-based device with high-speed transmission of 40 Gbps and bandwidth greater than 30 GHz. Device improvements for achieving higher extinction ratios, as required for certain applications, are also discussed. These devices are key components of integrated silicon photonic chips which could enable optical interconnects in future terascale processors.

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1. INTRODUCTION

Over the past few years, the demands for high-performance computers, ever increasing instructions per cycle and high-energy efficiency, have fuelled the rapid development of multicore and many core microprocessors. With the recent advent of quad-core processors into the market [1, 2], coupled with the laboratory demonstration of a teraflop processor containing 80 cores [3], the need for interconnects supporting gigascale and terascale I/O has become imperative. Although present implementations of chip to chip copper interconnects are being pushed to deliver gigascale bandwidths with the design of transceivers that use active or passive equalizers [4, 5], this is unlikely to be a frequency scalable option.

On a parallel front, optical technology has been successfully deployed in long-haul fiber communications for more than two decades now. Individual components targeted toward these applications have been developed to the extent of delivering bandwidths as large as 40 Gbps [6, 7]. Multiple channels of such high bandwidth transmitted together using wavelength division multiplexing (WDM) is capable of terascale data rates. It would therefore seem intuitive to extensively employ similar optical technology in short reach applications such as rack to rack and board to board communications. However, this approach has not gathered momentum and the primary reason has been the high costs of materials such as III-V semiconductors and lithium niobate, which are inherently suited for photonic applications. Thus, developing a cost-effective optical technology has become essential for its adoption in the computer industry.

Interest in silicon photonics has been spurred predominantly by the low cost of silicon. In addition, its high volume manufacturability and the potential of electronics and photonics integration in the all pervasive microelectronics applications have added a further boost to this field. Silicon photonics is now being enabled by the successful demonstration of the requisite building blocks on silicon such as fast silicon optical modulators [8–13], SiGe photodetectors [14–16], silicon Raman lasers [17, 18], silicon optical amplifiers [19–22], silicon wavelength converters [23–25], and hybrid silicon lasers [26]. A high speed silicon photonic transceiver circuit which monolithically integrates all of these functionalities would be the ultimate culmination point expected to provide a low-cost solution for future optical interconnects.

Silicon optical modulators are one of the key building blocks which have been extensively studied. High-speed data transmission at 10 Gb/s [9–11], 30 Gb/s [12], and 40 Gb/s [13] has been demonstrated using silicon modulators with

different device configurations. Combining these gigascale silicon modulators with recently developed hybrid silicon lasers [26] and using WDM, one could create a single chip that can transmit data at Tb/s data rate for future high performance computing applications and mega data centers.

Unlike today's commercially available optical modulators which use III-V semiconductors [27] or $LiNbO_3$ [28], achieving modulation in crystalline silicon is challenging due to the fact that it exhibits no linear electro-optic (Pockels) coefficient and has a very weak Franz-Keldysh effect [29, 30]. It has been very recently shown that strained silicon possesses the Pockels effect [31], but the measured electro-optic coefficient is relatively small (an order of magnitude smaller than that for $LiNbO_3$). It has also been shown that strained Ge/SiGe quantum well structures have relatively strong electro-optic absorption due to the quantum-confined Stark effect [32], making it possible for optical modulation. However, critical strain engineering is needed and high-speed optical modulator performance has yet to be demonstrated for the Ge quantum well system. Silicon also exhibits an appreciable thermo-optic efficient ($\sim 2 \times 10^{-4}$/K) [33]. However, the thermo-optic modulator is not suitable for high-speed applications because of its inherently slow response.

The most effective way of performing fast optical modulation in silicon is via the free carrier plasma dispersion effect. This effect relates the variation in the concentration of electrons (ΔN_e) and holes (ΔN_h) in a semiconductor to changes in the absorption coefficient ($\Delta\alpha$) and refractive index (Δn). This effect has been mathematically described by the Drude-Lorenz equations [33] and further refined experimentally to give the following empirical relation at the wavelength of 1.55 μm:

$$\Delta n = -(8.8 \times 10^{-22} \Delta N_e + 8.5 \times 10^{-18} \Delta N_h^{0.8}), \quad (1)$$

$$\Delta\alpha = 8.5 \times 10^{-18} \Delta N_e + 6 \times 10^{-18} \Delta N_h. \quad (2)$$

The performance of modulators using free carrier plasma dispersion is determined by the speed and efficiency of carrier density modulation in the region of the traveling optical mode. Various device configurations have so far been proposed to achieve carrier density modulation in silicon. The first and most extensively investigated device configuration is the forward biased p-i-n diode modulator [34]. In this device, the free carrier density change in silicon is achieved through current injection and is primarily governed by minority carrier dynamics. The forward biased p-i-n diode approach in a resonant ring structure implementation has been demonstrated to give high modulation efficiency and, in turn, compact device sizes of $\sim$12 μm [35]. However, modulation speed in these devices is usually limited by the slow carrier generation and/or recombination processes, unless the carrier lifetime can be significantly reduced [36]. It is to be noted that a reduction in the carrier lifetime also results in a reduction in current injection as well as phase modulation and these tradeoffs need to be considered based on specific applications.

Contrary to the forward biased diode, the MOS capacitor [8, 9] and reverse biased pn junction [10, 12, 13, 37] based modulators rely on electric field-induced majority carrier dynamics and do not suffer from inherent bandwidth limitations. However, the phase modulation in these devices is not as efficient due to smaller overlap between the charge modulation area and the optical mode. In addition, since these devices are limited by their resistance-capacitance (RC) time constants, reducing device parasitic effects is critical to exploit their high bandwidth characteristics.

This paper describes our efforts progressively toward developing a high-speed silicon optical modulator. We focus on the investigation of the phase modulator or phase shifter, as it is the key element of modulators that can be constructed based on various implementation configurations such as Mach-Zehnder interferometer (MZI) and microring resonators. Since the MZI modulator has a broad operation wavelength range and provides a good vehicle for the modulator characterization, we adopted the MZI configuration in all our approaches [33]. In addition, our devices were designed to operate in the push-pull configuration in order to achieve higher power efficiency. This paper is organized as follows. In Section 2, we present details of the MOS capacitor-based silicon modulator and demonstrate 10 Gbps operation with an extinction ratio of 4 dB. Section 3 describes further device development to achieve bandwidths greater than 10 Gbps and discusses the implementation of the silicon modulator based on a pn-diode. Here, we present experimental results of data transmission at 40 Gbps with a 3 dB bandwidth of >30 GHz. Section 4 concludes this paper.

2. MOS CAPACITOR-BASED SILICON MODULATOR

Carrier density modulation is obtained by driving an MOS capacitor into the accumulation mode of operation. A voltage applied across the capacitor can induce an accumulation of charges in the doped silicon near the center dielectric. This modifies the refractive index profile of silicon in the waveguide region and ultimately the optical phase of light passing through it, thus acting as a phase modulator. When placed in one or both arms of an MZI, this phase modulator(s) can change the relative phase difference between the light passing through the two paths. Interference of the outputs from the two arms causes the phase modulation to be converted into the desired optical intensity modulation.

2.1. Design and structure

Figure 1(a) shows the schematic of the cross-section of the designed silicon waveguide-based MOS capacitor phase shifter. It comprises of a 1.0 μm *n*-type-doped crystalline silicon layer (the epitaxial silicon layer of the SOI wafer) at the bottom and a 0.55 μm *p*-type-doped crystalline silicon on the top with a gate dielectric separating them. The 10.5 nm gate dielectric consists of a multilayer stack of silicon dioxide and nitride. A process called epitaxial lateral overgrowth (ELO) is used to grow the crystalline silicon on top of the gate dielectric [38]. This use of single crystalline silicon was a significant development toward reducing device transmission loss from its prototype version which had a polysilicon layer that gave much larger optical

loss due to defects in the material lattice [39]. The p-doping concentration in the ELO-silicon is $1 \times 10^{18}/\text{cm}^3$, while the n-dopant concentration in the SOI silicon is $2 \times 10^{17}/\text{cm}^3$. These doping concentrations were chosen to ensure high bandwidth performance but were not strictly optimized for minimum resistance.

To form the rib waveguide, the entire ELO-silicon, gate dielectric, and ~0.1 μm of the SOI silicon are etched. This results in a waveguide rib height of 0.65 μm and waveguide slab thickness of 0.9 μm. The rib width is 1.6 μm (measured at the middle of the rib height), and since the sidewalls of the waveguide rib are not entirely vertical, the gate dielectric width is 1.9 μm. This yields a 1.6 μm by 1.6 μm waveguide with single-mode operation. In order to minimize the metal contact loss, it is necessary to place the contacts outside of the optical mode. To meet this requirement, two ~3 μm wide polysilicon sections with high p-doping concentration and a 0.3 μm overlap with the top corners of the ELO-silicon rib (Figure 1(a)) are grown. Aluminum for contacting the p-region is subsequently placed on top of the polysilicon. This design ensures an Ohmic contact between the metal and the polysilicon as well as electrical connectivity between the polysilicon and the rib. The 1 μm wide oxide region between the two polysilicon regions shown in Figure 1(a) serves to isolate the contact metal from the rib as well as push the optical mode downwards, away from the lossy polysilicon. The aluminum contacts to the n-region are deposited on the slab, also far from the waveguide. The oxide regions underneath the polysilicon and on both sides of the rib ensure optical confinement and prevent optical field from penetrating into the contact areas. The scanning electron microscope (SEM) cross-sectional image of the fabricated device is shown in Figure 1(b).

The overall length of the MZI modulator is 15 mm, which includes the input and output waveguides, 3 dB directional coupler-based splitters, and two arms of straight waveguides of a nominally equal length of 13 mm. Each arm comprises of a 3.45 mm long high-doping, high-speed RF MOS capacitor phase shifter section, and two ~4.75 mm long lightly-doped, low-speed phase shifters that are driven with DC voltages to electrically bias the MZI at quadrature.

2.2. Optical performance

As mentioned earlier, the MOS capacitor device operates in accumulation mode, where the *n*-type silicon slab is grounded and a positive drive voltage, V_D, is applied to the *p*-type ELO-silicon causing a thin charge layer to accumulate on both sides of the gate dielectric. The resulting change in free carrier density causes a change in refractive index (n) of silicon in accordance with (1), which is manifested as a change in the effective refractive index of the optical mode (Δn_{eff}). The optical phase shift at the end of the capacitor depends on the magnitude of this voltage-induced Δn_{eff}, the device length L, and the optical wavelength λ and can be calculated as [33]

$$\Delta\phi = \frac{2\pi \Delta n_{\text{eff}} L}{\lambda}. \tag{3}$$

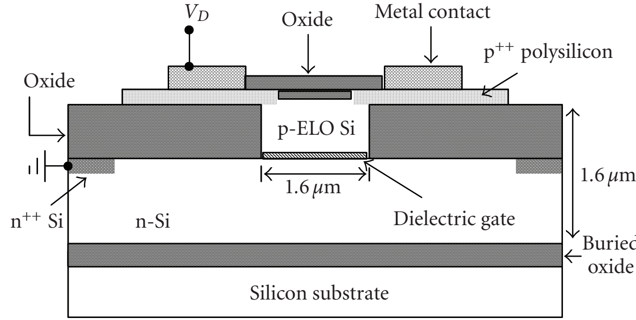
The Δn_{eff} is governed by device design parameters such as the waveguide dimensions and the position of the gate dielectric as they determine how effectively the accumulated charges overlap with the optical mode [8]. As a figure of merit for phase efficiency, the product $V_\pi L_\pi$ can be determined from the measured phase shift, where V_π and L_π are the voltage swing (beyond the flat-band voltage of 1.25 V) and device length required to achieve π radian phase shift. The goal is to minimize the $V_\pi L_\pi$ product to lower the required voltage drive and shorten the device length for a given phase shift. Smaller waveguide dimensions, though harder to fabricate, ensure stronger mode-charge interaction and hence higher phase efficiency. As an example, the phase shifter design of Figure 1 with waveguide dimensions of 1.6 μm × 1.6 μm gives $V_\pi L_\pi$ of 3.3 V-cm, which is 50% smaller than the prototype of this device which had waveguide dimensions of 2.5 μm × 2.3 μm and gave $V_\pi L_\pi$ of 7.8 V-cm.

The optical loss of the phase shifters is measured to be 10 dB/cm for the high-speed sections and 5.2 dB/cm for the low-speed sections. Optical measurements on the MZI modulator gives a total insertion loss of 19 dB comprising of 9 dB coupling loss and 10 dB on-chip loss, when the MZI is in the "on" state, which is defined here as the maximum optical output intensity of the MZI. Of the 10 dB on-chip loss, 3.5 dB is due to the high-speed (RF) sections, 2.5 dB due to the low-speed (bias) sections, and the remaining 4 dB is estimated to be due to a combination of voltage-induced free carrier absorption [40] and the unoptimized design of the splitters and bends. Optical coupling to the 1.6 μm × 1.6 μm waveguides is done using a lensed single-mode fiber with approximately 3.3 μm spot size. The total coupling loss of 9 dB can be significantly reduced using one of the known waveguide mode converter techniques [41–43]. Although mode converters were not implemented with the MOS capacitor-based devices, we have extensively studied their performance and have achieved coupling loss as low as ~1.5 dB/facet for similar waveguide thickness [44].

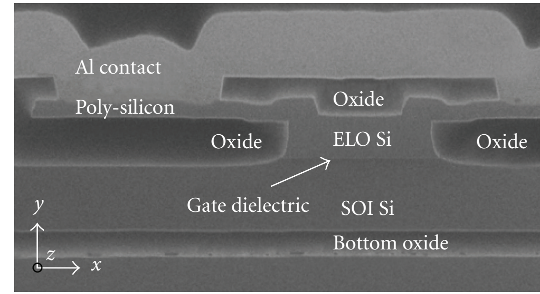
2.3. High-speed performance

The intrinsic bandwidth of the modulator was expected to be limited by the RC time constant. Since the capacitance of the device is proportional to its length, a shorter device would have a larger bandwidth. Therefore, in order to maintain the same phase shift as a 3.45 mm long RF phase shifter but simultaneously enhancing the bandwidth, the phase shifter is divided into eleven equal segments of 315 μm each and every segment driven by the same signal with a phase correlation determined by the group velocity of light. The impedance of these sections is measured as a function of frequency and is plotted in Figure 2. The reactance is modeled to be from a capacitance of 2.4 pF, while the resistance is measured as 6.5 Ω. The RC cutoff frequency, $(2\pi\text{RC})^{-1}$, can therefore be calculated to be 10.2 GHz.

High-speed operation of the modulator required the use of a low-impedance driver circuit. A custom IC was designed and manufactured using a 70 GHz-F_T SiGe HBT process, details of which can be found in [9]. It employs a



(a) Schematic of the device. The optical waveguide has dimensions of $1.6\,\mu$m × $1.6\,\mu$m. The highly doped (p++) polysilicon slabs are each $3\,\mu$m wide and with an overlap of $0.3\,\mu$m with the ELO silicon region. (The n-contacts are not shown here.)



(b) SEM of the device showing the optical waveguide, comprising of the *p*-type ELO-silicon and the *n*-type SOI silicon with the gate dielectric in the middle

Figure 1: Cross-section of the MOS capacitor-based silicon optical modulator.

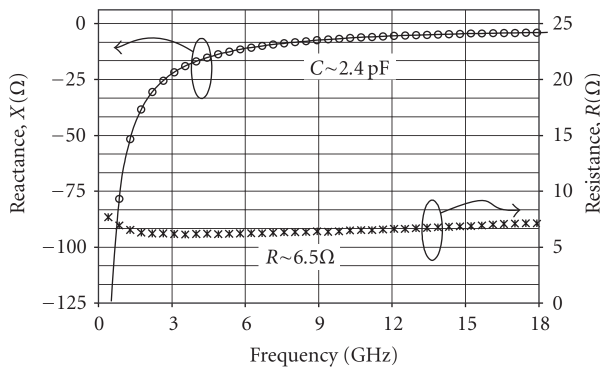


Figure 2: Impedance of a $315\,\mu$m long phase-shift segment on the MOS capacitor-based modulator. Resistance is measured as ∼6.5 Ω, while a modeled capacitance of ∼2.4 pF fits the measured reactance, giving an RC cutoff of 10.2 GHz.

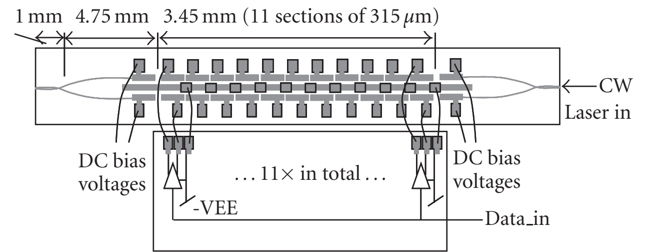


Figure 3: Schematic of the MZI-based modulator along with the driver inputs and wire-bonds.

push-pull emitter-coupled logic (ECL) output stage which is wire-bonded directly to each of the 11 segments of the RF phase-shifter on each arm and has been indicated schematically in Figure 3. The driver operates from a single-ended power supply in the range from 3.3 to 3.9 V and is targeted to deliver up to 1.6 V_{pp} (3.2 V_{pp} differential) to each phase-shifter when operating at 8 Gbps. The data pulses delivered to each of the segments are delayed using internal transmission lines to match the optical group velocity across the modulator. A number of control settings are available to trade performance for power dissipation (from 2.7 W to 3.9 W depending on supply voltage, output swing, bit rate, and edge rate). Of this power, approximately 10% is dissipated in the modulator. Improved driver design and improved phase-shifter efficiency will lead to reduced power dissipation.

To characterize data transmission performance, a DC voltage of −3.3 V is applied to the *n*-type silicon slab. A DC voltage applied to the ELO-silicon rib of the low-speed phase sections sets the MZI at quadrature bias. The DC bias is chosen such that the entire AC swing of 1.4 V_{pp} applied to the RF phase shifters is above the flat-band voltage [8]. This voltage swing, based on calculations for the device in Figure 3, should yield $0.15\,\pi$ radian phase shift in each MZI arm, enough to give a modulation extinction ratio (ER) of 4.2 dB. The modulator was tested at several data rates with a maximum at 10 Gbps. The resulting eye diagram for a 10 Gbps $[2^{32}-1]$ pseudorandom bit sequence (PRBS) input gives an ER of 3.8 dB and is shown in Figure 4. The 20–80% rise/fall time is measured to be ∼55 ps and is not found to vary too much from measurements at lower data rates such as at 6 Gbps. Combined with the fact that the inherent bandwidth of the modulator was earlier estimated to be ∼10 GHz from measurements of capacitance and resistance, it is evident that the inherent modulator bandwidth is not the limitation in these measurements. On the contrary, it is the ∼0.7 nH inductance of the wirebonds and the slower slew rate of the driver circuit, corresponding only to 8 Gbps, that limit the demonstrated device bandwidth.

This MOS capacitor-based modulator is the first silicon modulator to reach the 10 GHz bandwidth milestone. In addition, further improvements in phase efficiency, optical loss, as well as bandwidth are possible with optimization. Modeling and experimental studies show that reducing the waveguide dimensions and thinning down the gate dielectric could greatly improve the phase efficiency [45, 46]. A waveguide with dimensions of $1\,\mu$m × $1\,\mu$m and a gate dielectric of 6 nm is expected to give a $V_\pi L_\pi$ product as low as 0.68 V-cm. Such a device would facilitate the use of a CMOS-based driver with drive voltages <1 V_{pp} to obtain an ER as

high as 12 dB for a 0.25 cm long phase shifter length. By optimizing the doping profiles as well as the MZI splitter design, this small cross-section device can achieve 10 GHz modulation bandwidth with >12 dB ER and on-chip loss as little as 2 dB.

While the MOS capacitor-based modulator has the potential to realize several GHz of intrinsic bandwidth with reasonably low-optical loss, the device operation speed that can be experimentally demonstrated depends on the electrical drive design. As the capacitance of the MOS capacitor modulator is large (6–8 pF/mm), it requires very short device segments for high data rates if lumped drive is used. An alternative approach would be to use a traveling-wave electrode (transmission line) design. This approach not only addresses the RC speed limitation of lumped devices but also significantly reduces the frequency dependence of the power dissipation of the modulator. For the MOS capacitor-based modulator, however, its high capacitance makes matching the RF phase velocity and optical group velocity more challenging for high-speed operations. In addition, the RF loss of the transmission line would be large at high frequencies because of the large capacitance per unit length. Therefore, from the electrical drive circuitry point of view, it is critical to reduce device capacitance. With this in mind and with the aim of pushing up modulation speeds higher, we started exploring the pn-diode-based optical modulator design, which can potentially have a smaller capacitance. The following section describes the design and performance of the pn-diode-based modulator.

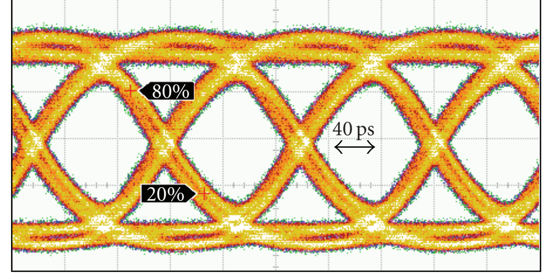
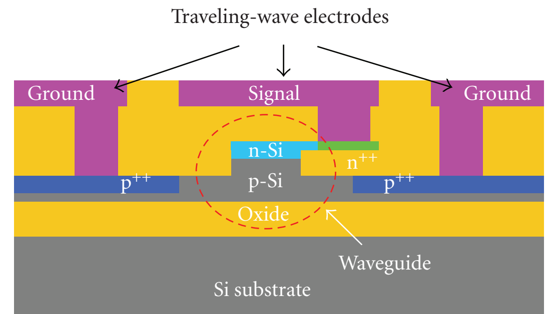
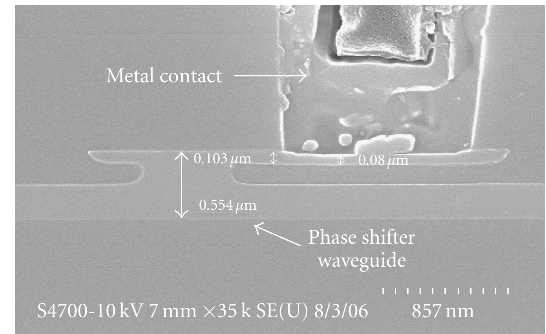


Figure 4: Optical eye diagram at 10 Gbps for the capacitor-based modulator copackaged with the custom designed driver. Measured ER = 3.8 dB.



(a) Schematic of the device. The optical waveguide has dimensions of 0.6 μm × 0.6 μm. The coplanar waveguide electrode has a signal metal width of 6 μm and signal-ground metal separation of 3 μm



(b) SEM of the rib area showing the metal contact on the n-type silicon cap

Figure 5: Cross-section of the PN-diode-based silicon optical modulator.

3. PN DIODE-BASED SILICON MODULATOR

This implementation of the modulator, also based on free carrier dispersion, produces a carrier modulation by operating a pn diode in reverse bias and hence in the carrier depletion mode. This modulator is also built in an MZI configuration but is an improvement over the MOS capacitor-based device in a couple of different ways. The dielectric layer between the two doped sections in the MOS capacitor is now replaced by the depletion width of the pn junction, and this leads to a reduction in the modulator capacitance and hence improved bandwidth. At the same time, the metal electrodes are now designed to operate as traveling wave electrodes and this eliminates the dependence of bandwidth on the RC time constant. Processing of this modulator also employs a simpler and more standard nonselective epitaxial silicon growth process instead of the ELO growth step required for the demonstrated version of the MOS capacitor-based device.

3.1. Design and structure

The phase shifter components of this silicon modulator are the reverse biased pn diodes embedded in the MZI arms. Figure 5(a) shows a schematic of the cross-sectional view of the phase shifter. It comprises of a p-type-doped crystalline silicon rib waveguide having a rib width of ~0.6 μm and a rib height of ~0.5 μm with an n-type-doped silicon cap layer. This thin cap layer which is 0.1 μm thick and ~1.8 μm wide is formed using a nonselective epitaxial silicon growth process and is used for pn junction formation and electrical contact. Both modeling and experiments confirm that the 0.6 μm by 0.6 μm waveguide can support only a single TE mode for wavelengths around 1.55 μm.

The p-doping concentration is ~1.5×10^{17} cm^{-3}, and the n-doping concentration varies from ~3×10^{18} cm^{-3} near the top of the cap layer to ~1.5×10^{17} cm^{-3} at the pn junction. To ensure good Ohmic contact between silicon and metal contacts, two slab regions ~1 μm away from both sides of the rib edge and part of the thin cap layer starting ~0.3 μm away

from the rib edge are heavily doped with a concentration of $\sim 1 \times 10^{20}\,\text{cm}^{-3}$ of p- and n-type dopants, respectively. The process parameters described above have been designed to target the pn junction at approximately $0.4\,\mu$m above the buried oxide to enable optimal mode overlap with the depletion region. As the n-doping concentration is much higher than the p-doping concentration, carrier depletion under reverse bias occurs mainly in the p-type-doped region. This leads to better phase modulation efficiency because the hole density change results in a larger refractive index change as compared to the electron density change as indicated by (1).

Modeling shows that the high-speed performance of a pn-diode modulator is limited by the pn junction capacitance, silicon resistances, and the metal contact parasitics, and not by the carrier dynamics. To minimize the RC limitation of the frequency response of the modulator [47, 48], we designed a traveling wave electrode based on a coplanar waveguide structure as shown in Figure 5(a). The "signal" metal layer is $\sim 6\,\mu$m wide and is connected to the heavily doped n-type silicon region through a $1\,\mu$m contact. The separation between the signal and ground metal layers is $\sim 3\,\mu$m and the metal thickness is $\sim 1.5\,\mu$m. The RF traveling wave coplanar waveguide and modulator optical waveguide are carefully designed so that both electrical and optical signals copropagate along the length of the phase shifter with similar speeds. In addition, it is necessary to keep the electrode capacitance small so that the RF loss of the electrodes is minimal. The single-sided asymmetric silicon cap layer design, also shown in Figure 5(a), is used to reduce the capacitance of the phase shifter. The transmission line loss, impedance, and phase velocity are calculated using a commercial software package HFSS, and details on this can be found in [49]. These parameters strongly depend on the metal trace dimensions as well as silicon doping concentration and profile. The cross-section SEM image of a fabricated pn diode phase shifter waveguide is shown in Figure 5(b).

3.2. Optical performance

As in the MOS capacitor-based modulator, the phase shift in the reverse biased pn junction is also given by (3). By changing the applied reverse bias voltage V across the diode, we can obtain a change in depletion width (W_D) according to the following equation [50]:

$$W_D = \left(\frac{2\varepsilon_0 \varepsilon_r (V_{\text{Bi}} + V)}{eN_A} \right)^{1/2}, \tag{4}$$

where the condition of an asymmetrically doped pn junction has been assumed with the n-doping concentration much higher than the p-doping concentration. Here, ε_r is the low-frequency relative permittivity of silicon, N_A is the acceptor concentration, and V_{Bi} is the built-in voltage. Changing the depletion width of a pn junction is equivalent to changing the free carrier density, and hence a change in the refractive index Δn_{eff}. Because the depletion width is usually smaller than the waveguide height, the phase modulation efficiency strongly depends on the pn junction location relative to the guided mode center.

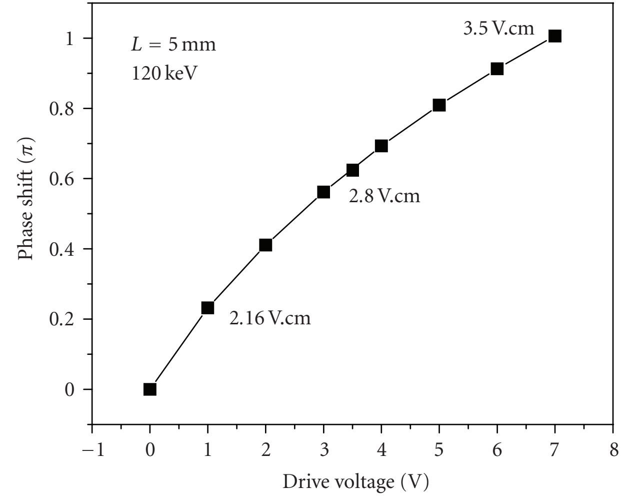


Figure 6: Nonlinear phase-shift versus drive voltage as modeled along with the phase efficiency values for the PN-diode-based modulator with a 5 mm long phase shifter at 1 V, 3.5 V, and 7 V.

Similar to the MOS capacitor-based modulator, we define the figure of merit for phase efficiency as the $V_\pi L_\pi$ product, where V_π and L_π are the reverse bias voltage and device length required for achieving π-radian phase shift, respectively. The $V_\pi L_\pi$ dependence on junction position location is modeled to show that at 3.5 V drive, junction depths of 0.1, 0.2, and $0.3\,\mu$m from the top of the waveguide rib yield $V_\pi L_\pi$ values of 5.2, 3.1, and 2.8 V-cm, respectively. This marked dependence proves the importance of optimizing the p- and n-doping profiles to get maximum overlap between the free carrier density change and the optical mode. Figure 6 also shows the modeled phase shift versus the reverse bias for the device with a junction depth of $0.3\,\mu$m and with a length of 5 mm. It is clear from Figure 6 that the phase efficiency is not linearly dependent upon the voltage, and this is in accordance with the nonlinear dependence of W_D on the bias, as indicated in (4). A better phase efficiency is obtained for a smaller drive voltage. For example, $V_\pi L_\pi = 2.16$ V-cm for 1 V drive, while it is 2.8 V-cm for 3.5 V drive and 3.5 V-cm for 7 V drive.

Figure 7 shows the measured phase shift of the pn junction phase shifter as a function of the drive voltage for different phase shifter lengths. As the data shows, $\pi/2$ phase shift is achieved at 4 V bias for a phase shifter length of 5 mm, and hence the measured $V_\pi L_\pi$ is ~ 4 V-cm. This measured phase efficiency is much smaller than the modeled results shown in Figure 6. We suspect this is mainly due to process variations in the pn junction location, causing it to be nonoptimal. We can also see that the measured phase shift is not linearly dependent on the drive voltage, which is qualitatively in agreement with our modeling. Figure 7 also shows the phase shift versus drive voltage for 1 mm and 3 mm phase shifters. As expected, they have the same phase efficiency of ~ 4 V-cm.

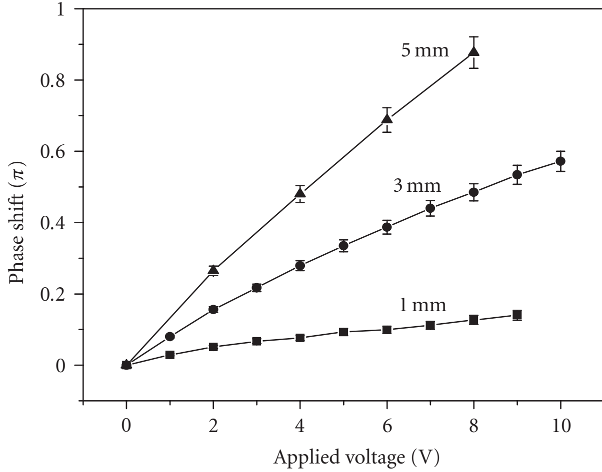


Figure 7: Measured phase shift versus applied voltage for MZIs with phase shifter lengths of 1 mm, 3 mm, and 5 mm. Phase efficiency for these devices is calculated as 4 V-cm.

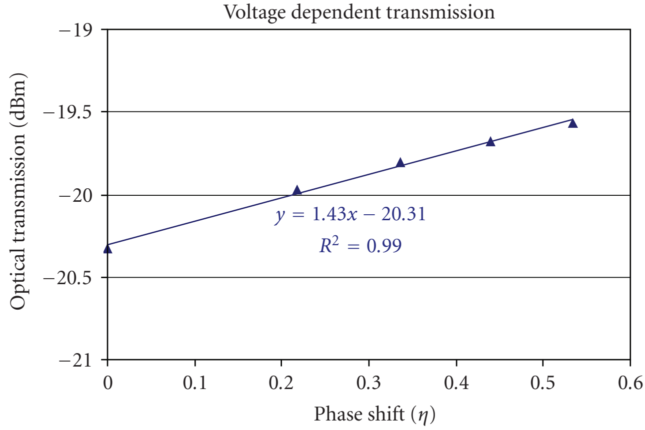


Figure 8: Measured change in optical transmission versus phase shift yields a voltage dependent gain of 1.43 dB/τ.

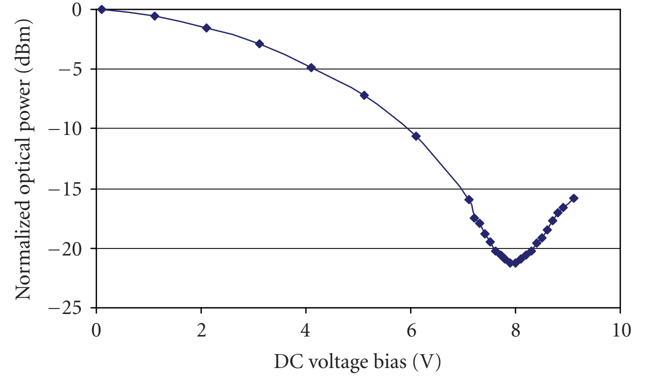


Figure 9: Transfer characteristics (optical power output versus bias voltage) for an MZI with phase shifter length of 5 mm. Measured DC extinction ratio >20 dB.

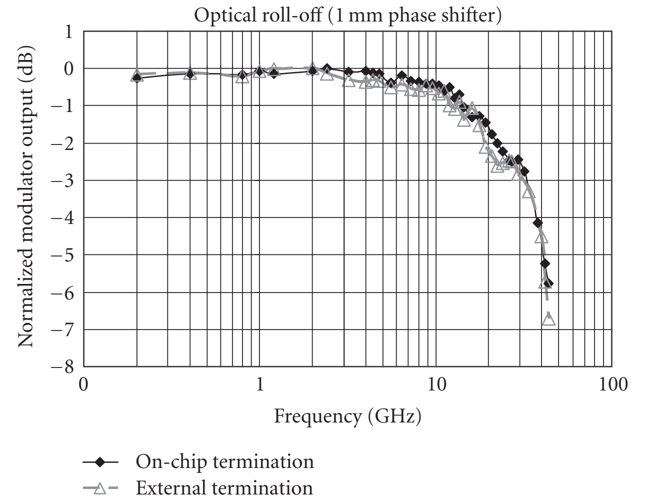


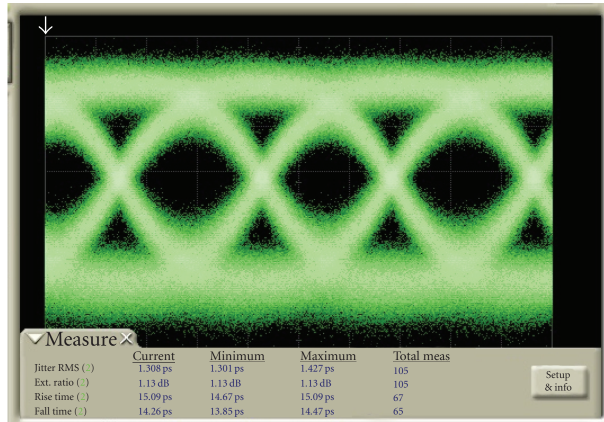
Figure 10: Frequency response measurements for an MZI with a 1 mm long phase shifter with on-chip and external termination, respectively, indicating a 3 dB roll-off at ~33 GHz.

The phase modulation is accompanied by optical absorption modulation, as can be seen in (2). Therefore, we expect a voltage induced gain in the phase shifter transmission which can introduce an optical field amplitude imbalance between the two arms of the MZI and potentially degrade the extinction ratio of the device. To quantify this effect, we measure the change in transmission for a straight phase shifter for different bias voltages and plot the optical transmission versus the phase shift. The results are given in Figure 8 which shows that the measured VDG is ~1.43 dB/π. This is in excellent agreement with our modeling. Inspite of the VDG-induced arm imbalance, the DC extinction ratio of the MZI is measured to be >20 dB, as can be seen in Figure 9.

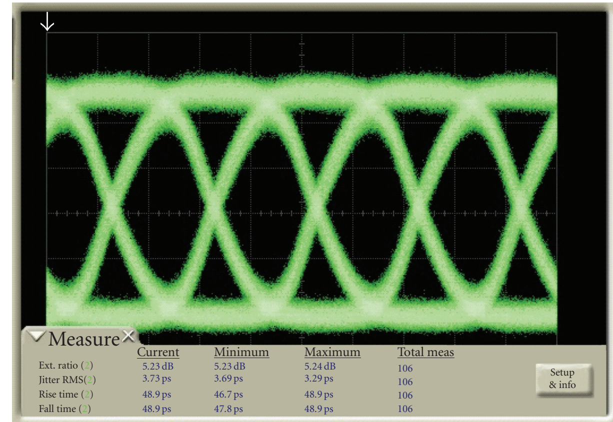
The total length of the MZI modulator is 8.25 mm. This includes the input and output waveguides, 2 MMI splitters, and the two straight arms of the MZI, each ~3 mm long, inclusive of a 1 mm long phase shifter. 1 × 2 multimode interference (MMI) couplers are used as the splitters in the MZI because the directional coupler-based splitter (used for the MOS capacitor device) for the small waveguide size used here requires very fine lithography resolution to keep excess optical loss at a minimum. The on-chip insertion loss is ~4 dB, when the MZI is in the "on" state, which is defined here as the maximum optical output intensity of the MZI. This on-chip insertion loss (excluding coupling loss) includes ~1 dB passive waveguide transmission loss, ~0.5 dB MMI coupler loss, and ~2.5 dB phase shifter loss, which can be attributed primarily to the dopants. The passive waveguide and phase shifter losses are measured using the well-known cutback method [33], and the MMI coupler loss is determined by comparing its transmission to that of straight reference waveguides.

3.3. High-speed performance

As described in Section 3.1, the metal electrodes have been designed to give high-bandwidth performance. Both modeling and measurements show that the capacitance of



(a) 1 mm phase shifter at 40 Gbps. Single-ended drive signal = 6.2 V_{pp} with DC bias of 3.1 V. Measured ER = 1.1 dB



(b) 3 mm phase shifter at 10 Gbps. Dual drive signal = 7.6 V_{pp} differential with DC bias of 2 V. Measured ER = 5.2 dB

Figure 11: Optical eye diagram of the PN-diode-based modulator.

this device is an order of magnitude smaller than the MOS capacitor-based modulator. However, it is imperative to ensure proper termination of the modulator transmission line in order to suppress the RF signal reflection from the end of the traveling-wave electrode. In our experiment, we have used two different approaches for device termination. One approach is to flip-chip bond the silicon MZI modulator chip to a printed circuit board (PCB) and surface mount external resistors on the PCB traces that are connected to the output end of the modulator electrode. The PCB is designed for high-speed performance with PCB traces having ~0.3 dB/cm RF loss and 50 ohm impedance at 40 GHz and is used with low RF loss connectors. The other approach for terminating the device is to monolithically integrate a thin-film resistor with the silicon modulator die. For our MZI devices, we used titanium nitride (TiN) as the resistor material.

The high-frequency performance of the silicon modulator has been characterized by measuring both its 3 dB frequency roll-off and data transmission capability. The MZI silicon modulator used for the high-speed experiments contains a 1 mm long phase shifter in each arm. The RF signal from either a signal generator or a pseudorandom bit sequence (PRBS) generator is amplified using a commercially available modulator driver. For single-ended drive, the amplified output of 6.2 V_{pp} is combined with 3.1 V_{DC} using a bias tee to ensure reverse bias operation for the entire AC voltage swing. (For dual drive, we use an RF signal of ~7.6 V_{pp} differential with each arm biased at ~2 V_{DC}.) This DC-coupled signal is connected to the input of the traveling-wave electrode of one of the phase shifters via the PCB connector or a GSG probe with RF insertion loss of <1 dB up to 50 GHz. The output of the electrode is terminated with a 14 Ω load. A continuous-wave laser beam at ~1550 nm is coupled into the silicon modulator via a lensed fiber. The modulated optical output is collected using another lensed fiber and is connected to a 53 GHz digital communications analyzer (DCA) optical module.

For the optical frequency roll-off measurement, the signal generator is swept from 100 MHz to 44 GHz. The input drive signal is first measured as a function of frequency using a DCA electrical module with 63 GHz bandwidth. This DC-coupled RF signal is then applied to the modulator and the modulated optical signal is also measured as a function of frequency. To obtain the frequency response of the MZI modulator for a constant input drive voltage, the optical output is normalized by the measured input drive voltage for all frequencies. The results for the frequency roll-off measurements for both the devices packaged on a PCB as well as that with on-chip resistors are plotted in Figure 10, where we can see that both the devices have a 3-dB roll-off frequency of >30 GHz.

The high-speed data transmission performance of the MZI modulator was measured using a PRBS source with [2^{31}−1] pattern length as the RF input. The MZIs have been designed such that both arms can be driven in a push-pull configuration but can be driven more simply in the single-ended configuration as well. The high-speed testing of the device on the PCB was performed using a single-ended drive scheme, while the device with the on-chip termination was driven differentially. Figure 11(a) shows the eye diagram of the modulator optical output at a bit rate of 40 Gb/s. The ER is measured to be 1.1 dB with a rise/fall time of ~14 ps. The open eye diagram proves that the modulator is capable of transmitting data at 40 Gb/s, which is consistent with the 3 dB roll-off frequency of >30 GHz.

Demonstration of such high-speed data transmission represents a significant leap in silicon modulator performance and is a testament to the success of the steps taken to extend the bandwidth beyond 10 Gbps. However, the demonstrated performance above is, by no means, the fundamental limit and there is a lot of room for improvement. For example, the ER can be significantly improved by optimizing the pn-junction location, which alone can lead to ~30% improvement in phase efficiency based on our simulation results.

Another approach toward increasing the ER is to increase the length of the phase shifter contained in the MZI. However, this comes with the trade-off of a larger RF signal attenuation, which limits the data rate to a lower value. Figure 11(b) shows the measured eye diagram at 10 Gbps for an MZI with a 3 mm phase shifter section, which gives an ER of ~5.2 dB for a 7.6 V_{pp} differential drive with each arm biased at 2 V_{DC}. Increasing the data rate beyond 10 Gbps rapidly closes the eye due to insufficient bandwidth. One way to overcome the bandwidth limitation would be to break up the 3 mm phase shifter into three smaller segments of 1 mm each and drive every segment with the same signal. This configuration can be expected to give an ER of ~5 dB even for ~40 Gbps since the bandwidth is now determined by that of a 1 mm device, which has already been shown to be >30 GHz. This is identical to the approach taken for the MOS capacitor which has already been successfully demonstrated. Analogously, the total phase shifter length in the MZI can be further increased to 5 or even 10 mm to give larger extinction ratios, while still maintaining individual segment length at 1 mm. The limitations now become the optical loss, and the increase in driver and packaging complexity.

4. CONCLUSIONS

In this paper, we have presented two implementations of silicon optical modulators, both based on the free carrier plasma dispersion effect. One of them is based on an MOS capacitor operating in the accumulation mode, while the other incorporates a pn-diode operating in the carrier depletion mode. The MOS capacitor-based device was the world's first silicon optical modulator to give data transmission at 10 Gbps. Transmission line implementation of the pn-diode-based modulator helped us push the bandwidths even higher to demonstrate 40 Gbps data transmission and provide a more frequency scalable option for optical modulators. Several straightforward options have been suggested for improving the performance further in terms of the phase efficiency and the achievable extinction ratio. The developments in the silicon optical modulator described in this paper indicate that reaching the performance levels demonstrated so far by other materials is now a forthcoming reality, thus providing a huge impetus toward driving optical interconnects in future terascale microprocessors.

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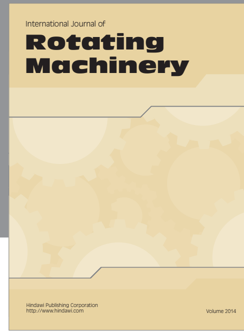
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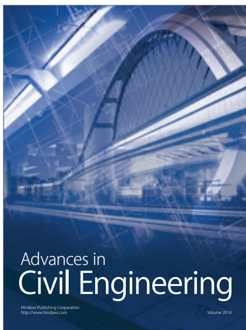
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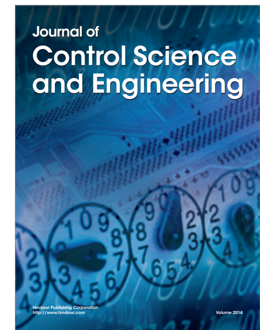
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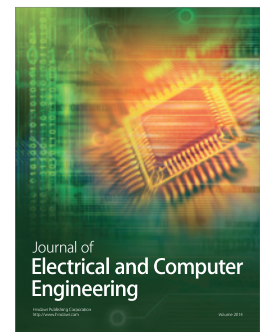
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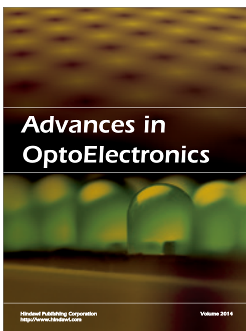
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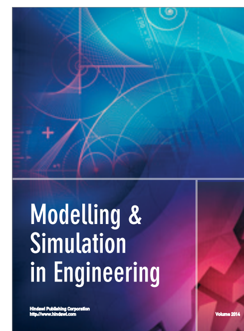
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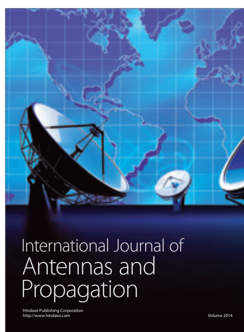
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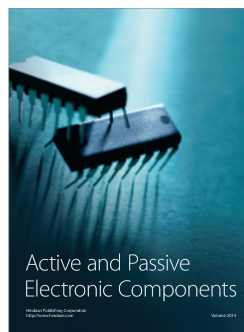
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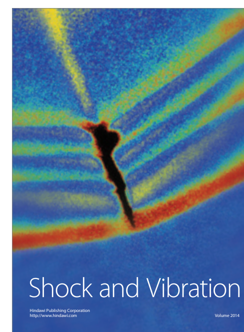
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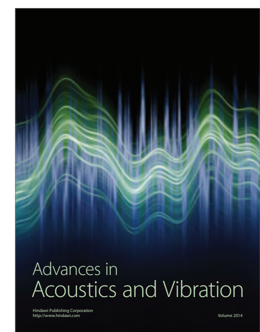
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