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Research Article

Silicon Carbide Emitter Turn-Off Thyristor

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A novel MOS-controlled SiC thyristor device, the SiC emitter turn-off thyristor (ETO) is a promising technology for future high-voltage switching applications because it integrates the excellent current conduction capability of a SiC thyristor with a simple MOS-control interface. Through unity-gain turn-off, the SiC ETO also achieves excellent Safe Operation Area (SOA) and faster switching speeds than silicon ETOs. The world's first 4.5-kV SiC ETO prototype shows a forward voltage drop of 4.26 V at 26.5 A/cm^2 current density at room and elevated temperatures. Tested in an inductive circuit with a 2.5 kV DC link voltage and a 9.56-A load current, the SiC ETO shows a fast turn-off time of 1.63 microseconds and a low 9.88 mJ turn-off energy. The low switching loss indicates that the SiC ETO could operate at about 4 kHz if 100 W/cm^2 conduction and the 100 W/cm^2 turn-off losses can be removed by the thermal management system. This frequency capability is about 4 times higher than 4.5-kV-class silicon power devices. The preliminary demonstration shows that the SiC ETO is a promising candidate for high-frequency, high-voltage power conversion applications, and additional developments to optimize the device for higher voltage (>5 kV) and higher frequency (10 kHz) are needed.

1. INTRODUCTION

Although silicon power devices have served the power electronics industry well for over five decades, silicon-based technology is reaching its physical limits for power handling and switching frequency speed. To our knowledge, a summary of the capability of today's silicon-based, high-power devices, is shown in Figure 1. Although these silicon devices have achieved very large power handling capability by increasing current handling to more than 1500 A per device, their voltage capability is typically below 4.5 kV and their frequency capability is below 1 kHz. Also, these silicon power devices normally cannot be used at temperatures higher than 125°C in power electronic systems.

The demand for smaller, higher power density power systems requires the development of novel power semiconductor devices capable of operating at higher frequencies, higher voltages, and higher temperatures. Wide-bandgap SiC material is the most promising of the postsilicon alternatives because of its superior properties (e.g., ten times higher breakdown electric field, higher thermal conductivity, and much lower intrinsic carrier concentration). We summarize the calculated capability of SiC power devices in terms of power handling capability and switching frequency, as shown in Figure 2. The picture and performance of SiC MOSFET can be referred to the previous work of Ryu et al. [1]. Power handling capability is expressed in W/cm^2 because, due to the immature material growth technology that limits the maximum size of the device, today's SiC power devices are manufactured in much smaller die sizes than comparable silicon devices. Based strictly on the material properties, however, SiC power devices can potentially handle three times more power and can switch ten times faster than comparably rated silicon devices. The self-heating induced by their larger power losses at higher frequency operation results in their higher junction operating temperature (around 225°C), so their high temperature operation capability improve their power and frequency capability.

Beginning in the 1990s, continued improvements in SiC single-crystal wafers have resulted in significant progress toward the development of low-defect, thick-epitaxial SiC materials, and high-voltage SiC devices [2, 3], including the

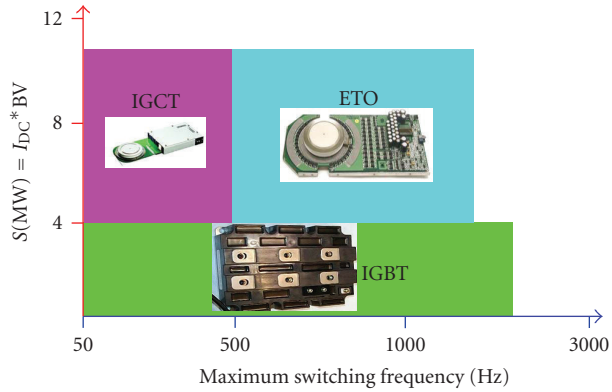

Figure 1: Comparison of the power and frequency capabilities of today's silicon power devices.

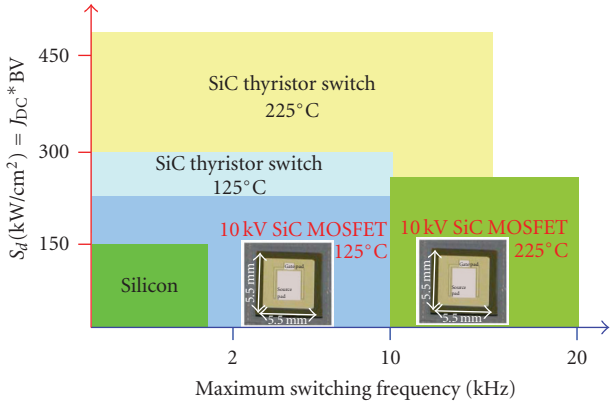

Figure 2: Calculated SiC power device power versus frequency capability.

development of a 7-kV gate turn-off (GTO) thyristor [4], 10-kV SiC MOSFETs [1], and 13-kV insulated gate bipolar transistor (IGBT) [5]. Among the high-voltage SiC devices whose properties have been experimentally verified, SiC MOS devices suffer from poor channel mobility and poor oxide reliability at high temperatures [6, 7]. Additionally, the on-state resistance of the SiC MOSFET and the bipolar IGBT device both increase significantly as the blocking voltage (>5 kV) and operating temperature increase. In contrast, the SiC thyristor, with its double-side carrier injection and stronger conductivity-modulated drift region, maintains a low forward voltage drop even at 200°C. Simulation studies by the authors also indicate that, even at 10 to 15 kV levels, the SiC thyristors still exhibit excellent conduction and switching performance. It is therefore clear that SiC thyristor is one of the most promising devices for high-power applications.

In such applications, however, the SiC thyristor has the same drawbacks as a silicon-based GTO (e.g., current controlled turn-on and turn-off, the need for a turn-on *di/dt* snubber, and, sometimes, a turn-off *dv/dt* snubber). The ETO was developed to avoid these drawbacks and to meet the demands of advanced power conversion applications

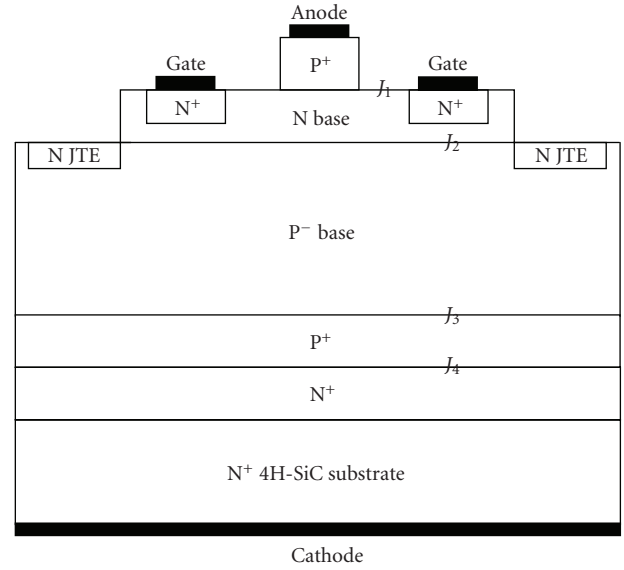

Figure 3: p-type SiC GTO structure used in the first SiC ETO demonstration [12].

[8]. The ETO is an MOS-bipolar high-power semiconductor device with high-current/voltage capability of a thyristor and the simple MOS control interface. Theoretical analysis and experimental results on silicon-based ETO devices have shown that the ETO technology can achieve MOS gate control, better SOA, current saturation capability, and faster switching speed [8–11].

The innovative ETO concept can also be applied to the SiC thyristor technology. By integrating a high-voltage SiC GTO with the mature silicon power MOSFET technology, the SiC ETO is expected not only to simplify the user interface, but also to improve the speed and dynamic performance of the device.

2. ETO DEVICE OPERATION PRINCIPLE AND EXPERIMENT DETAILS

The SiC ETO is most suitable for high-voltage applications (5 to 15 kV). These applications maximize the benefits of the SiC-based device while requiring less current in any given application. The lower current requirement is attractive as it compensates somewhat the current issues in increasing the die size of SiC-power devices.

The world's first SiC ETO, reported here, is a 4.5 kV prototype based on a 4.5 kV GTO thyristor manufactured by Cree Inc.(Durham, NC, USA) [12]. As shown in Figure 3, the GTO structure is different from the conventional pnpn structure used in silicon GTO. The SiC GTO is a p-type thyristor that uses an npnp thyristor structure because only n^+ substrate is currently available. The emitters of the upper pnp and lower npn transistors form the anode and cathode, respectively, and the upper base forms the gate contact.

Figure 4 shows the equivalent circuit of the SiC ETO based on the above p-type SiC GTO. The p-type GTO is connected in series with an emitter switch (Q_e), and a gate

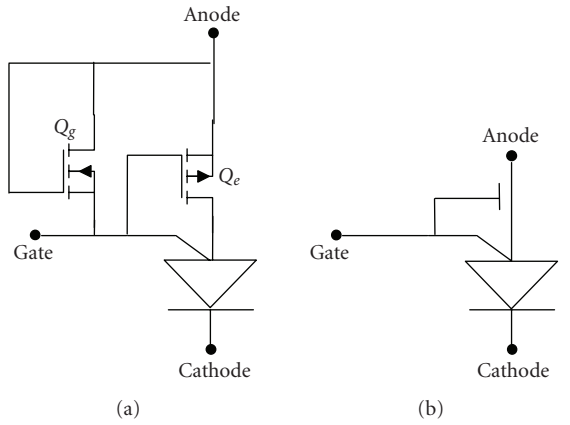

Figure 4: (a) p-type ETO equivalent circuit and (b) corresponding ETO symbol.

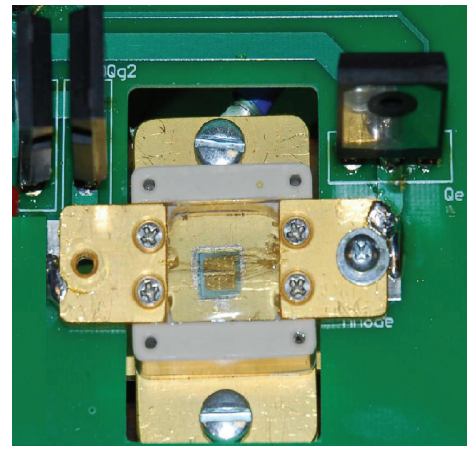

Figure 5: 4.5-kV SiC ETO prototype.

switch (Q_g) is connected to its gate. The resulting SiC ETO is a three-terminal device. During the turn-off transient, the turn-off of the emitter switch cuts off the GTO's anode current path and the anode current is commutated to the gate path before the cathode voltage starts to decrease. In this way, the hard-driven turn-off (or unity-gain turn-off) condition is realized, and the whole turn-off process is like an open-base npn transistor turn-off. The open-base npn transistor turn-off means that no thyristor latch-up mechanism exists during the turn-off, which ensures a uniform transient process without current filamentation. Thus, the maximum turn-off current dramatically increases, resulting in a wider SOA. The SiC ETO also improves the turn-off speed because of the rapid extraction of stored charge by such a large gate current.

In the SiC ETO, the emitter switch (Q_e) and gate switch (Q_g) make use of the mature silicon power MOSFET because neither are subjected to high voltages. The gate switch is connected as a gate-drain shorted diode. When the GTO gate voltage is smaller than the threshold voltage of gate switch, it conducts and the gate voltage of the SiC GTO is hence clamped at a value slightly lower than its threshold voltage. Because the inner structure of the SiC GTO's gate-anode is a pn junction, the maximum voltage applied to the emitter switch therefore cannot exceed that of the gate switch during the turn-off.

The developed prototype ETO device is shown in Figure 5. The SiC ETO comprises the power packaged SiC GTO [12] in series with the TO-247 AD packaged silicon power MOSFETs. The distance between the SiC GTO and silicon power MOSFETs is very small in order to reduce the stray inductance. Similar to the mechanical structure of Si ETO [9], a copper board with thermally conductive and electrically insulated dry-to-touch thermal interface pad in its bottom can be attached to the package base plate below the cathode of SiC GTO, so that heat can be dissipated through heat-sink, and another copper board can be attached to the drain of silicon power MOSFETs if they are surface mounted. Because the power losses in silicon power MOSFETs are much smaller than that of SiC GTO, the heat isolation between SiC GTO and silicon power MOSFETs can enable SiC GTO high temperature operation (>150°C), while keeping silicon power MOSFETs in lower junction operating temperature (<150°C). An isolated gate driver is used to drive the SiC ETO. In the clamped inductive load circuit, an air-core 2.8-mH inductance is used as the load inductor, and a 10-kV SiC junction barrier Schottky (JBS) diode from Cree Inc. is used as the freewheeling diode. The tests were conducted at a DC-link voltage of 2.5 kV.

3. RESULTS AND DISCUSSION

The forward I-V characteristics for the 6 mm × 6 mm SiC GTO at elevated temperatures are shown in Figure 6(a). The devices show a forward current of −9 A (−25 A/cm^2) with a voltage drop of −4.2 V at −100 mA gate drive current and room temperature. The insignificant reduction of the slope of I-V curve after knee voltage with temperature indicates the increase of carrier lifetime with the temperature since the carrier mobility reduces with the increase of temperature. The reduction of turn-on knee voltage indicates the reduction of built-in potential of p-n junction with the increase of temperature. The device shows a negative temperature coefficient due to the increase of carrier lifetime and the decrease of built-in potential of p-n junction with the increase of temperature.

The forward I-V characteristics of the three-terminal SiC ETO are shown in Figure 6(b). Compared to the GTO test results, there is no visible increase of the forward voltage, which indicates that the ETO preserved the excellent conduction capability of the GTO device. The integrated MOSFET contributes to only a small increase in the forward voltage drop. At elevated temperatures, the increase of ON-state resistance in the silicon MOSFET compensates for the reduced ON-state voltage in the SiC GTO, thus reducing the temperature coefficient of the hybrid device.

For the switching test, the SiC ETO is in the forward blocking state initially and most DC-link voltage is applied to the SiC GTO in the clamped inductive load circuit. After applying the turn-on optical pulse, a 100-mA gate current is injected into the GTO to turn on the GTO and −15 V is applied to Q_e (a p-channel MOSFET) to turn it on. After Q_e

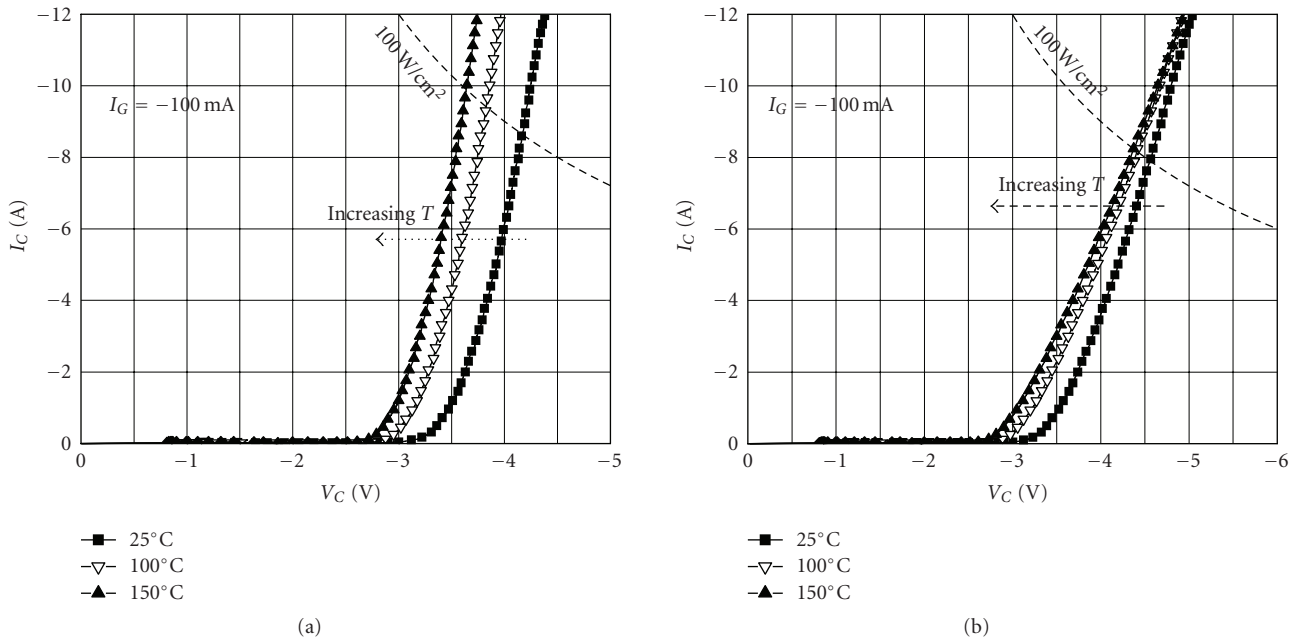

FIGURE 6: (a) SiC GTO I-V characteristics and (b) SiC ETO I-V characteristics.

and the GTO are on, the inductor current increases linearly until the turn-off signal. In the conduction state, the forward voltage drop of the SiC ETO equals the voltage drop of the SiC GTO plus the voltage drop of Q_e, so the forward voltage of the SiC ETO is 4.6 V at a current density of 26.5 A/cm^2.

Turn-off starts when the optical pulse is removed and Q_e turns off. A detailed waveform of the SiC ETO turning off 9.5 A is shown in Figure 7, where V_C, V_G, I_C, and V_A represent cathode voltage, gate driver signal, cathode current, and anode voltage, individually. Several important time instances occur during the snubberless turn-off of the SiC ETO. The turn-off operation begins from time = t_0 when the gate driver signal of the gate switch (Q_g) starts to rise from −15 V to 0. Thereafter, Q_e is turned off. In the period t_0-t_1, the voltage on Q_e increases. Because the internal structure of the SiC GTO gate anode is a pn junction, the voltage rise in Q_e will turn on Q_g. During this time, the current in the anode (p^+ emitter) will be commutated to the gate switch until finally the anode current becomes zero at $t = t_1$. At t_1, the ETO achieves unity-gain turn-off and the device operates like an open-base npn transistor. Once the unity-gain turn-off is established, the hole injection at the emitter of the upper pnp transistor stops. The absence of hole injection results in a net extraction of excess carriers from the n base because the cathode current (I_C) has to be maintained and equals to the inductive current. In the time period t_1-t_2, the minority carriers in the n-base region are pulled out by the current ($\alpha_{PNP} \cdot I_C$) until t_2 when the main junction J_2 is recovered from forward bias to reverse bias. From t_2 to t_3, the minority carriers in the p drift region and p buffer region are swept out, while the voltage increases to the DC-link voltage value due to the formation and expansion of the depletion region on the p-side of J_2 junction. In the time period t_3-t_4, because no more base current is being injected into the base

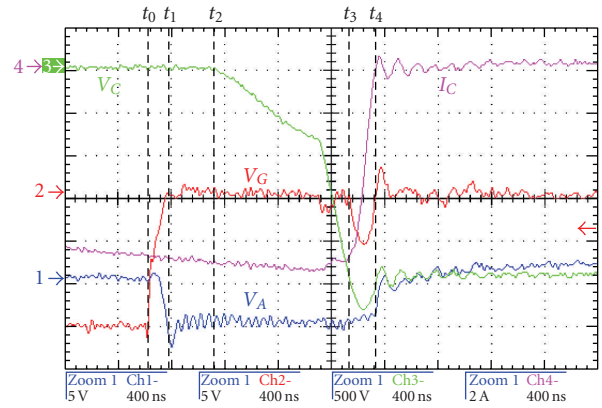

FIGURE 7: Turn-off waveforms for the 4.5-kV SiC ETO.

of the lower npn transistor, the cathode current falls to 0 rapidly and a cathode voltage spike appears due to the stray inductance. Finally after t_4, the cathode voltage remains high and the cathode current decreases quickly, as determined by minority carrier recombination in the undepleted p buffer region.

In the turn-off waveforms shown in Figure 7, the storage time of the SiC ETO is 504 nanoseconds from time interval t_0–t_2. The total cathode voltage rise time is 980 nanoseconds from time interval t_2-t_3. The voltage rise process is separated into two stages. First, there is a slow rise of cathode voltage up to −820 V ($dV_c/dt \approx 1$ kV/μs) from time interval t_2–t_{22}. This is followed by a fast voltage rise ($dV_c/dt \approx 8.8$ kV/μs) from time interval time interval t_{22}–t_3. When the cathode voltage increases to −820 V, the p-base region is fully depleted. The stored minority carriers in the heavily doped p buffer are fewer than those in the p-drift layer

and are also recombined at a faster speed due to their much shorter lifetime; the shorter lifetime greatly reduces the excess carriers' extraction time in this phase resulting in a faster voltage rise. After the cathode voltage increases to the DC-link voltage value, the clamped diode starts to conduct and the cathode current decreases. The cathode current decay rate (di_c/dt) is 42.6 A/μs. The di_c/dt-induced cathode voltage spike reaches −2.8 kV. The total current fall time is 142 nanoseconds. The total turn-off time is 1.63 microseconds, and the total turn-off energy is 9.88 mJ. This turn-off loss is about a factor of five lower than that of a 4.5-kV silicon-based ETO. It indicates that the prototype SiC ETO can operate at about 4 kHz with around 125°C junction temperature when a conventional cooling system is used to dissipate 100 W/cm^2 conduction loss and 100 W/cm^2 turn-off loss. Based strictly on the material properties, SiC power devices can theoretically operate above 400°C and potentially handle three times more power. Higher operation frequency of the SiC ETO (around 8 kHz) can be expected if its high temperature operation capability is utilized because the self-heating induced by its larger power loss at higher frequency operation results in higher junction operating temperature (around 225°C).

Further improvement in the SiC ETO switching speed is also possible. Most of the turn-off loss of the tested SiC ETO arises in the first period of cathode voltage rise. During this stage, the total cathode current is almost keep constant, and only the hole current, $(1 - \alpha_{\mathrm{NPN}}) \cdot I_C$, is useful in extracting the excess carriers. In the prototype device, this current is not optimized and not high enough, resulting in slower voltage rise and, consequently, higher turn-off loss. A faster excess carrier extraction rate would greatly improve the rate of depletion region expansion and thus the cathode voltage rise rate (dV_c/dt). So, a smaller npn transistor common base current gain (α_{PNP}) or a higher upper transistor gain (α_{NPN}) would help to improve the turn-off speed and reduce turn-off loss. In other words, a stronger upper transistor design is needed. Implementation of such a design would favor an n-type thyristor structure using pnpn structure, where the upper transistor is an npn transistor. This change would require a p^+ type SiC substrate, a challenge that remains to be overcome by future research.

4. CONCLUSIONS

The SiC ETO is a novel three-terminal MOS-controlled device. It makes use of the high-voltage blocking and excellent current conduction capability of SiC thyristor, and the easy drive interface of an MOSFET. The 4.5 kV prototype reported here demonstrates SiC ETO operation and its improved switching performance compared with a silicon ETO. Further efforts are being made to develop higher voltage (>5 kV) and higher frequency (10 kHz) SiC ETO devices.

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