

Research Article

Integrated VCOs for Medical Implant Transceivers

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The 402–405 MHz medical implant communication service (MICS) band has recently been allocated by the US Federal Communication Commission (FCC) with the potential to replace the low-frequency inductive coupling techniques in implantable devices. This band was particularly chosen to provide full-integration, low-power, faster data transfer, and longer communication range. This paper investigates the design of a voltage-controlled oscillator (VCO) that will be an essential building block of such wireless implantable devices operating in the MICS service band. Three different integrated quadrature VCOs that meet the requirements of the MICS standard are designed in 0.18 μm TSMC CMOS process to propose an optimum choice. Their performances in terms of power consumption, die area, linearity, and phase noise are compared. The fabricated VCOs are a four-stage differential ring VCO, an LC tank VCO directly loaded with a poly-phase filter, and an 800 MHz LC tank VCO with a high-frequency master-slave divider. All three architectures target a VCO gain of $K_{\text{vco}} = 15 \text{ MHz/V}$ with 3 calibration control and 2 frequency-shift keying (FSK) control signals and are designed for 1.5 V supply voltage in a 0.18- μm standard CMOS process.

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1. INTRODUCTION

Design of implantable miniature devices to be able to record or to transmit real-time physiologic parameters (e.g., ECG, EEG, EOG, EMG, Neural, Blood Flow, Blood Pressure, etc.) from a patient body in medical environments is becoming very important research area. FCC has recently allocated a new band at 402–405 MHz with 300 kHz channels to enable the wireless communication of such implantable devices to deliver high level of comfort, mobility, and better patient care [1]. In addition to medical implants, metrological aids service has primary allocation at 402–405 MHz band and the Earth exploration-satellite service together with metrological-satellite service has secondary allocation at 402–403 MHz [2]. With the advance of radio frequency IC (RFIC) technology, this frequency band promises high-level integration (compared to inductive link designs) which results in miniaturization and low-power consumption. In addition, there exist relatively insignificant penetration loss at these frequencies (10 dB with 10 mm tissue penetration) [3] and is therefore very suitable for the above applications. Although higher frequency causes higher penetration loss, high-level integration becomes difficult at low frequencies. Moreover, a small antenna design is also difficult at lower frequencies

[4]. Combining all these with the availability of the 402–403 MHz band internationally, this frequency band offers an attractive choice for future medical implant devices [5].

Low power consumption and full integration are the most critical targets for implantable transceivers. Recently, some low-power CMOS transceivers, working at 433 MHz and 435 MHz bands, have been reported [6–8]. These designs achieve low-power operation, leaving the matching networks or voltage-controlled oscillator (VCO) tank inductor off-chip. As the size of an implantable transceiver is required to be low, the VCOs presented in this paper are designed as fully integrated. A direct conversion frequency-shift-keyed (FSK) transceiver shown in Figure 1 is selected for a low-power implantation because of the simple demodulation process of FSK signals when used with an I/Q direct conversion architecture [5, 9]. The system in Figure 1 is based on a half full-duplex communication system, namely, it does not receive and transmit at the same time. In the receive mode, the VCO is in the PLL loop. In the transmit mode of the architecture, the PLL loop opens and the base-band digital data directly modulate the VCO with an offset tone of $\pm\Delta f = 70 \text{ kHz}$ fitting optimally into one of ten 300 kHz channels. The technique can easily be used for other modulation schemes as well (e.g., AM/FM/PM, etc.). Herein, we are

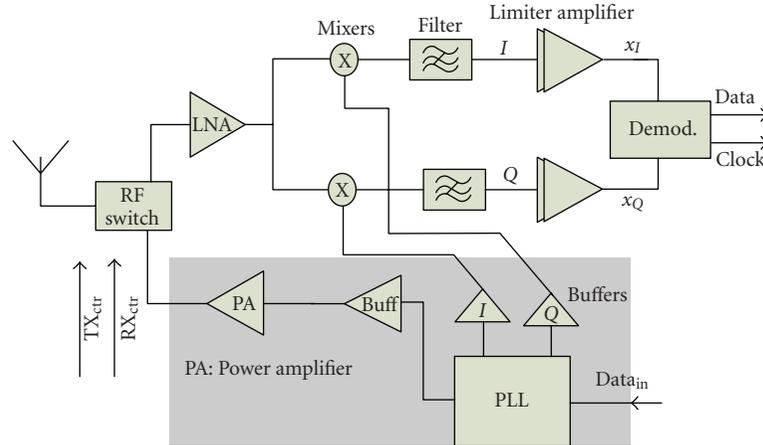


FIGURE 1: Block diagram of an MICS transceiver. The shadow area shows the transmitter part.

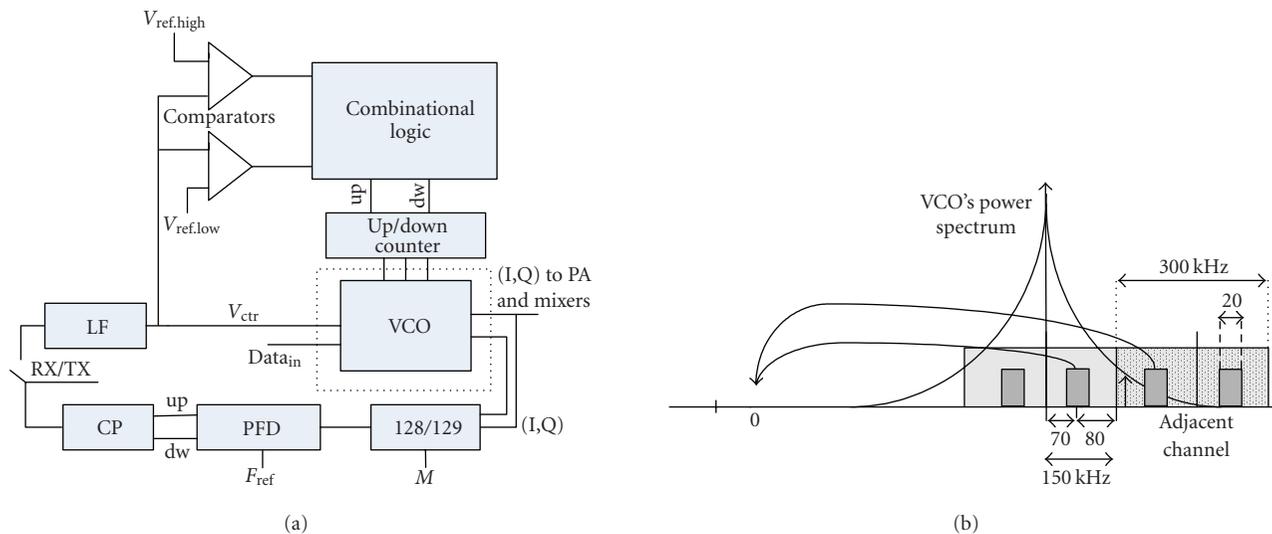


FIGURE 2: PLL architecture, (a) block diagram for the PLL with calibration, (b) down conversion of the adjacent channel by the phase noise.

mainly interested in the direct modulation of VCOs for FSK signals because of the relaxed bandwidth requirements per channel (20 kb/s maximum data rate). When the input to the VCOs is analog data, then an FM modulated signal will be generated [10]. The detailed specifications of the proposed architecture were discussed in [11].

The rest of the paper is organized as follows. Section 2 discusses the details of the phase-locked loop (PLL) architecture for an MICS transceiver. In Section 3, the design including a 402 MHz VCO directly loaded with a single-stage poly phase filter is presented. In Section 4, the performance of an 800 MHz VCO followed by a high frequency master-slave divider is discussed. Section 5 presents a four-stage differential ring VCO as a very low-power candidate for the implantable devices in the MICS band. Section 6 is the conclusion that does a performance comparison of the three different architectures targeting the same specifications with a minimal power.

2. PLL ARCHITECTURE

The block diagram of the target PLL architecture for this application is shown in Figure 2(a). A choice of fractional-N PLL with 128/129 division ratio is considered with a reference oscillator of ~ 3.14 MHz. With this selection, the whole 3-MHz MICS band (420–405 MHz) is covered. All of the VCOs designed here employ direct modulation, where the base-band data arrange the frequency tones of FSK signals in the transmit mode. To utilize a precise reference frequency, crystal oscillators are generally used, but they increase the package size. We are investigating alternate methods such as using an on-chip temperature compensated relaxation oscillator. The main reason for choosing the proposed architecture in Figure 2(a) is to have an on-chip temperature compensated relaxation oscillator to generate the frequency reference instead of a bulky off-chip crystal. Some designs reported in the literature have successfully

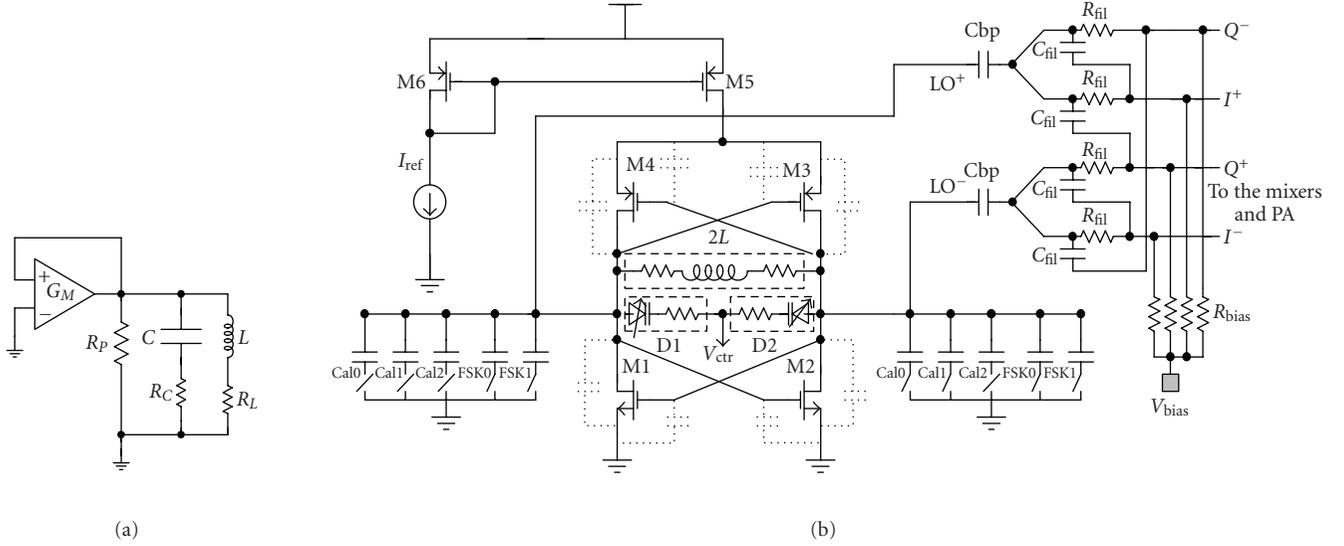


FIGURE 3: (a) Basic LC-tank oscillator configuration with tank parasitics, (b) schematic of a VCO directly loaded with poly-phase filter.

demonstrated sub-100 ppm accuracy across temperature and supply variations [12, 13]. Such an integrated device would inevitably contribute substantial phase noise. Direct open loop modulation of the VCO in the transmit mode and very low loop bandwidth PLL can alleviate this problem.

In order to minimize the center frequency variations in the transmit mode, the VCO gain is kept very low. This reduces the susceptibility of the oscillation frequency to the noise on the control voltage. However, having a narrow tuning range might leave the VCO frequency range out of the desired band, considering the effect of process variations. To prevent this to happen, a second static calibration loop is utilized to maintain the VCO frequency in the desired range. Two comparators track the control voltage and step the VCO frequency up or down with three-bit resolution, in case the control voltage exceeds the predefined limits. Total of 8 overlapping frequency clusters provides large enough overall tuning range while still keeping the VCO gain very low in every cluster. Overlapping regions between the clusters should be kept large enough to prevent unstable switching among the clusters due to noise and temperature variations. Moreover, by setting the thresholds of these comparators properly, the VCO is easily kept in the linear regions of its total tuning range.

Unlike the other mobile communication circuits, the phase noise requirement of a VCO for the targeted application (i.e., MICS regulation) is not stringent due to the low regulated power and short communication distance [5]. Because of the fixed distance and upper bound on EIRP (equivalent isotropically radiated power), the dynamic range is not too high (set by the path loss in 2 m, ~ 30 dB [11]). For this reason, the down conversion of the noise in the adjacent channel due to the phase noise of the oscillator is not very detrimental (except strong outside interferers). Assuming a signal-to-noise ratio (SNR) of 10 dB due to the next channel, the phase noise requirement of the VCO can be driven with

the help of Figure 2(b) as [14]

$$\begin{aligned} L(160 \text{ kHz}) &= -30 - 10 - 10 \log 20000 \\ &= -83 \text{ dBc/Hz}, \end{aligned} \quad (1)$$

where the transmission data rate is selected 20 kb/s to cover the majority of physiological signals [3, 8, 11]. All of the different VCOs presented in the following sections were designed for the same specifications described so far, targeting the minimum power consumption with 3-bit calibration control (~ 15 MHz/V VCO gain in every cluster) and 2-bit FSK control ($\pm \Delta f = 70$ kHz to 80 kHz). They are followed by the same two-stage single-ended power amplifier carefully sized to deliver around -7 dBm power to a $50\text{-}\Omega$ antenna with an integrated 13.9-nH RF-choke spiral inductor and 9-pF by-pass capacitors (MIM). This output stage consumes 2.2 mA current from a 1.5 V supply.

3. A 400 MHz LC TANK VCO DIRECTLY LOADED WITH A POLY-PHASE FILTER

In this section, the circuit design parameters and the measurement results of a poly-phase filter loaded 400 MHz LC tank VCO are discussed.

3.1. Circuit design

As shown in Figure 3(b), a topology that uses nMOS-pMOS cross-coupled pairs with pMOS tail current source was chosen for the core VCO design. Using both nMOS and pMOS pair gives double amplification for a given current. In addition, this circuit can be optimized to have more symmetry in the output waveform leading to a further phase noise reduction [15]. Due to its lower flicker noise pMOS transistor was used as a tail current source.

For a given process and VCO topology, enlarging the oscillation amplitude is a very efficient way of reducing

the phase noise [16]. For a given current level, this can be achieved by maximizing the values of the resonant tank inductors [17]. However, there are some serious limitations on the value of the inductor if the inductor is to be integrated in a CMOS process. As the value of the inductance in a spiral inductor increases, the resistive losses associated with it would degrade the Q of this inductor, which is the most important phase noise source in a fully integrated VCO. Thus, it is desirable to construct large inductors with very low resistive losses [16]. An 8-turn 22.4 nH spiral inductor with a trace width of $w = 12 \mu\text{m}$ and gap of $s = 1.5 \mu\text{m}$ is used for this design. Only the top metal layer (metal6) was used for the spirals which would result in a total series resistance of $R_{\text{ind}} = 20 \Omega$ at 400 MHz. The quality factor of this inductor at 400 MHz is 5.2. The total tank capacitance corresponding to this inductance value is $C_{\text{tot}} = 7.07 \text{ pF}$. This total capacitance represents all the parasitic capacitances associated with the FETs, capacitive loading due to poly-phase filter, 3-bit binary weighted MIM-Caps for calibration, and varactor diodes for tuning. Moreover, two switchable 7-fF metal2-metal3 capacitors were used for FSK modulation.

The basic configuration for an LC tank oscillator is given in Figure 3(a) [16]. To satisfy the oscillation condition, the transconductance necessary to have the unity loop gain at the oscillation frequency, ω_o , can be calculated from the transfer function as [16]

$$G_M = R_{\text{eff}}(\omega_o C)^2, \quad (2)$$

where $R_{\text{eff}} = R_C + R_L + 1/(R_P(\omega_o C)^2)$. R_P is the parallel tank resistance, R_L is the inductor series resistance, and R_C is the varactor series resistance. The most important term in determining the value of R_{eff} is the series resistance of the inductor at 400 MHz, which is approximately 20Ω . Using (1), the transconductance required to compensate the losses can be calculated as

$$G_M = 20 \Omega \cdot (2\pi \cdot 0.4 \text{ GHz} \cdot 7.07 \text{ pF})^2 = 6.5 \text{ mS}. \quad (3)$$

Therefore, each transistor should have a gm of 6.5 mS. Thus, with a safety factor of 3, the design assumes 20-mS transconductance for each device. Current required to achieve the given transconductance value with an over-drive voltage of $V_{GS} - V_T = 0.12 \text{ V}$ would be $I_D = g_m(V_{GS} - V_T)/2 \cong 1 \text{ mA}$. Hence, the total tail current of VCO core is set to be 2 mA from a 1.5-V supply during the simulations. The corresponding transistor W/L ratios are $100 \mu\text{m}/0.18 \mu\text{m}$ for nMOS pair transistors and three times bigger for the pMOS pair devices.

Using a poly-phase filter to generate quadrature phases is a popular approach for low power, I-Q mismatch tolerant applications [18, 19]. In general, these filters have low input impedance and require power hungry buffers to drive them after the VCO. They might also require buffers following them to drive the mixers (Figure 1). These buffers isolate the mixer input capacitance from the filter and also provide the signal swing required for the mixer.

For this specific application, taking advantage of relatively low operating frequency, both buffers have been

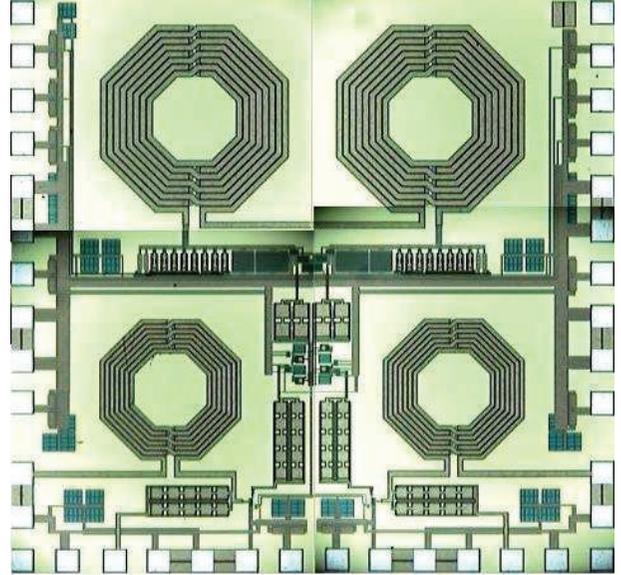


FIGURE 4: The microphotograph of the VCO directly loaded with a poly-phase filter and a two-stage power amplifier.

removed and the VCO is directly loaded with a single-stage poly-phase filter as shown in Figure 3(b) (only single stage is used to limit the filter loss). R_{fil} and C_{fil} were chosen very carefully to maximize the filter input impedance while keeping capacitance value large enough compared to total parasitic capacitance in order not to deteriorate the I-Q mismatch. The total input capacitance of mixer and power amplifier driver together with the parasitic capacitance of the poly-resistors to substrate is around 38 fF in this design. Thus, C_{fil} was chosen to be 132.7 fF (four times bigger than total parasitic capacitance) which would lead to a resistor value of $R_{\text{fil}} = 3 \text{ k}\Omega$. The filter impedance for these values can be reflected to the VCO as parallel combination of $R_p = R_{\text{fil}}(Q^2 + 1)/2 \cong 3 \text{ k}\Omega$ and $C_p = 2 \cdot C_{\text{fil}}((Q^2)/(Q^2 + 1)) = 132 \text{ fF}$ [19]. This 3 k Ω resistor value is 6 times larger than the total effective parallel tank resistance (dominated by inductor series resistance R_{ind}) $R_{\text{p tot}} = R_{\text{ind}}(Q^2 + 1) \cong 20 \Omega \cdot 25 = 500 \Omega$. Thus, the loading due to the filter impedance is negligible. The capacitive part of the filter impedance is absorbed into the total tank capacitance to generate 400 MHz center frequency.

3.2. Measurement results

The design has been fabricated in $0.18 \mu\text{m}$ TSMC CMOS process. The total die area including the bonding pads, a fully integrated power amplifier with the RF choke coil, and the by-pass capacitors is $1.2 \text{ mm} \times 1.2 \text{ mm}$ (Figure 4). LLP-40 leadless 40-pin RF package is used for the measurements. The oscillator can sustain the oscillation with a current as low as $800 \mu\text{A}$. The detailed spectrum measurements were done with a core supply current of 1.25 mA, leaving some safety margin. The measured spectrum and the tuning characteristics are shown in Figure 5. The desired tuning characteristics were obtained with a total tuning range of

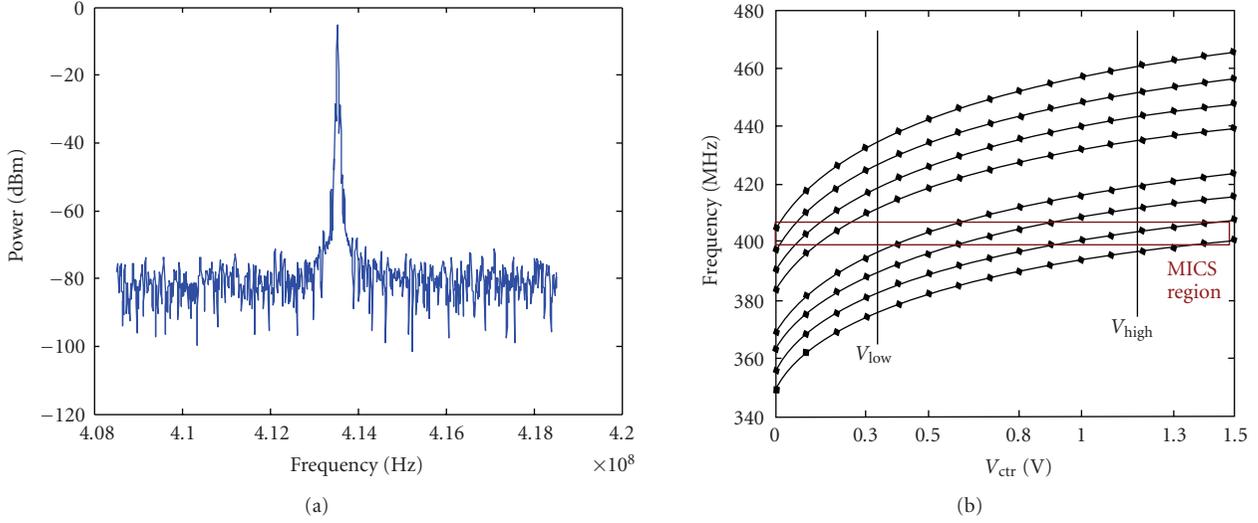


FIGURE 5: (a) The measured spectrum of the VCO with poly-phase filter, (b) the measured tuning characteristics of this VCO.

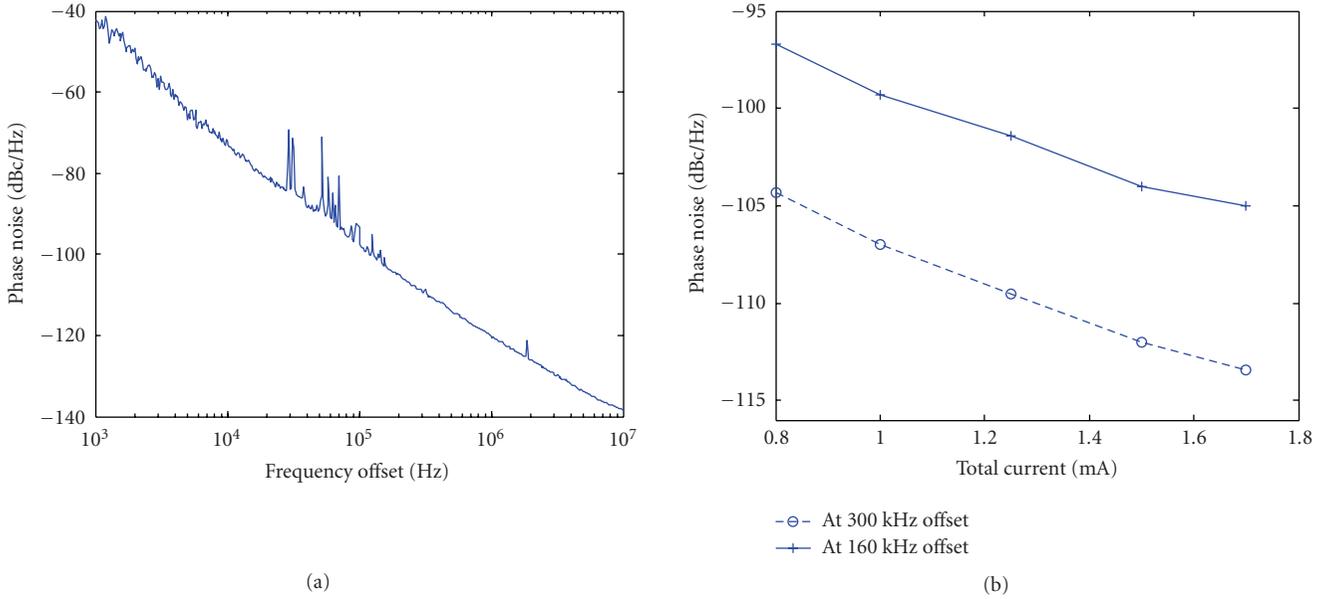


FIGURE 6: (a) The measured phase noise of the VCO with poly-phase filter, (b) phase noise for various VCO core current levels.

90 MHz spread into 3-bit controlled 8 clusters. The VCO gain inside every cluster is around 15 MHz/V as expected. Although the most significant bit (MSB) of the calibration input causes a larger step in the tuning range, a safe overlap can still be observed. The FSK control bits caused 60-kHz tones around the center frequency. Although this tone frequency still can be employed with FSK, this value can easily be tuned to the desired 70-kHz tone in the next iteration of the design by modifying the FSK capacitors. The phase noise measurement is done with Agilent E5052A. The phase noise at an offset of 160 kHz is -98 dBc/Hz, which is far below the prerequisite value for the application. The phase noise plot is shown in Figure 6(a). Figure 6(b) shows the phase noise values at the offsets of interest for various power levels.

4. AN 800 MHZ LC TANK VCO WITH A MASTER-SLAVE DIVIDER

Another way to generate quadrature signals is to use a master-slave divide-by-2 circuit following a VCO operating at double frequency. In this section, the performance of an 800 MHz LC tank VCO with an analog master-slave divider is discussed. The divider outputs drive the same mixer and power amplifier load as in the case of first design (as shown in Figure 1).

4.1. Circuit design

Since the fast analog D-flip-flops of the divider circuit needs to be driven with high swing inputs, a VCO topology with only nMOS cross-coupled pair is used to have a higher swing

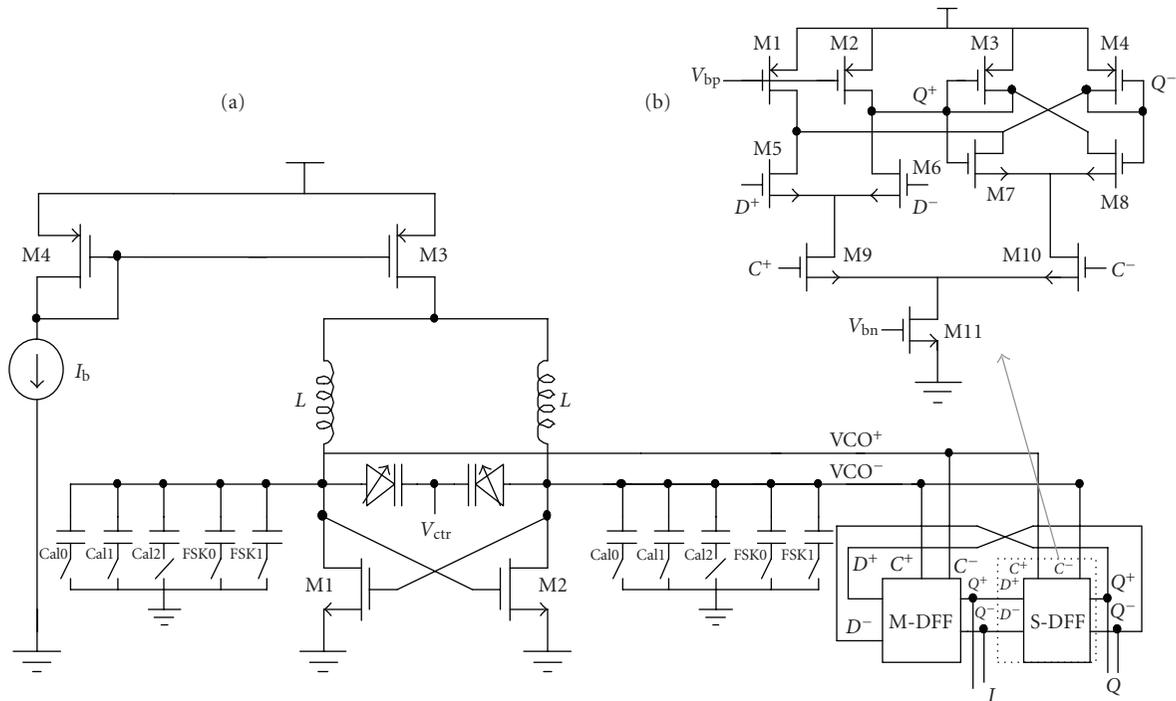


FIGURE 7: The schematic for 800 MHz VCO with master-slave divider.

at the oscillator output. The circuit schematic of the design including the divider is shown in Figure 7. Two 13.69-nH spiral inductors with 7 turns are used for this 800-MHz LC tank. The top metal (metal6) with conductor width $w = 9\ \mu\text{m}$ and conductor spacing $s = 1.5\ \mu\text{m}$ yields an effective series resistance of $13\ \Omega$. Q factor for this inductor is around 4.2 at the frequency of 800 MHz. The total of 2.89 pF tank capacitance includes varactor diode capacitances, 3-bit binary weighted switchable MIM-caps, parasitic gate-source, and drain-source capacitances of the cross coupled nMOS pair and the parasitic input gate capacitance of the divider circuit. Two 5-fF metal2-metal3 capacitances are used for direct FSK modulation by the base-band binary data. The total effective series resistance of the tank was estimated to be $16\ \Omega$ with an additional up to 3- Ω varactor series resistance. Again using (2), the overall required transconductance is calculated to be 3.36 mS. Assuming a safety factor of 3, each nMOS device of the cross-coupled pair should have a g_m of around 20 mS to sustain reliable oscillation. This transconductance value can be obtained by having 1 mA current through each branch with 120 mV overdrive voltage across 100 μm width minimum channel length nMOS devices. A current source pMOS device of 400 μm channel width and 0.3 μm channel length can support this 2-mA total current with an overdrive voltage of 140 mV.

A very common topology shown in Figure 7 was used for fast divide-by-2 operation. In this design, M3 and M4 would not allow a large voltage drop at the drains of M1 and M2, which otherwise would push M11 into triode region in case of a large VCO output driving this stage, particularly in the case of a low supply voltage. Transistors were carefully sized to achieve successful division using a 1.5-V supply

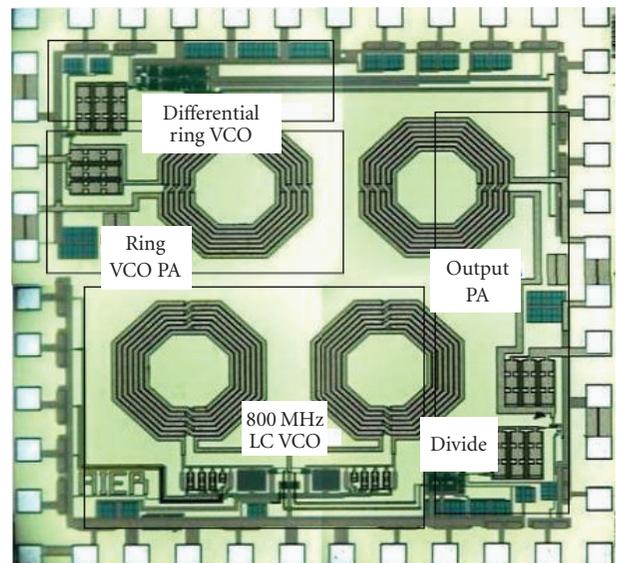


FIGURE 8: The microphotograph of the chip including an 800 MHz LC tank VCO with dividers and a four-stage differential ring VCO.

with minimum power consumption. The divider circuit can directly drive the mixers and the PA consuming 400 μA from a 1.5-V supply [20].

4.2. Measurement results

The design has been fabricated in 0.18 μm TSMC CMOS process. The total die area including the bonding pads, a fully integrated power amplifier with the RF choke coil and the by-pass capacitors is 1.1 mm \times 1.2 mm (Figure 8). The VCO

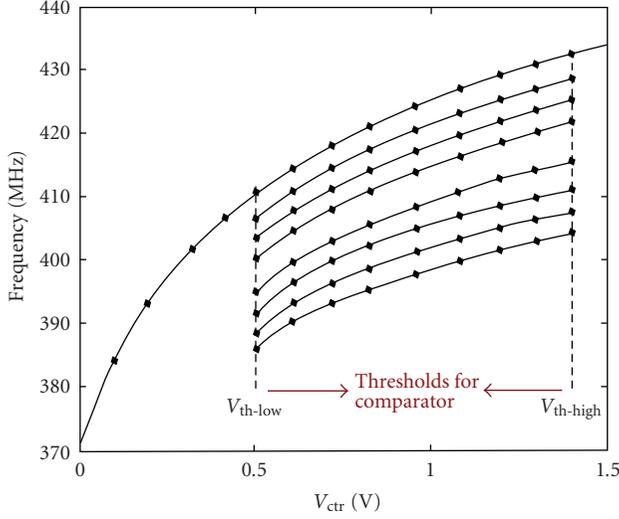


FIGURE 9: The tuning characteristic of 800 MHz oscillator followed by a divider.

core and the divider circuit consume 2.2 mA from a 1.5-V supply. The measured tuning characteristic of the design is shown in Figure 9. The desired tuning characteristics were obtained with a total tuning range of 70 MHz spread into 3-bit controlled 8 clusters. The linear tuning region of this VCO is much less compared to linear tuning range of the 400 MHz design. However, due to large overlapping margins across the clusters, the comparator thresholds can be set accordingly to keep the VCO in the linear part of the tuning curve as shown in Figure 9. The VCO gain inside every cluster is around 17 MHz/V. The FSK control bits in this case caused 120-kHz tones around the center frequency. The measured spectrum and the phase noise plot are shown in Figure 10. The phase noise at an offset of 160 kHz is -97.7 dBc/Hz, a value which is very close to the -98 dBc/Hz value obtained from the previous design.

5. A FOUR-STAGE DIFFERENTIAL RING VCO

Since the phase noise requirement of the application is relatively relaxed, the performance of a four-stage differential ring VCO is evaluated as a low power alternative to LC tank VCOs. There is no extra step to generate the quadrature outputs in the case of this four-stage ring VCO. The area of the design, most of which is occupied by the on-chip inductor of the PA, is considerably less compared to the LC tank VCOs (Figure 9). The same PA and mixer loads as in the case of LC tank designs are driven by the differential buffers following the Ring VCO.

5.1. Circuit design

Ring oscillators are generally avoided in communication circuit applications due to their poor phase noise and linearity performance relative to LC tank oscillators. However, some researchers have investigated the ways to improve the phase noise and linearity of the ring VCOs [21, 22]. The noise

transfer function can be calculated using a linear model for the oscillator. In the paper, these calculations were supported with the measurements in order to predict the thermal noise contributions of the delay elements accurately. A four-stage differential VCO was optimized to achieve the desired tuning and FSK modulation characteristics satisfying the phase noise requirement (-83 dBc/Hz at 160 kHz offset). The schematic of the design including an individual delay element is shown in Figure 11. Every delay cell in this VCO gets three bit calibration control and two bit FSK control signals. These two bit FSK data turn long channel devices M11 and M12 on and off, causing the total sink current change in slight amounts such that frequency deviations will be around 80 kHz. The delay cell topology proposed in [22] is modified to have additional calibration and FSK control. This topology is particularly suitable for the application due to two main reasons. First, one can obtain a very low VCO gain, K_{vco} , by properly sizing the devices M5 and M6 relative to the devices M3 and M4. Second, the tuning devices M5 and M6 would stay in saturation even for very small control voltage levels. Using Barkhausen oscillation criteria, oscillation frequency for an n -stage ring oscillator can be written down as [21, 22]

$$\omega_o = \frac{1}{RC} \tan\left(\frac{\pi}{n}\right), \quad (4)$$

where, R and C are the resistance and capacitance, respectively, at the output node of individual delay cells. For this design the output impedance is dominated by $1/g_{m3,4}$. Since the devices M3 and M4 are mostly in saturation, the relation between the control voltage and the oscillation frequency can be written down as

$$\begin{aligned} \omega_o &= \frac{gm_{3,4}}{C} \\ &= \sqrt{\frac{2\mu n C_{ox} W_{3,4}}{C^2 I_{3,4}}} \sqrt{\left(\frac{I_s}{2} - \frac{\mu n C_{ox} W_{5,6}}{2I_{5,6}} (V_{dd} - V_{ctr})^2\right)}. \end{aligned} \quad (5)$$

Although not perfectly linear, monotonic, and linear-like characteristic can be maintained over the full useful tuning range due to low supply voltage.

The circuit was optimized in simulations to obtain -82 dBc/Hz phase noise at a 160 kHz offset. *Spectre* was used for phase noise optimization. The simulated current consumption of the VCO core including the differential buffers was $700 \mu A$ from a 1.5-V supply.

5.2. Measurement results

The design was laid out on the upper left corner of the 800-MHz LC tank VCO die (Figure 8). The same inductively loaded two-stage PA follows the buffers isolating the delay cells. The measured spectrum and the tuning characteristic of the ring VCO are shown in Figure 12. Very fine distributed overlapping tuning clusters were obtained as predicted. The linearity of this ring VCO even outperforms the linearity of its LC tank counterparts. A very serious drawback of this ring VCO was the excessively high susceptibility of the

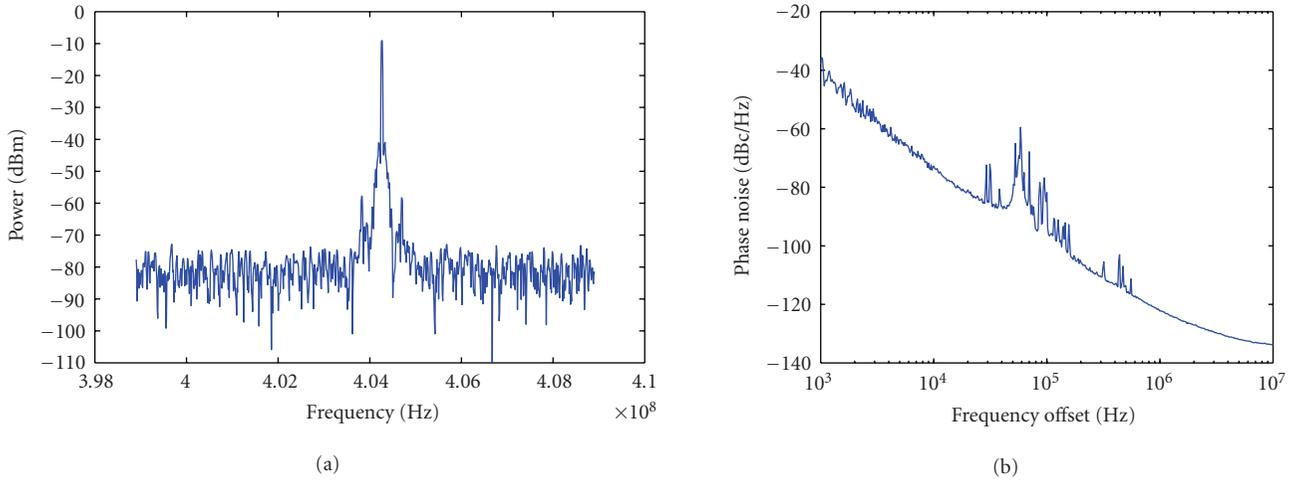


FIGURE 10: (a) The measured spectrum, (b) the phase noise of 800 MHz oscillator followed by a divider.

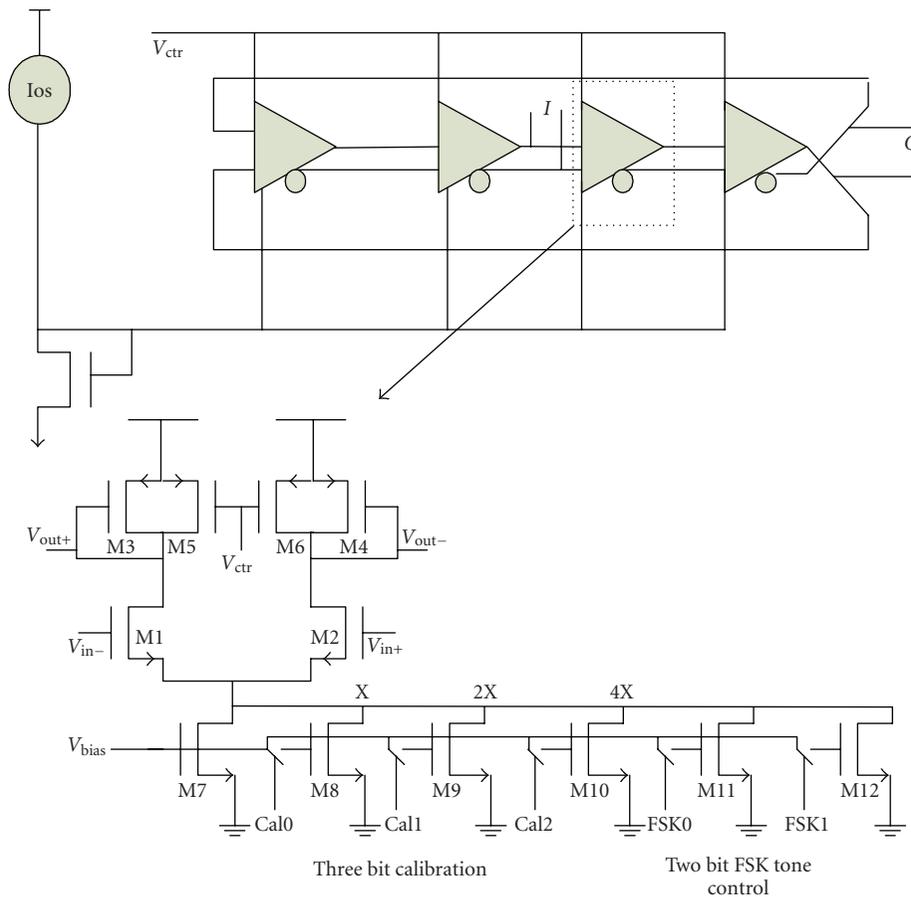


FIGURE 11: The schematic of the four-stage differential ring VCO.

oscillating frequency to the noise in the supply and control lines. Although an average frequency deviation of $\pm \Delta f \cong 120$ kHz observed with FSK control, this drawback associated with this ring VCO should be addressed in order to be able to observe accurate 70 kHz FSK tones.

The phase noise at 160 kHz offset is -77 dBc/Hz, which is extracted by looking at the power from the measured spectrum at this offset and subtracting the resolution bandwidth. The measured current consumption was $738 \mu\text{A}$ from a 1.5-V supply.

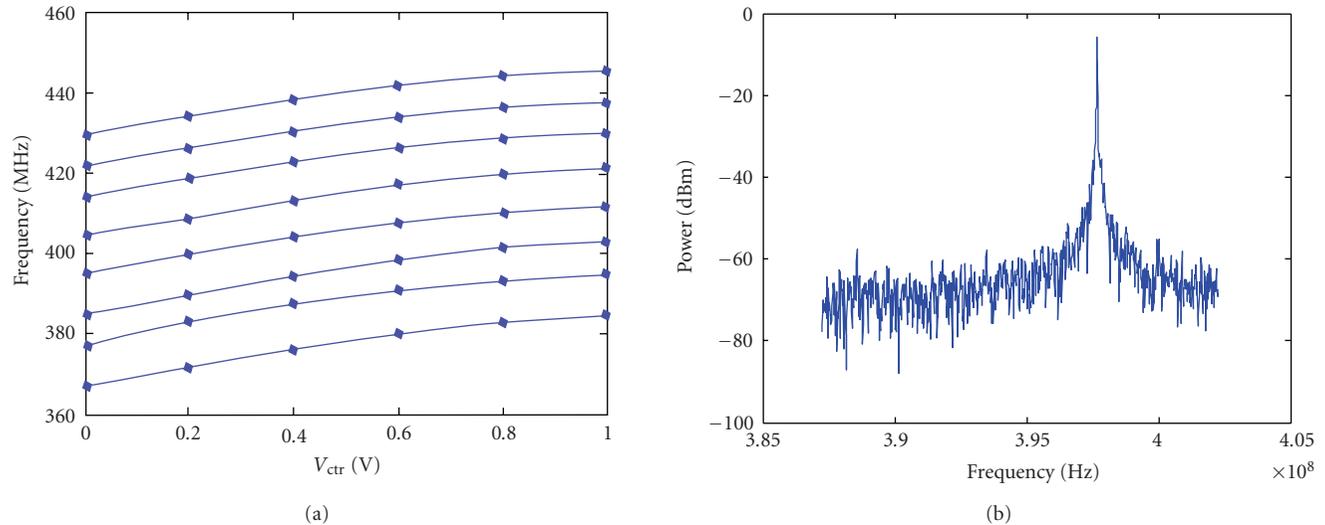


FIGURE 12: (a) The tuning characteristic, (b) the measured spectrum of the four-stage differential ring VCO.

TABLE 1: Comparison table for the three oscillator architectures.

VCO type	Current consumption	Die area	Phase noise @ 160 kHz offset	Linearity	Frequency stability	Supply noise sensitivity
Ring	0.74 mA	0.2 mm × 0.2 mm	-77 dBc/Hz	Good	Poor	Sensitive
LC-tank divided	2.20 mA	0.4 mm × 0.7 mm	-97 dBc/Hz	Moderate	Good	Immune
LC-tank with PF	1.25 mA	0.6 mm × 0.8 mm	-98 dBc/Hz	Moderate	Good	Immune

6. COMPARISON AND CONCLUSION

Three different fully integrated VCOs including the driving buffers and the power amplifiers were designed, and fabricated in 0.18 μm TSMC CMOS process to evaluate the best option for an MICS band transceiver operating at the new 402–405 MHz band. Although it consumes very low power and occupies very small die area, the poor frequency stability of ring VCO makes it difficult to obtain a reasonable FSK tone for 300 kHz channel spacing in MICS band. Moreover, the measured phase noise was 5 dB more than the predefined maximum level. The 800 MHz LC tank VCO with master-slave divider achieves almost the same phase noise performance at the expense of almost double power consumption, compared to the 400 MHz LC tank VCO directly loaded with poly-phase filter. The linearity of the tuning curve of 800 MHz design is worse than the 400 MHz one. The measurement results of these three architectures were summarized in a comparison table (Table 1). In conclusion, a carefully designed 400 MHz LC tank driving a poly-phase filter was proven to be the best option for this application.

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REFERENCES

- [1] FCC Rules and Regulations, "MICS Band Plan," Table of Frequency Allocations, Part 95, January 2003.
- [2] Australian Communications Authority, Radio Frequency Planning Group, "Planning for Medical Implant Communications Systems & Related Devices," Proposals Paper, October 2003, <http://www.acma.gov.au>.
- [3] W. G. Scanlon, J. B. Burns, and N. E. Evans, "Radiowave propagation from a tissue-implanted source at 418 MHz and 916.5 MHz," *IEEE Transactions on Biomedical Engineering*, vol. 47, no. 4, pp. 527–534, 2000.
- [4] A. K. Skrivervik, J.-F. Zurcher, O. Staub, and J. R. Mosig, "PCS antenna design: the challenge of miniaturization," *IEEE Antennas and Propagation Magazine*, vol. 43, no. 4, pp. 12–27, 2001.
- [5] P. Bradley, "An ultra low power, high performance medical implant communication system (MICS) transceiver for implantable devices," in *Proceedings of the IEEE Biomedical Circuits and Systems Conference (BioCAS '06)*, London, UK, November–December, 2006.
- [6] T. Melly, A.-S. Porret, C. C. Enz, and E. A. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: transmitter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 467–472, 2001.
- [7] E. Zencir, T.-H. Huang, A. Tekin, N. S. Dogan, and E. Arvas, "UHF RF front-end circuits in 0.35- μm silicon on insulator

- (SOI) CMOS,” *Analog Integrated Circuits and Signal Processing*, vol. 45, no. 3, pp. 231–245, 2005.
- [8] N. M. Neihart and R. R. Harrison, “Micropower circuits for bidirectional wireless telemetry in neural recording applications,” *IEEE Transactions on Biomedical Engineering*, vol. 52, no. 11, pp. 1950–1959, 2005.
- [9] A.-S. Porret, T. Melly, D. Python, C. C. Enz, and E. A. Vittoz, “An ultralow-power UHF transceiver integrated in a standard digital CMOS process: architecture and receiver,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 452–466, 2001.
- [10] Y. B. Choi, T. H. Teo, and W. G. Yeoh, “A 2.4 GHz fully integrated CMOS VCO with direct FM/FSK modulation capability,” in *Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC '03)*, pp. 175–178, Hong Kong, December 2003.
- [11] A. Tekin, M. R. Yuce, and W. Liu, “A low power MICS band transceiver architecture for implantable devices,” in *Proceedings of the IEEE Annual Conference on Wireless and Microwave Technology (WAMICON '05)*, pp. 55–58, Clearwater, Fla, USA, April 2005.
- [12] J. B. Nolan and R. S. Ellison, “Calibration techniques for a precision relaxation oscillator integrated circuit with temperature compensation,” US patent 299338, March 2002.
- [13] M. H. Splithof, A. J. M. van Tuijl, S. L. J. Gierkink, and E. A. M. Klumperink, “Current-ratio temperature compensation in bipolar relaxation oscillator,” in *Proceedings of the 24th European Solid-State Circuits Conference (ESSCIRC '98)*, pp. 392–395, The Hague, The Netherlands, September 1998.
- [14] B. Razavi, *RF Microelectronics*, Prentice-Hall, Upper Saddle River, NJ, USA, 1998.
- [15] J. Bhattacharjee, D. Mukherjee, E. Gebara, S. Nuttinck, and J. Laskar, “A 5.8 GHz fully integrated low power low phase noise CMOS LC VCO for WLAN applications,” in *Proceedings of the IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 585–588, Seattle, Wash, USA, June 2002.
- [16] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 1998.
- [17] B. Razavi, “A 1.8 GHz CMOS voltage-controlled oscillator,” in *Proceedings of the 43rd IEEE International Solid-State Circuits Conference (ISSCC '97)*, pp. 388–389, San Francisco, Calif, USA, February 1997.
- [18] M. Borremans, M. Steyaert, and T. Yoshitomi, “A 1.5 V, wide band 3 GHz, CMOS quadrature direct up-converter for multi-mode wireless communications,” in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 79–82, Santa Clara, Calif, USA, May 1998.
- [19] M. Borremans, B. De Muer, and M. Steyaert, “The optimization of GHz integrated CMOS quadrature VCO’s based on a poly-phase filter loaded differential oscillator,” in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '00)*, vol. 2, pp. 729–732, Geneva, Switzerland, May 2000.
- [20] J. F. Parker and D. Ray, “A 1.6-GHz CMOS PLL with on-chip loop filter,” *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 337–343, 1998.
- [21] B. Razavi, “A study of phase noise in CMOS oscillators,” *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, 1996.
- [22] H. Chen and R. Geiger, “Transfer characterization of CMOS ring voltage controlled oscillators,” in *Proceedings of the 44th IEEE Midwest Symposium on Circuits and Systems (MWS-CAS '01)*, vol. 1, pp. 66–70, Dayton, Ohio, USA, August 2001.



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