Hindawi Publishing Corporation
International Journal of Plasma Science and Engineering
Volume 2009, Article ID 308949, 10 pages
doi:10.1155/2009/308949

Research Article

Plasma-Induced Damage on the Reliability of Hf-Based High-*k*/Dual Metal-Gates Complementary Metal Oxide Semiconductor Technology

Wu-Te Weng,[1] Yao-Jen Lee,[2] Horng-Chih Lin,[1,2] and Tiao-Yuan Huang[1]

[1] *Institute of Electronics, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan*
[2] *National Nano Device Laboratories, Science-Based Industrial Park, 26 Prosperity Road 1, Hsinchu 30078, Taiwan*

Correspondence should be addressed to Wu-Te Weng, wtweng.ee90g@nctu.edu.tw

Received 15 April 2009; Revised 23 July 2009; Accepted 30 September 2009

Recommended by Paul K. Chu

This study examines the effects of plasma-induced damage (PID) on Hf-based high-*k*/dual metal-gates transistors processed with advanced complementary metal-oxide-semiconductor (CMOS) technology. In addition to the gate dielectric degradations, this study demonstrates that thinning the gate dielectric reduces the impact of damage on transistor reliability including the positive bias temperature instability (PBTI) of n-channel metal-oxide-semiconductor field-effect transistors (NMOSFETs) and the negative bias temperature instability (NBTI) of p-channel MOSFETs. This study shows that high-*k*/metal-gate transistors are more robust against PID than conventional SiO_2/poly-gate transistors with similar physical thickness. Finally this study proposes a model that successfully explains the observed experimental trends in the presence of PID for high-*k*/metal-gate CMOS technology.

Copyright © 2009 Wu-Te Weng et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

1. Introduction

Researchers first reported plasma-induced damage (PID) in 1983 [1] using the plasma steps during the interconnect formation processes. PID is well known to degrade both gate dielectric and metal-oxide-semiconductor field-effect transistors (MOSFETs) reliability [2]. The silicon wafer manufacturing employs many plasma-processing steps, including gate electrode etching [3], high-density plasma chemical vapor deposition (HDP-CVD) [4], metal interconnect etching [5], and photoresist ashing [6]. During plasma processing, charges (i.e., ions or electrons) accumulated from a large interconnect area cause a local imbalance in the surface potential across the gate dielectric and cause current to flow through the gate electrode. The plasma damage current can potentially break the gate dielectric bonds with increasing gate dielectric leakage current or decreasing breakdown voltage. Moreover, the defects or weak points that PID creates in the bulk dielectric and the dielectric/Si-substrate interfaces can further degrade the transistor reliability after reliability stressing.

However, SiO_2 as the gate dielectric is now facing fundamental physical limitations, as film thickness comprises only a few atomic layers [7]. To solve this fundamental barrier, high-*k*/metal-gate transistors can be introduced into advanced complementary metal-oxide-semiconductor (CMOS) technology to replace SiO_2/poly-gate transistors in suppressing the gate leakage current and eliminating poly depletion effect [8]. Therefore, the process of high-*k*/metal-gate fabrication must be compatible with current CMOS technology, and the electrical reliability of high-*k*/metal-gate transistor must be considered for long-term operation [9]. Previous studies on p-channel MOSFETs (PMOSFETs) have shown that positive charges become trapped in the SiO_2/Si-substrate interface under negative gate bias, causing shifts in the threshold voltage (V_{TH}) during prolonged device operation (i.e., negative bias temperature instability (NBTI) effect) [10]. In addition, for n-channel MOSFETs (NMOSFETs), electrons trapped in oxygen vacancies cause a significant shift in V_{TH} under positive gate bias stress (i.e., positive bias temperature instability (PBTI) effect) [11]. Therefore, both NBTI and PBTI become important issues for high-*k*/metal-gate transistors and it is necessary to pay significant attention to the PID-enhanced transistor reliability degradation as CMOS technology continues to scale. Several studies reported PID impacts on

high-k/metal-gate transistors [12, 13], but a comprehensive study on the antenna ratio dependence and gate dielectric thickness dependence in damage-enhanced gate dielectric failure and damage-enhanced transistor reliability degradation is still lacking.

In this study we propose both damage mechanism and degradation models for high-k/metal-gate transistors and compares the damage-enhanced degradations between high-k/metal-gate and conventional SiO_2/poly-gate transistors. In addition to gate dielectric degradation, in this study we investigate the transistor reliability issues, including NMOSFETs' PBTI and PMOSFETs' NBTI by damage-enhanced electron trapping. For the first time, a universal relationship between PID and gate dielectric thickness scaling is unveiled. Further, this study demonstrates the power-law dependence between gate antenna ratio and the transistor's reliability degradations. Researchers can use proposed models to accurately predict gate dielectric failure and transistor lifetime in the presence of PID for advanced high-k/metal-gate CMOS technology.

2. Experimental Procedure

2.1. Wafer Processing. Advanced high-k/metal-gate and conventional SiO_2/poly-gate transistors processed with full layers of CMOS technology were investigated in this study. Many process steps including shallow trench isolation (STI) and the formation of a triple well, shallow junction, and Co salicide were all integrated for high-performance circuit applications. The doping concentration of the substrate was about $5 \times 10^{15}\,\text{cm}^{-3}$ and the concentration of the transistor's well was around $4 \times 10^{17}\,\text{cm}^{-3}$. For the conventional SiO_2/poly-gate transistors, the gate oxide thickness ranged from 1.5 nm to 3.0 nm, while for the Hf-based high-k/metal-gate transistors, the equivalent oxide thickness (EOT) ranged from 1.5 nm to 2.0 nm (i.e., with physical thickness of approximately 3.0–5.0 nm). For high-k/metal-gate transistors, the dielectric consisted of a SiO_2 interfacial layer (IL) and an HfSiO film, which were both treated with NH_3 annealing. A rapid thermal annealing (RTA) at 1000°C for 5 seconds was performed for the source/drain activation. The ratio of Hf/(Hf+Si) of HfSiO film was 50%. After NH_3 annealing, Hf–N bonds increase the crystallization temperature of high-k/metal-gate process, retaining the compatibility to conventional SiO_2/poly-gate process with high-temperature RTA [14, 15]. A chemical oxide with thickness of 0.8 nm was used as the IL layer, and HfSiO layers with different physical thicknesses ranging from 2.0 to 4.0 nm were fabricated in this study. It is worth noting that the IL layer serves as a reaction barrier between high-k and Si-substrate [9]. Dual metal-gate structures (i.e., TaC for NMOSFET's metal-gate and MoNx for PMOSFET's metal-gate) were manufactured to meet high-speed performance requirements. The high-k and metal films were deposited using atomic-layer deposition (ALD) and physical vapor deposition (PVD) techniques, respectively.

2.2. Test Structure Design. Figure 1(a) illustrates that plasma-induced damage can usually be detected using various antenna structures. These antenna structures include a transistor with a large gate antenna attached to its gate electrode, which amplifies the charging damage produced under plasma processing during the gate electrode formation process. Therefore, during metal-gate definition process in etching systems as well as postgate dielectric film deposition in HDP-CVD systems, plasma will attack the gate antenna area and damage the gate dielectric (Figure 1(b)). The gate antenna ratio, AR, is defined as

$$\text{AR} = \frac{\text{Area of gate antenna}}{\text{Area of gate oxide}}. \quad (1)$$

In this study we have fabricated a set of test structures with various AR of 3X (i.e., undamaged transistors), 100X, 500X, 1000X, 5000X, and 10000X (i.e., significantly damaged transistors) to simulate the impact of the PID effects on real circuits during various stages of plasma processing. The gate oxide area of the monitoring transistor used in our experiment was $1\,\mu\text{m}^2$, and the transistor length and width were $0.2\,\mu$m and $5\,\mu$m, respectively.

2.3. Electrical Measurements. In this study we define the gate dielectric failure as a twofold increase in the dielectric leakage current compared to undamaged transistors. The gate dielectric leakage current was measured under an electric field of 7∼9 MV/cm, and the gate dielectric breakdown voltage V_{BD} was measured by the voltage ramp method. In this study we define the failure ratio of gate dielectric leakage current and gate dielectric breakdown as the percentage of failure out of the total measured samples. The measurements of NBTI on PMOSFETs and PBTI on NMOSFETs were performed under an electric field of 10 MV/cm using an HP-4156 system at 125°C. The NBTI lifetime and PBTI lifetime were defined as the time until the transistor exhibited a 50 mV shift in threshold voltage. The EOT was extracted from the capacitance-voltage characteristics using an HP-4284 system at room temperature.

3. Results and Discussion

3.1. Dielectric Degradation

3.1.1. Damage-Enhanced Dielectric Degradation. Dielectric breakdown of high-k/metal-gate transistor is due to the clusters of disconnected bonds. These clusters propagate through the dielectric film and finally reach the high-k/metal-gate interface. It is generally believed that defects existing in the dielectric layers can produce weak spots or trap centers that trap charges. During plasma processing, the damage current flowing through the gate dielectric can be viewed as an equivalent voltage stress, V_{st}, or electric field stress, E_{st}, across the gate dielectric. V_{st} or E_{st} is able to generate lots of defects in high-k/metal gate transistors [16]. Moreover, these PID effects can aggravate the degradations of the dielectric layer owing to the extra damage current paths generated by the V_{st} across the dielectric layers during the plasma processing. To simplify the analysis of damage impacts during the wafer fabrication, the dependence of the damage effect on AR is

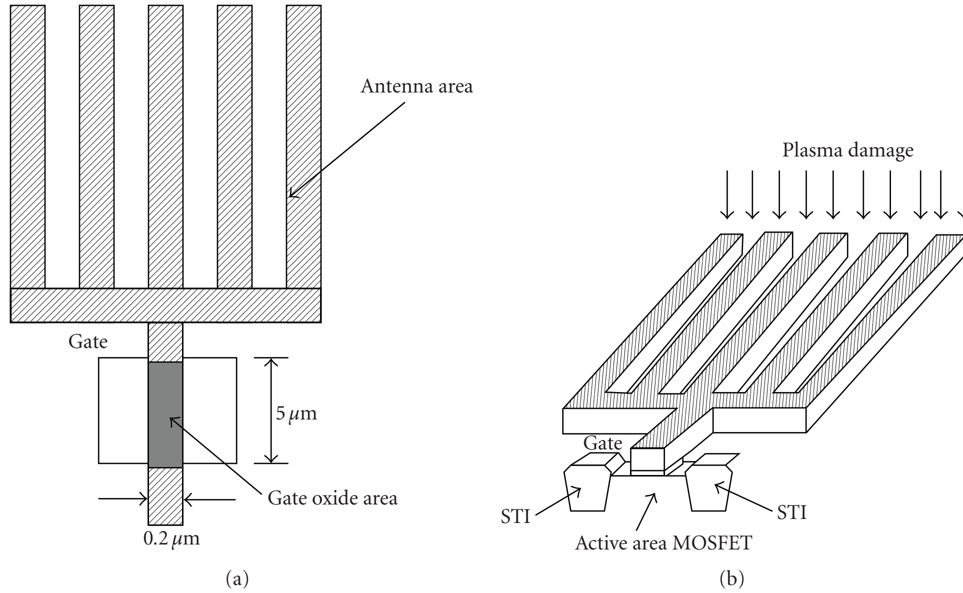

Figure 1: Schematic diagrams of the transistor with its gate being connected to an antenna structure: (a) top view of the test structure, and (b) cross section.

introduced in terms of the plasma damage current I_{plasma} to simulate the damage characterization. By assuming a fixed AR under a given plasma process, the term I_{plasma} can be considered as a constant current source of "damage current" that passes through the high-k/metal-gate electrode. As the AR increases, the total plasma current passing through the gate dielectric increases proportionally to AR. Figure 2 shows the dielectric current-voltage curves of PMOSFETs with different gate dielectric thicknesses and values of AR. I_{plasma} can be expressed as $I_{\text{plasma}} = P \cdot \text{AR}$, where P is the plasma damage current collected when $\text{AR} = 1$ (i.e., an antenna ratio of unity). The P value is assumed to be a constant under a given plasma processing and is expected to exhibit a process dependence due to changes in ion density, electron temperature, and so forth, as the plasma processing changes [17]. During plasma processing, dielectric breakdown occurs at plasma current density of approximately 2–20 A/cm^2[18]. Thus, the experiments in this study assume that the P value is approximately 2×10^{-10} A with 1 μm^2 transistors size (i.e., for the damaged structures with antenna ratio AR = 100X, $I_{\text{plasma}} = 2\,\text{A/cm}^2$, and for structure with AR = 1000X, $I_{\text{plasma}} = 20\,\text{A/cm}^2$). Figure 2 depicts the dielectric current-voltage curves of PMOSFETs with different gate dielectric thicknesses for both high-k/metal-gates and SiO_2/poly-gates. This figure also indicates the plasma damage current simulated for various AR. Comparing the plasma current-voltage with dielectric current-voltage characteristics, I_{plasma} corresponds to a voltage stress, V_{st}, on the gate electrode during plasma processing. Aggravated dielectric degradation from PID results in an increase in the effective stress voltage V_{st} across the gate dielectric during plasma processing. Clearly, V_{st} not only depends on AR but is also influenced by EOT. Figure 3 shows that the E_{st}, defined as V_{st}/EOT, is a function of AR. A larger AR results in a larger E_{st}

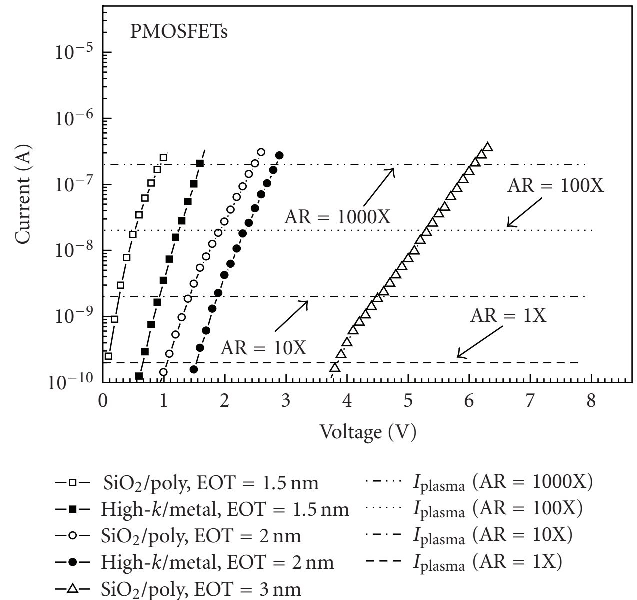

Figure 2: Characteristics of gate dielectric current and simulated plasma damage current with respect to voltage. The gate dielectric current curves are measured at various gate oxide thicknesses ranging from 1.5 nm to 3.0 nm for SiO_2/poly-gate PMOSFETs and EOT ranging from 1.5 nm to 2.0 nm for high-k/metal-gate PMOSFETs. This study simulates the plasma damage current for gate antenna ratios AR of 1X, 10X, 100X, and 1000X.

and therefore much more severe degradation in dielectric reliability for EOT ranging from 1.5 nm to 3.0 nm for both SiO_2/poly-gate and high-k/metal-gate transistors.

Moreover, E_{st} strongly depends on EOT. For example, for SiO_2/poly-gate transistors with a gate oxide thickness

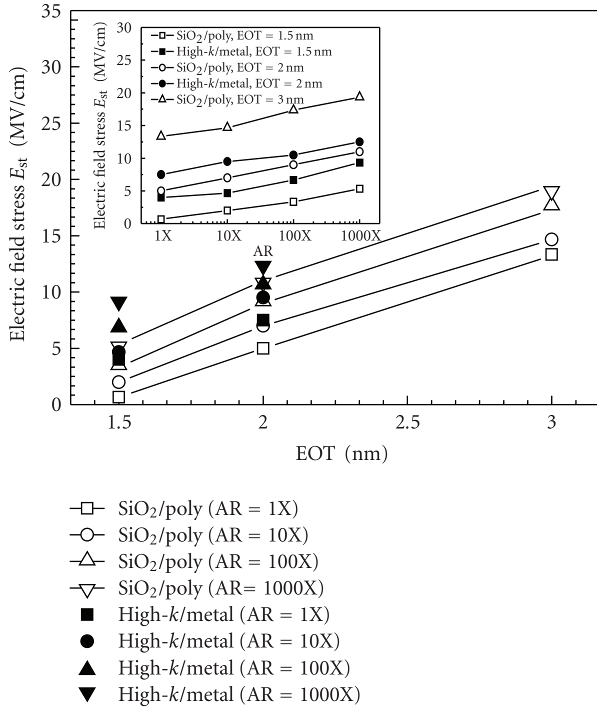

Figure 3: Estimated electric field stress (E_{st}) during plasma processing as a function of EOT for different AR. The inset shows the E_{st} as a function of AR for different EOTs.

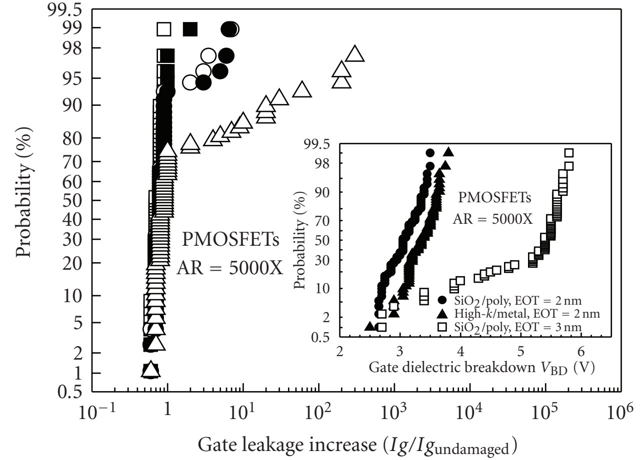

Figure 4: Failure probability of gate dielectric leakage measured on PMOSFETs with EOTs ranging from 1.5 nm to 3.0 nm for SiO_2/poly-gate transistors and EOTs ranging from 1.5 nm to 2.0 nm for high-k/metal-gate PMOSFETs. The inset is the failure probability of V_{BD} measured for the above transistors with EOTs greater than 2.0 nm. The AR attached to these transistors is 5000X.

of 3.0 nm, the tunneling mechanism of plasma current passing through the dielectric can be dominated by Fowler-Nordheim (FN) tunneling, and E_{st} exhibits a greater antenna dependence during plasma process. In contrast, when the EOT is reduced to 1.5~2.0 nm for both high-k/metal-gate and SiO_2/poly-gate transistors, the tunneling mechanism shifts from Fowler-Nordheim tunneling to direct tunneling. This in turn produces a lower antenna dependence of E_{st} compared to SiO_2/poly-gate transistors with a gate oxide thickness of 3.0 nm.

3.1.2. Results for Damage-Enhanced Dielectric Degradation. Figure 4 demonstrates the failure ratios in terms of gate dielectric leakage current and breakdown voltage for a given AR of 5000X for both SiO_2/poly-gate and high-k/metal-gate PMOSFETs with various EOTs. It is evident that SiO_2/poly-gate transistors with a gate oxide thickness of 3.0 nm show significant gate oxide leakage distribution and a higher V_{BD} failure ratio as the plasma current I_{plasma} increases. Specifically, the failure ratios of gate dielectric leakage and V_{BD} for SiO_2/poly-gate MOSFETs with a gate oxide thickness of 3.0 nm increase by 26%. In contrast, for SiO_2/poly-gate and high-k/metal-gate transistors with an EOT of approximately 1.5–2.0 nm, the oxide tunneling mechanism is dominated by direct tunneling. This in turn produces a smaller stress voltage V_{st}, on the gate electrode stacks during plasma process. Figure 4 shows that the failure ratio of gate dielectric leakage and V_{BD} degradation can be reduced to less than 6% by decreasing the EOT to below 2.0 nm. In addition, Figure 5 demonstrates the dependence between failure ratios of gate leakage current and transistors' EOTs ranging from 1.5 nm to 3.0 nm with different ARs of 100X, 500X, and 5000X. By reducing the EOT from 3.0 nm to 1.5 nm, the dielectric failure ratio of the antenna transistors connected to AR = 500X can be decreased from 12% to nil, and the failure ratio of the transistors connected to AR = 5000X can be further reduced to from 26% to 2%, as Figure 5 indicates. These results confirm that the E_{st} is linearly dependent on EOT and can be decreased by reducing EOT from 3.0 nm to 1.5 nm as well as changing the test structure from SiO_2/poly-gate to high-k/metal-gate transistors. In addition, the EOT dependence of damage-enhanced gate dielectric degradation is irrespective of the AR. The results of Figures 4 and 5 are consistent with the damage models proposed in this study and shown in Figures 2 and 3. Clearly, a transistor with an EOT of approximately 3.0 nm shows a strong AR dependence of E_{st}. Further, PID impact on gate dielectric degradation of high-k/metal-gate transistor is determined by EOT, rather than physical thickness. This study confirms that the strong dependence of dielectric EOT causes significant damage to the input/output transistors with a thicker EOT of approximately 3.0 nm both for high-k/metal-gate and SiO_2/poly-gate transistors. Therefore, high-k/metal-gate transistors with a thinner EOT would be robust for PID, because damage-induced dielectric degradation is not a serious issue for the thinner gate dielectric high-k/metal-gate transistors needed to support the operation voltage in the core circuit design.

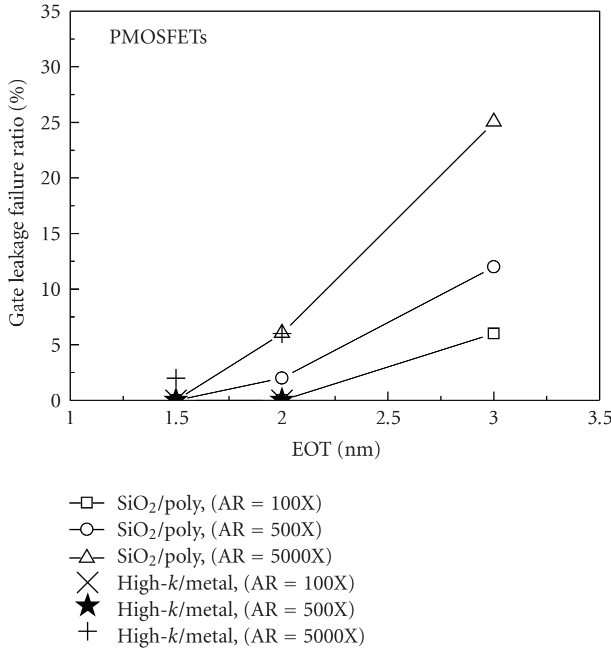

Figure 5: Failure percentages of gate leakage current as a function of EOT for both high-k/metal-gate and conventional SiO_2/poly-gate PMOSFETs with EOTs ranging from 1.5 nm to 3.0 nm with ARs of 100X, 500X, and 5000X.

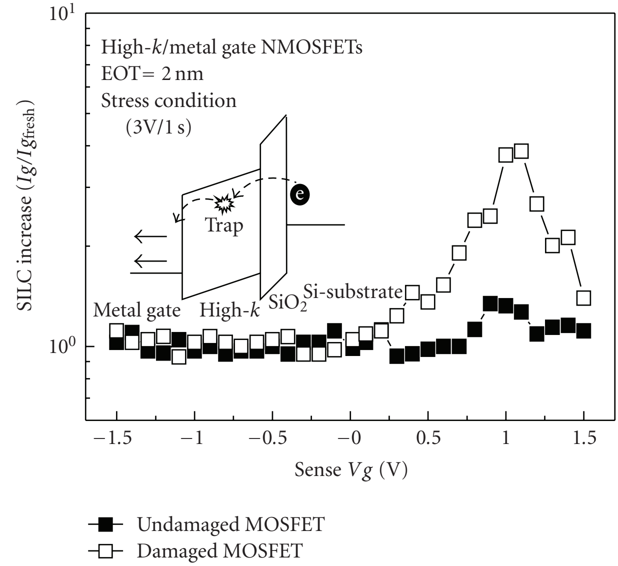

Figure 6: The increase of SILC as a function of gate voltage sensed from −1.5 V to 1.5 V for a damaged and an undamaged high-k/metal-gate NMOSFET. The inset illustrates trap-assisted electron tunneling through high-k film for a damaged high-k/metal-gate NMOSFET.

3.2. Damage-Enhanced Threshold Voltage Instability for High-k/Metal-Gate MOSFETs

3.2.1. Damage-Enhanced PBTI Degradations for High-k/Metal-Gate NMOSFETs. The results in Figure 4 show that plasma-induced damage is usually evaluated by monitoring the gate dielectric leakage current [19] or breakdown voltage [20] with a given antenna ratio attached to the gate electrode. The occurrence of additional gate oxide leakage implies the existence of additional current paths within the gate dielectric layers. However, prior to the formation of a conductive path within the dielectric layers, sufficient damage (i.e., defects and traps) would have been accumulated to degrade transistor reliability [21]. In other words, the degradation of transistor reliability occurs before the gate leakage increases. Because the difference in PID-induced gate leakage current between damaged and undamaged transistors is small compared with the gate tunneling current, the conventional methods (i.e., monitor the increase of gate leakage current with applying high electric filed) may fail to detect PID, especially for transistors fabricated with a thinner EOT. Previous study shows that providing a constant voltage stress (CVS) on the gate electrode after wafer processing and the traps created during plasma process can be revealed in the dielectric layers [22]. These traps can act as sites for assisting the electron tunneling from substrate to gate electrode (i.e., trap-assisted tunneling effect) resulting in an increase in the gate dielectric leakage, as shown in Figure 6. Moreover, the energy level of the traps can be calculated from the curve of stress-induced gate leakage current (i.e., SILC) by monitoring how the peak of the increase of SILC responds to the gate voltage [23]. This result indicates that the PID preferentially degrades the high-k film or the interfacial layer. Figure 6 shows that damaged high-k/metal gate transistor exhibits an obvious and significant increase of SILC with a peak at around $Vg = 0.9 \sim 1.0$ V. The results are consistent with high-voltage stress on transistor's well causing substrate hot electron injection and generating defects in high-k film [23, 24]. Furthermore, based on previous studies [25, 26], it has been proposed that the charge state of oxygen vacancies could describe the energy signature of these traps and is responsible for the increase in SILC.

This study assumes that the PID effects in the gate dielectric of high-k/metal-gate transistors are similar to those caused by gate voltage stress, V_{st}. Moreover, during the plasma process, the damage current flux I_{plasma} breaks the weak Hf-based dielectric bonds, generating oxygen-vacancy-related defects (Od) in the high-k film. Note that the oxygen-vacancy-related defect bonds are located below the conduction band of the Hf-based dielectric, and oxygen vacancies, Vo^{++}, are produced from the following reaction: $Od \rightarrow Vo^{++} + 2e^- + 1/2O_2$ [27, 28]. The oxygen-vacancy-related defects might not be evident after the plasma processing because the postmetallization annealing process passivates them [29]. However, further electrical stress, such as PBTI and NBTI, reveals their existence.

Under plasma charging, a large E_{st} stress on high-k film creates many oxygen-vacancy-related defects and oxygen vacancies within the high-k film. Applying PBTI stress to high-k/metal-gate NMOSFETs causes electrons in the inversion layer to gain sufficient energy to be injected into the dielectric layers. As a result, electrons are easily trapped in the oxygen vacancies within the high-k film [11, 21].

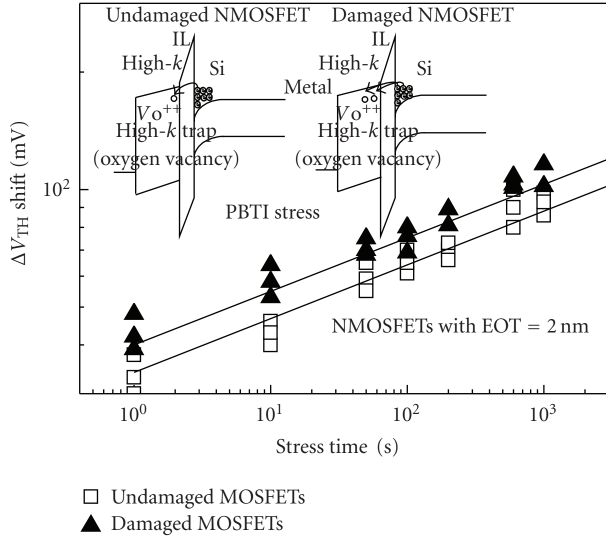

Figure 7: PBTI-induced ΔV_{TH} shift as a function of stress time for damaged and undamaged high-k/metal-gate NMOSFETs. The inset illustrates the mechanism difference between damaged and undamaged transistors during PBTI stress.

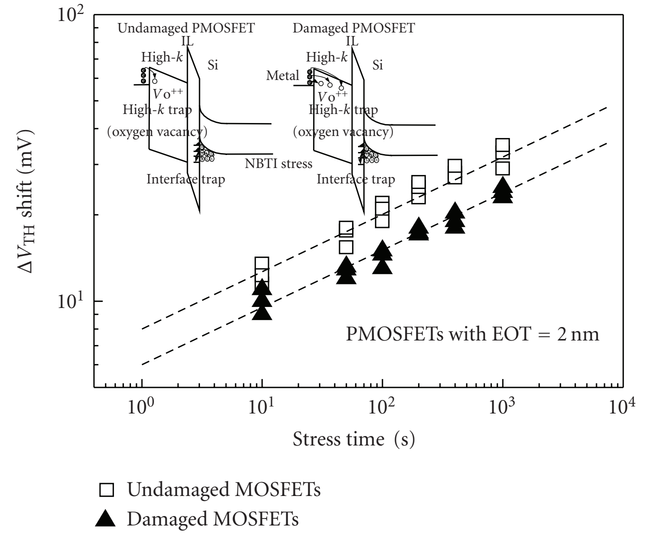

Figure 8: NBTI-induced ΔV_{TH} shift as a function of stress time for damaged and undamaged high-k/metal-gate PMOSFETs. The inset illustrates the difference between damaged and undamaged transistors during NBTI stress.

Figure 7 shows that all NMOSFETs (both damaged and undamaged transistors) exhibit PBTI degradations: however, the damaged transistors are likely to have a higher number of oxygen vacancies as evidenced by the larger ΔV_{TH} shift in the time dependence of threshold voltage instability. Figure 7 depicts the PBTI dependence of high-k/metal-gate NMOSFETs with an EOT of 2.0 nm for a damaged transistor with an AR of 10000X and an undamaged transistor with an AR of 3X. This figure shows that the damaged transistors exhibit larger ΔV_{TH} shift than the undamaged transistors as the stress time progresses. Specifically, after 1000 seconds of PBTI stress, the ΔV_{TH} shift is only around 85 mV for the undamaged transistors, but nearly 100 mV for the damaged transistors. This is because the damage induces an increase in oxygen-vacancy-related defects, then electrons are captured in oxygen vacancies during PBTI stress. The increased degradation exhibited by damaged transistors shown in this study is consistent with the PBTI physical models demonstrated in previous literatures [11, 25, 26].

3.2.2. Damage-Enhanced NBTI Degradations for High-k/ Metal-Gate PMOSFETs. For high-k/metal-gate PMOSFETs experiencing NBTI stress, holes in the inversion layer gain sufficient energy to dissociate the weak Si–H bonds. This in turn generates interface states with holes (positive charges) trapping at the SiO_2/Si-substrate interface [10]. Figure 8 shows that many oxygen-related defects and oxygen vacancies exist in the high-k film, and electrons injected from the metal-gate are captured by oxygen vacancies Vo^{++}. Furthermore, the damaged transistors show less degradation because these transistors have higher concentrations of electron trapping (i.e., negative charges) in the high-k film, which mitigates the ΔV_{TH} shift of hole trapping (i.e., positive charge) during NBTI stress. Figure 8 depicts the ΔV_{TH} shift as a function of NBTI stress time for damaged and undamaged high-k/metal-gate PMOSFETs with an EOT of 2.0 nm. This figure shows that the damaged transistors exhibit less threshold voltage shift ΔV_{TH} than the undamaged transistors as the stress time progresses. Specifically, after 1000 seconds of NBTI stress, the ΔV_{TH} shift is about 30 mV for the undamaged transistors, but only 25 mV for the damaged transistors.

To verify the NBTI models proposed in this study, current separation measurements were carried out after NBTI stress ($Vg = -2$ V, 1000 seconds). Figure 9 shows that after NBTI stress, the injected holes are monitored by the drain (source) current, while electrons are monitored by the substrate current. Further, to investigate the electron capturing effect, this study examined both high-k/metal-gate transistors and SiO_2/Poly-gate PMOSFETs with an EOT of 2.0 nm. Figure 9 shows the ratio of electron current (Ie) over the total current (i.e., hole current (Ih) + electron (Ie)) as a function of the sweeping gate voltage. This figure shows that the damaged high-k/metal-gate transistor depicts the greatest ratio of Ie/(Ie + Ih) in all experiments. This suggests that, unlike the conventional SiO_2/poly-gate PMOSFETs, the damage-induced electron trapping in the high-k film plays an important role in the NBTI characteristics of high-k/metal-gate PMOSFETs, as Figure 8 indicates. This is consistent with the damage model proposed in this study. In summary, the results of Figures 6–9 show that the transient nature of the damage-enhanced electron trapping in high-k film affects the NMOFETs' PBTI and PMOSFETs' NBTI performance in advanced high-k/metal-gate CMOS technology.

3.3. The Model of Damage-Enhanced Instability for High-k/Metal-Gate MOSFETs Reliability. Figure 10 compares the plasma damage with gate dielectric current-voltage

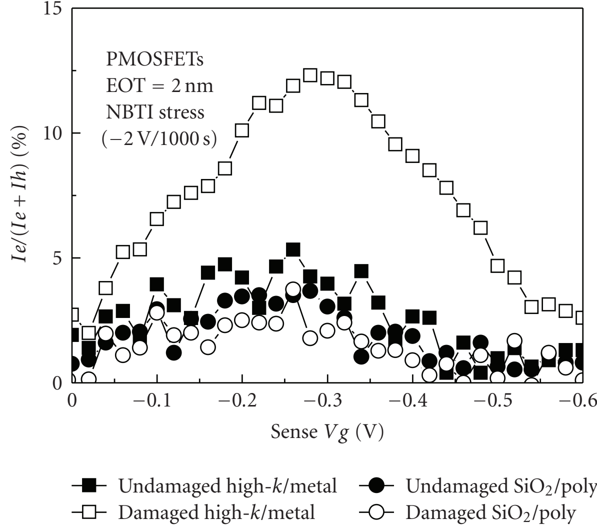

Figure 9: The ratios of Ie/(Ie + Ih) as a function of sweeping gate voltage for damaged and undamaged PMOSFETs fabricated with high-k/metal-gate and conventional SiO_2/poly-gate after NBTI stress (i.e., $Vg = -2$ V, and 1000 seconds). The inset illustrates the current separation method to identify the injection carriers within the gate dielectric.

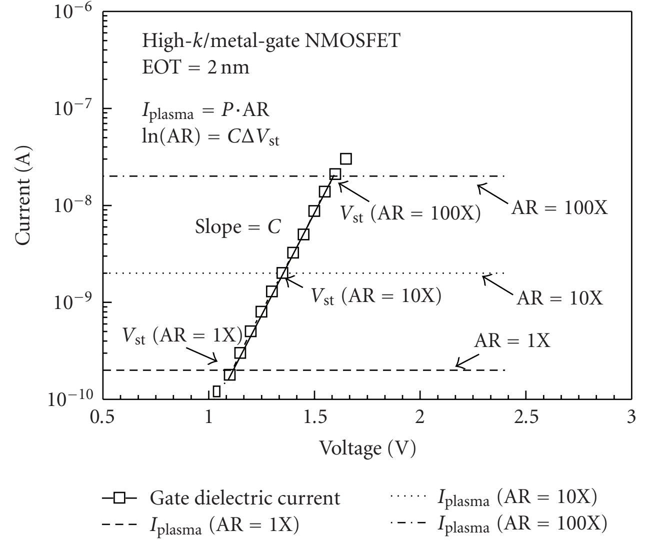

Figure 10: The characteristics of measured dielectric current and simulated damage current as a function of voltage for various AR for high-k/metal-gate NMOSFETs with an EOT of 2.0 nm.

characteristics for a high-k/metal NMOSFET with EOT = 2.0 nm, showing that I_{plasma} corresponds to a voltage stress, V_{st}, on the transistor gate dielectric during processing. Instability of PBTI and NBTI resulting from PID therefore represents an increase in the effective stress voltage ΔV_{st} across the gate dielectric during plasma processing. Furthermore, the relationship between AR and ΔV_{st} can be expressed as

$$\ln(\text{AR}) = \text{C}\Delta V_{\text{st}}, \tag{2}$$

where C is the slope of the gate dielectric current-voltage characteristics in Figure 10 and is strongly dependent on the EOT, as Figure 2 indicates. During the plasma processing, defects or traps are generated when the damage-induced V_{st} or E_{st} breaks the dipoles within the dielectric [30, 31]. Several previous studies have shown that the increase of defects or traps could be a function of voltage stress [32], and these studies depict an exponential relationship between trap generation and electric field stress across the gate dielectric [33, 34]. Thus, during the plasma process, an increase in the density of oxygen-vacancy-related traps within the high-k dielectric, ΔN_{OV}, from the gate stress can be written as an increase of voltage stress ΔV_{st} as

$$\Delta N_{\text{OV}} = A\exp\left(\gamma_{\text{p}}\Delta E_{\text{st}}\right) = A\exp\left(\frac{\gamma_p \Delta V_{\text{st}}}{\text{EOT}}\right), \tag{3}$$

where A is a constant and γ_p is the electric field acceleration factor. Both of these terms are dependent on the plasma process and γ_p is approximately 0.1∼0.2 (Dec-cm/MV) for plasma processing [35].

During PBTI or NBTI stress, the model proposed in this study shows that the injected electrons which are trapped in oxygen vacancies cause an increase in the negative charge and instability in the transistor threshold voltage. All transistors, irrespective of their antenna ratio, exhibit ΔV_{TH} shift under PBTI or NBTI stress. However, transistors with larger AR have higher concentrations of negative charge trapped within the high-k layer. For a constant EOT, the ΔV_{TH} instability resulting from the increase of negative charge trapped for antenna transistor can be modeled as

$$\Delta V_{\text{TH}} = Ht^n \text{AR}^{\alpha}, \tag{4}$$

where t is the duration of the NBTI or PBTI stress, n is approximately 0.16 for both NBTI and PBTI [36], and H is a constant. The parameter α can be expressed as

$$\alpha = \frac{\gamma_p}{\text{EOT} \cdot C}. \tag{5}$$

Note that α for PBTI stress is positive (i.e., ΔV_{TH} increases with AR), while α for NBTI stress is negative (i.e., ΔV_{TH} decreases with AR). The failure time t_f, defined as the time required to reach the critical threshold voltage increase ΔV_{thc}, is

$$t_f = G\Delta Vc\text{AR}^{-m}, \tag{6}$$

where G is a constant for a given process, $\Delta V_C = (\Delta V_{\text{thc}})^{1/n}$, and $m = \alpha/n$.

3.4. The Effects of EOT on the Damage-Enhanced Instability for High-k/Metal-Gate MOSFETs Reliability. Figures 11 and 12 plot the PBTI lifetime and NBTI lifetimes, respectively, as a function of antenna ratio for high-k/metal-gate transistors with an EOT of 2.0 nm. These figures indicate that the antenna dependence m follows the power-law relationship, consistent with (6). Figure 11 shows the antenna dependence

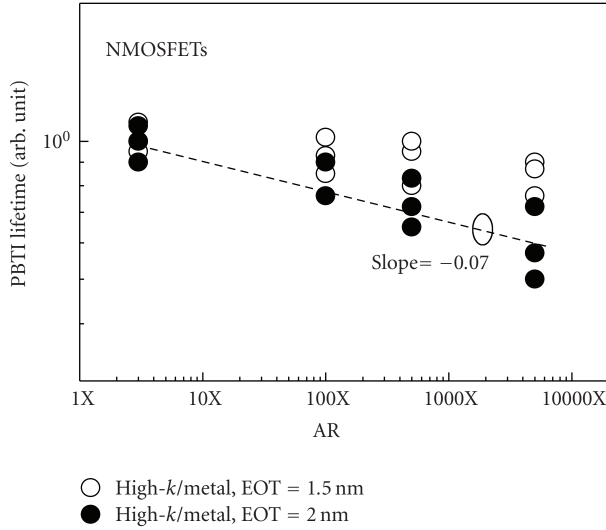

Figure 11: PBTI lifetimes as a function of AR for high-k/metal-gate NMOSFETs with EOTs of 2.0 nm and 1.5 nm, respectively.

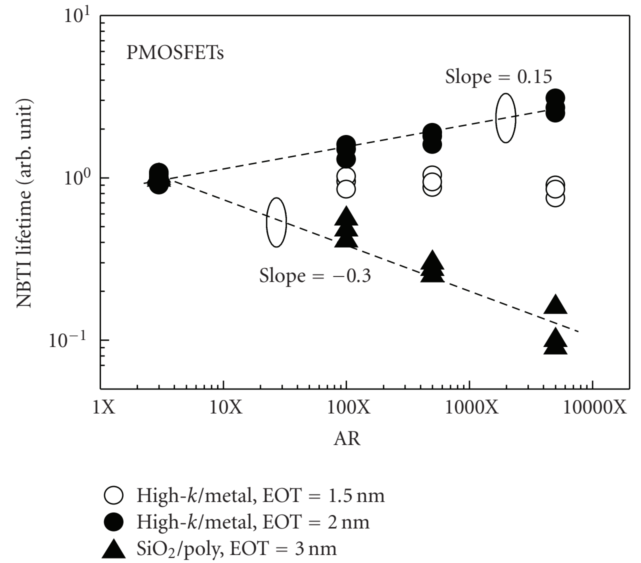

Figure 12: NBTI lifetime as a function of AR for high-k/meta-gate PMOSFETs with EOTs of 2.0 nm and 1.5 nm, and conventional SiO_2/poly-gate PMOSFETs with an EOT of 3.0 nm, respectively.

m is 0.07 for NMOSFETs' PBTI lifetime. However, Figure 12 indicates a larger m of 0.15 for PMOSFETs' NBTI lifetime. The difference in the antenna dependence is caused by the difference of dielectric current-voltage characteristics. For a plasma process with a given I_{plasma}, PMOSFETs experience a higher stress-voltage that leads to a higher oxygen vacancy generation rate than NMOSFETs. In addition, Figure 12 demonstrates a "reverse antenna effect" (i.e., the NBTI lifetime increases with AR) for high-k/metal-gate PMOSFETs. This effect is caused by damage-enhanced electron trapping within the high-k bulk film. This trend is contrary to previously observed results in thicker SiO_2/poly-gate transistors, where damage-enhanced hole trapping within SiO_2 film is dominant [37]. Furthermore, based on the power-law relationship demonstrated in this study, the reliability data obtained from existing antenna test structures can be extrapolated to the transistors with any antenna ratios used in the circuitry.

Figure 10 also shows that C can be determined by the oxide conduction mechanism, and the antenna dependence m in (6) can be significantly reduced with larger C for transistors with a thinner EOT. Figures 2 and 3 show that a smaller V_{st} and E_{st} dependence suggests that the plasma damage effects are mitigated for high-k/metal-gate transistors. As a result, Figures 11 and 12 show that high-k/metal-gate transistors exhibit smaller antenna ratio dependence than SiO_2/poly-gate PMOSFETs with a similar physical dielectric thickness of approximately 3.0 nm. For example, SiO_2/poly-gate PMOSFETs with an EOT of 3.0 nm exhibit the greatest plasma damage and the largest value of m (i.e., 0.3) among all samples. Furthermore, as the EOT of the high-k/metal-gate transistor decreases from 2.0 nm to 1.5 nm, Figures 2 and 3 show that the stress voltage can be reduced to the operation voltage or below. Thus, the stress electric field E_{st} becomes insignificant, which in turn produces a lower failure ratio of gate leakage and dielectric breakdown, as Figures 4 and 5 indicate. Moreover, for damage-enhanced transistor reliability degradation, the increasing C value eliminates the oxygen-related defects introduced within the high-k film. This suppresses the antenna dependence in reliability. Figures 11 and 12 show that large C reduces the antenna dependence of PBTI lifetime and NBTI lifetime until it becomes almost negligible. The models proposed in this study are consistent with experimental results and further confirm that damage-enhanced transistor reliability degradation is alleviated for advanced high-k/metal gate CMOS technology that employs ultra thin high-k film with an EOT smaller than 1.5 nm.

4. Conclusions

For both SiO_2/poly-gate and high-k/metal-gate transistors, plasma-induced charging damage creates many defects and weakened interface bonds that can be easily damaged during reliability testing. Importantly, for high-k/metal-gate transistors, the damage current breaks the bonds of Hf-based dielectric and produces more oxygen vacancies to enhance the instability of NBTI and PBTI. This study develops a comprehensive model of the impact of plasma damage and shows that the dielectric degradation and transistor instability are strongly dependent on the EOT and antenna ratio. Reducing the EOT suppresses the gate dielectric degradation, and the damage becomes minor when the EOT is smaller than 2.0 nm. In addition, the damage becomes negligible when the EOT is smaller than 1.5 nm. This study also discusses the power-law relationship between antenna ratio and transistor PBTI lifetime and NBTI lifetime. Furthermore, NBTI degradations for PMOSFETs can be mitigated with damaged-enhanced electron trapping in oxygen vacancy during NBTI stress, showing a "reverse

antenna effect." In summary, this study demonstrates that plasma-induced damage can be alleviated for advanced high-*k*/metal gate CMOS transistors fabricated with thin dielectric thickness.

References

[1] Y. Yoshida and T. Watanabe, "Gate breakdown phenomena during reactive ion etching process," in *Proceedings of the 5th Dry Process Symposium (DPS '83)*, pp. 4–7, 1983.

[2] S. Krishnan, A. Amerasekera, S. Rangan, and S. Aur, "Antenna device reliability for ULSI processing," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '98)*, pp. 601–604, San Francisco, Calif, USA, December 1998.

[3] B.-W. Chan, Y. H. Liou, and M.-H. Chi, "Elimination of notch during gate polycide stack etching by adding nitrogen in over etch step," *Proceedings of the 5th International Symposium on Plasma Process-Induced Damage*, pp. 54–56, May 2000.

[4] K. M. Byun, D. H. Kim, Y. W. Cha, et al., "Reduction of plasma-induced damage during inter metal dielectric deposition in high-density plasma," in *Proceedings of Intergrated Circuit Desing & Technology Conference (ICICDT '05)*, pp. 99–102, Seoul, Korea, May 2005.

[5] J. Ackaert, B. D. Eddy, C. Peter, and C. Martin, "Prevention of plasma induced damage on thin gate oxide of HDP oxide deposition, metal etch, ar preclean processing in BEOL sub-half micron CMOS processing," in *Proceedings of the 5th International Symposium on Plasma Process-Induced Damage*, pp. 77–80, May 2000.

[6] S. Q. Gu, R. Fujimoto, and M. Peter, "Impact of F species on plasma charge damage in a RF asher," in *Proceedings of the 7th Plasma and Process Induced Damage Symposium*, pp. 88–91, Maui, Hawaii, USA, August 2002.

[7] M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, "Ultra thin (< 4 nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: understanding the processing, structure, and physical and electrical limits," *Journal of Applied Physics*, vol. 90, pp. 2057–2121, 2001.

[8] H. Iwai, S. Ohmi, S. Akama, et al., "Advanced gate dielectric materials for sub-100 nm CMOS," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '02)*, pp. 625–628, December 2002.

[9] G. D. Willk, R. M. Wallace, and J. M. Anthony, "High-*k* gate dielectrics: current status and materials properties considerations," *Journal of Applied Physics*, vol. 89, pp. 5243–5275, 2001.

[10] S. Zafar, B. H. Lee, J. Stathis, A. Callegari, and T. Ning, "A model for negative bias temperature instability (NBTI) in oxide and high k pFETs," in *Proceedings of the Symposium on VLSI Technology, Digest*, pp. 208–209, San Francisco, Calif, USA, 2004.

[11] E. Cartier, B. P. Linder, V. Naryanan, and V. K. Paruchuri, "Fundamental understanding and optimization of PBTI in nFETs with SiO_2/HfO_2 gate stack," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '06)*, pp. 321–324, June 2006.

[12] S. C. Song, S. H. Bae, and Z. Zhang, "Impact of plasma induced damage on pMOSFETs with TIN/HF-silicate stack," in *Proceedings of 43th IEEE International Reliability Physics Symposium (IRPS '05)*, pp. 398–402, San Jose, Calif, USA, April 2005.

[13] C. D. Young, G. Berauker, F. Zhu, et al., "Comparison of plasma-induced damage in SiO_2/TIN and HfO_2/TIN gate stacks," in *Proceedings of 45th International Reliability Physics Symposium (IRPS '07)*, pp. 67–70, April 2007.

[14] M. Koyama, A. Kaneko, T. Ino, et al., "Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '02)*, pp. 849–852, San Francisco, Calif, USA, December 2002.

[15] M. Koike, T. Ino, and Y. Kamimuta, "Effect of Hf-N bond on properties of thermally stable amorphous HfSiON and applicability of this material to sub -50 nm technology node LSIs," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '03)*, pp. 107–110, Washington, DC, USA, December 2003.

[16] M. B. Zahid, R. Degraeve, L. Pantisano, J. F. Zhang, and G. Groeseneken, "Defects generation in SiO_2/HfO_2 studied with variable $T_{CHARGE} - T_{DISCHARGE}$ charge pumping (VT^2CP)," in *Proceedings of 45th International Reliability Physics Symposium (IRPS '07)*, pp. 55–60, April 2007.

[17] A. T. Krishnan, S. Krishnan, and P. Nicollian, "Impact of gate area on plasma charging damage: the "reverse" antenna effect," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '02)*, pp. 525–528, December 2002.

[18] K. P. Cheung, C. T. Liu, C. P. Chang, et al., "Charging damage in thin-gate-oxides better or worse?" in *Proceedings of the 3rd Plasma and Process Induced Damage Symposium*, pp. 34–37, Honolulu, Hawaii, USA, June 1998.

[19] K. P. Cheung, "Advanced plasma and advanced gate dielectric—a charging damage prospective," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 1, pp. 112–118, 2007.

[20] G. Cellere, M. G. Valentini, and A. Paccagnella, "Correlation between soft breakdown and plasma process induced damage," in *Proceedings of the 6th Plasma and Process Induced Damage Symposium*, pp. 40–43, Monterey, Calif, USA, May 2001.

[21] G. Bersuker, J. H. Sim, C. S. Park, et al., "Mechanism of electron trapping and characteristics of traps in HfO_2 gate stacks," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 1, pp. 138–145, 2007.

[22] G. Van den bosch, B. D. Jaeger, and G. Groeseneken, "Evaluation procedure for fast and realistic assessment of plasma charging damage in thin oxides," in *Proceedings of the 7th Plasma and Process Induced Damage Symposium*, pp. 37–40, Maui, Hawaii, USA, August 2002.

[23] R. O'Connor, L. Pantisano, R. Degraeve, et al., "SILC defect generation spectroscopy in HfSiON using constant voltage stress and substrate hot electron injection," in *Proceedings of the 46th IEEE International Reliability Physics Symposium (IRPS '08)*, pp. 324–329, Phoenix, Ariz, USA, April 2008.

[24] M. Toledano-Luque, L. Pantisano, R. Degraeve, et al., "Charge pumping spectroscopy: HfSiON defect study after substrate hot electron injection," *Microelectronic Engineering*, vol. 84, no. 9-10, pp. 1943–1946, 2007.

[25] J. L. Gavartin, D. M. Ramo, A. L. Shluger, G. Bersuker, and B. H. Lee, "Negative oxygen vacancies in HfO_2 as charge traps in high-*k* stacks," *Applied Physics Letters*, vol. 89, no. 8, Article ID 082908, 3 pages, 2006.

[26] K. Torii, K. Shiraishi, S. Miyazaki, et al., "Physical model of BTI, TDDB and SILC in HfO_2-based high-*k* gate dielectrics," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '04)*, pp. 129–132, San Francisco, Calif, USA, December 2004.

[27] E. Cartier, F. R. McFeely, V. Narayanan, et al., "Role of oxygen vacancies in V_{FB}/V_t stability of pFET metals on HfO_2," in

Proceedings of the Symposium on VLSI Technology, pp. 230–231, April 2005.

[28] K. Shiraishi, K. Yamada, K. Torii, et al., "Oxygen vacancy induced substantial threshold voltage shifts in the Hf-based high-*k* MISFET with p^+poly-Si gates—a theoretical approach," *Japanese Journal of Applied Physics*, vol. 43, pp. 1413–1415, 2004.

[29] P. Riess, R. Kies, G. Ghibaudo, G. Pananakakis, and J. Brini, "Reversibility of charge trapping and silc creation in thin oxides after stress/anneal cycling," *Microelectronics Reliability*, vol. 38, no. 6-8, pp. 1057–1061, 1998.

[30] J. W. McPherson and D. A. Baglee, "Acceleration factors for thin oxide breakdown," *Journal of the Electrochemical Society*, vol. 132, no. 8, pp. 1903–1908, 1985.

[31] J. Mcpherson, V. Reddy, K. Banerjee, and H. Le, "Comparison of E and 1/E TDDB models for SiO_2 under logn-term/low field test conditions," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '98)*, pp. 171–174, San Francisco, Calif, USA, December 1998.

[32] B. J. O'Sullivan, L. Pantisano, P. J. Roussel, et al., "On the recovery of simulated plasma process induced damage in high-*k* dielectrics," in *Proceedings of the 44th IEEE International Reliability Physics Symposium (IRPS '06)*, pp. 365–370, San Jose, Calif, USA, March 2006.

[33] D. Qian and D. J. Dumin, "Field, time and fluence dependencies of trap generation in silicon oxides between 5 and 13.5 nm thick," *Semiconductor Science and Technology*, vol. 15, no. 8, pp. 854–861, 2000.

[34] S. Mahapatra, P. B. Kumar, and M. A. Alam, "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of p-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1371–1379, 2004.

[35] A. E. Islam, G. Gupta, S. Mahapatra, et al., "Gate leakage vs. NBTI in plasma nitrided oxides: characterization, physical principles, and optimization," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '06)*, pp. 329–333, San Francisco, Calif, USA, December 2006.

[36] S. Pae, M. Agostinelli, M. Brazier, et al., "BTI reliability of 45 nm high-k + metal-gate process technology," in *Proceedings of the 46th IEEE International Reliability Physics Symposium*, pp. 352–357, 2008.

[37] A. T. Krishnan, V. Reddy, and S. Krishnan, "Impact of charging damage on negative bias temperature instability," in *Proceedings of the International Electron Devices Meeting Technical Digest (IEDM '01)*, pp. 865–868, Washington, DC, USA, December 2001.