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Research Article

Analysis and Compensation of the AM-AM and AM-PM Distortion for CMOS Cascode Class-E Power Amplifier

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Analysis and compensation methodology of the AM-AM and AM-PM distortion of cascode class-E power amplifiers are presented. A physical-based model is proposed to illustrate that the nonlinear capacitance and transconductance cause the AM-AM and AM-PM distortion when modulating the supply voltage of the PA. A novel methodology that can reduce the distortion is also proposed. By degenerating common-gate transistor into a resistor, the constant equivalent impedance is obtained so that the AM-AM and AM-PM distortion is compensated. An experimental prototype of 2.6 GHz cascode class-E power amplifier with the AM-AM and AM-PM compensation has been integrated in a 0.18 μm CMOS technology, occupies a total die area of 1.6 mm^2. It achieves a drain efficiency of 17.8% and a power-added efficiency of 16.6% while delivering 12 dBm of linear output power and drawing 31 mA from a 1.8 V supply. Finally, a co-simulation result demonstrated that, when the distortion of the PA has been compensated, the EVM is improved from -17 dB to -19 dB with an IEEE802.11a-like signal source.

1. Introduction

To increase the data rate, recent wireless communication systems allow the carried information encoded in both amplitude and phase of the RF signal and therefore a linear power amplifier (PA) is required. The linearity achieved in such amplifiers by operating below their maximum output power has the drawback of low efficiency and hence reduced battery lifetime. The switching class-E amplifier is a potential candidate for power amplification in wireless transceivers [1]. However, the PA nonlinearity, the AM-AM and AM-PM distortion, causes the amplitude error and phase error on the output signal and then will severely degrade the emission performance of the system. As discussed in [2], the phase distortion in the class-E power amplifier should be less than the maximum accepted value (5°) in the OFDM-based transmitters.

For highly integrated transceivers, many researches have been focused on the switching class-E PA [3–7], by far the most efficient because hard switching operation and zero voltage switching (ZVS) conditions allow a strong reduction of power losses [7]. In CMOS, switching class-E amplifiers have been integrated with great success since a CMOS technology basically is a digital technology. Unfortunately, class-E amplifiers feature high peak voltages and currents, that seriously stress MOS devices, severely threatening circuit functionality. Moreover, device stacking, in class-E-based PAs, is a viable way to reduce the voltage swing on each device for reliability issues [8]. Cascode class-E PAs are allowed for reliability considerations. However, the linearity problem of the AM-AM and AM-PM distortion during supply modulation is the other design challenge to be concerned.

After identifying the main sources of the distortion in a cascode class-E PA in Section 2, this paper gives insights in the mechanisms of the distortion peculiar of a solution based on the cascode topology and proposed a design methodology for minimizing this distortion, in Section 3. Section 4 describes a design of 0.18 μm CMOS solution, comprising a class-E power amplifier and a self-biased control circuit. Experimental results are also presented in Section 5. Results of a system cosimulation are compared in Section 6. Finally, Section 7 draws conclusions.

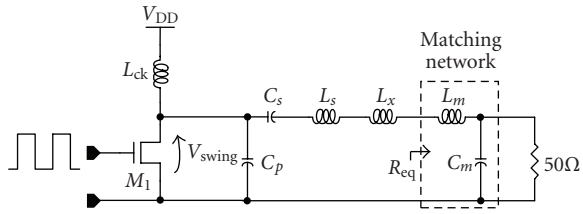

Figure 1: Schematic of common-source class-E PA.

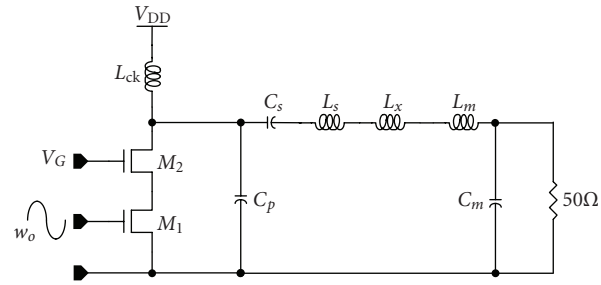

Figure 2: Schematic of CMOS cascode class-E PA.

2. Class-E PA Design

2.1. Basic Principle. In class-E PA, the voltage-current separation for efficiency enhancement is obtained by using a tuned LC network. The switch is closed at the instant where both the switch voltage and its first derivative are zero. The requirement of a zero first derivation makes the amplifier less sensitive to component variations. This leads to the well-known class-E conditions as stated by N. O. Sokal and A. D. Sokal [9]:

$$v_{\text{swing}}(t_1) = 0,$$
$$\left.\frac{\partial v_{\text{swing}}}{\partial t}\right|_{t=t_1} = 0, \tag{1}$$

where t_1 represents the instant at which the switch closes, and $v_{\text{swing}}(t_1)$ represents the switching voltage.

Figure 1 depicts a circuit that can satisfy the class-E requirements, provided that the correct component values are chosen. If the nMOS transistor is driven by a square wave, it can be viewed as a voltage controlled switch with a nonzero on-resistance R_{on}. The lowpass matching network made of L_m and C_m transforms 50 Ω, representative of the antenna resistance, into a lower value R_{eq}. The value of R_{eq} is chosen to deliver a desired amount of power with a specific supply voltage V_{DD}. This network acting as a filter also rejects the harmonics of the class-E waveform at the drain of the nMOS switch. In the original class-E design of Sokal, the RF-choke (L_{ck}) is made very large so it acts as a current source. C_s and L_s form a series resonator tuned at the desired frequency. Since the class-E working conditions are given by two equations, two components of the circuit can be chosen in such a way that the amplifier fulfills the class-E working conditions. For the circuit of Figure 1, these two components are the capacitor C_p and the inductor L_x. In this way, all components are determined.

2.2. Cascode-Based Topology. Regarding gate-oxide breakdown which occurs, if high voltages drop across the gate oxide, deserves particular care in a conventional common-source class-E PA [10]. Due to the class-E operation, the peak drain voltage when the device is off can be as large as 3.56 times the DC supply value [11]. For reliability issues, some efforts had been made to break up with the cascode solution, depicted in Figure 2 [6, 12–14].

An additional device (M_2) is placed in series with the switching device (M_1). In this way, the peak V_{DS} voltage is divided between the two devices and the maximum oxide voltage drop is reduced.

In general, from the reliability standpoint, the bias voltage V_G of the common-gate transistor is specified by the V_{DD} supply. For highly integration, an RF-choke is replaced by a small dc-feed. However, in practice, M_1 has a finite on-resistance and the transition time from the off-state to the on-state. These factors cause a certain amount of power dissipation on the switch, resulting in a reduction in power efficiency [15].

2.3. AM-AM and AM-PM Distortion. The AM-AM distortion is the difference between the supply voltage and the envelope of the RF output voltage. Such a difference is caused by a nonlinear relationship between the supply voltage and the envelope of the RF output signal. The AM-AM distortion in the RF PA itself can be kept low if it is always operated as a switching amplifier. In other words, the supply voltage of the PA driver stage will be kept high to ensure the switching nature of the amplifier. Besides the AM-AM, the AM-PM distortion will also be presented in the circuit. This distortion is an unwanted phase modulation of the RF output carrier due to the modulation of the supply voltage.

When modulating the PA supply, different operating regions of the transistor M_2 produce a nonlinear capacitance and a transconductance. These nonlinear components cause the AM-AM and AM-PM distortion at the output signal. The model is illustrated in Figure 3.

In small supply V_{DD}, M_2 operates in the deep-triode region and occupies extremely small voltage V_{DS2}. When V_{DD} is large enough to turn M_1 completely on, M_2 can be used for current driving and obtaining a significant voltage headroom V_{DS2}. According to the statement above, the voltage V_{DS2} is expressed as

$$V_{\text{DS2}} = \begin{cases} 0, & \text{for } V_{\text{DD}} < V_c, \\ V_{\text{DD}} \times \dfrac{(1/2)V_{\text{DD,peak}} - V_c}{V_{\text{DD,peak}} - V_c} + V_c & \\ \quad \times \dfrac{(1/2)V_{\text{DD,peak}}}{V_{\text{DD,peak}} - V_c}, & \text{for } V_{\text{DD}} \geq V_c, \end{cases} \tag{2}$$

where $V_{\text{DD,peak}} = 1.8\,\text{V}$, $V_c = (V_G - V_{\text{th}})/\lambda$ and λ is the ratio of the maximum peak-drain voltage of M_2 to $V_{\text{DD,peak}}$. Besides,

the capacitance C_{db2} and transconductance g_{m2} of M_2 can be given by

$$C_{db2} = \frac{C_{j0}}{\sqrt{1 + V_{DS2}/V_{bi}}}, \quad (3)$$

$$g_{m2} = \mu_n C_{OX}\left(\frac{W}{L}\right)_{M_2}(V_{GS2} - V_{th}), \quad (4)$$

where V_{bi} is the built-in potential of the body diode, C_{j0} is the output capacitance as $V_{DS2} = 0$, and V_{GS2} is gate-to-source voltage of M_2. Equations (2) show that the variations of the V_{DD} supply caused a nonlinear voltage V_{DS2}. In (4), the voltage V_{GS2} can also be expressed as $V_G - (V_{DD} - V_{DS2})$. Combining (2)–(4), the relationship of C_{db2} and g_{m2} against V_{DD} is plotted in Figure 4. The result indicates that the varied V_{DD} supply causes the nonconstant capacitance C_{db2} and the nonconstant tranconductance g_{m2}.

To illustrate the AM-AM and AM-PM distortion, the impedance $|Z_{ds2}|$ at the carrier frequency is derived according to the equivalent model and has been given by (5).

$$\begin{aligned}|Z_{ds2}| &= \left|\frac{V_{ds2}}{I_{ds2}}\right| \\ &= \left|\frac{V_{ds2}}{g_{m2}V_{gs2} + j\omega_o C_{db2}V_{ds2} + j\omega_o C_{gd2}\lambda V_{DD}}\right| \\ &= \left|\frac{V_{ds2}}{g_{m2}(V_G - (\lambda V_{DD} - V_{ds2})) + j\omega_o\left(C_{db2}V_{ds2} + C_{gd2}\lambda V_{DD}\right)}\right| \\ &= \sqrt{\frac{V_{DS2}^2}{\left(g_{m2}(V_G - \lambda V_{DD} + V_{ds2})\right)^2 + \left(\omega_o\left(C_{db2}V_{ds2} + C_{gd2}\lambda V_{DD}\right)\right)^2}},\end{aligned} \quad (5)$$

where C_{gd2} and ω_o denote the gate-to-drain capacitance of M_2 and angular frequency, respectively. To validate this analysis, the circuit performance was simulated by Agilent ADS simulator, assuming a 0.18 μm CMOS technology and the following parameter values: $V_{DD} = 1.8$ V, $\omega_o = 2\pi \cdot 2.6$ Grad/sec, $L_{ck} = 2$ nH, $C_s = 5$ pF, $C_m = 0.9$ pF, $(W/L)_{M_1,M_2} = (1080/0.18)\,\mu$m/$\mu$m, and the totally inductance of L_s, L_x, and L_m is 2.9 nH. The simulated and theoretical results of $|Z_{ds2}|$ are compared in Figure 5. The theoretical result is in good agreement with the simulated result and also indicates that the variant capacitance and the transconductance of M_2 bring a nonconstant $|Z_{ds2}|$. The difference between the theoretical result and the simulated result is due to the saturation voltage of transistors and the voltage drops of L_{ck} are neglected. Furthermore, the output drain voltage waveform of M_2 suffers from the magnitude and phase errors due to the nonconstant impedance. The PA output signal accompanies with the magnitude and phase errors from the drain node, so-called the AM-AM and AM-PM distortion. The simulated result of the AM-AM and AM-PM distortion is shown in Figure 6.

The result reveals that the relationship of the envelope of the RF output voltage against the supply V_{DD} is nonlinear and the voltage deviation at $V_{DD} = 0$ V causes an additional distortion at low envelope levels. When the supply voltage of the amplifier deviates from its optimum value (1.8 V), maximum AM-PM changes by 21 degrees/V and 18° of the phase error down to 0.5 V. In the supply voltage of 0 V to 0.5 V, the AM-PM is highly nonlinear and the phase error is as large as 67°. These characteristics indicate that low envelope levels are harder to reconstruct than high envelope levels.

3. Compensation Methodology

3.1. Improved AM-AM and AM-PM. Since various impedances will cause the nonlinear effect, a constant $|Z_{ds2}|$ should be designed to compensate this distortion. To obtain a constant $|Z_{ds2}|$, one of design solutions is to force the transistor M_2 to act as a resistor. When the common-gate transistor has been operated as a resistor, it is expected that the nonlinear capacitance and transconductance should be canceled. This requirement is realized by a voltage adder, as shown in Figure 7.

In Figure 7, the adder produces a voltage, which equals the threshold voltage V_{th} plus the supply V_{DD}, on the gate node of M_2 and therefore M_2 will be operated as a triode-mode resistor. During supply modulation the output voltage of the adder varied with the supply V_{DD} always forces M_2 to operate as a triode-mode resistor while M_1 is a switch. Therefore, a constant $|Z_{ds2}|$ is obtained and its simulated result is shown in Figure 8. The result shows that the voltage V_{DS2} is linearized and hence a constant $|Z_{ds2}|$ is obtained.

The results of the PA with and without the AM-AM and AM-PM compensation are compared in Figure 9. When the PA has the compensation, the relationship of the envelope of the output voltage against the supply voltage is linear and the AM-PM in the supply voltage of 0.5 V to 1.8 V is improved from 18° to 3°. Therefore, the proposed methodology evidently has compensated the AM-AM and AM-PM distortion of the PA during supply modulation.

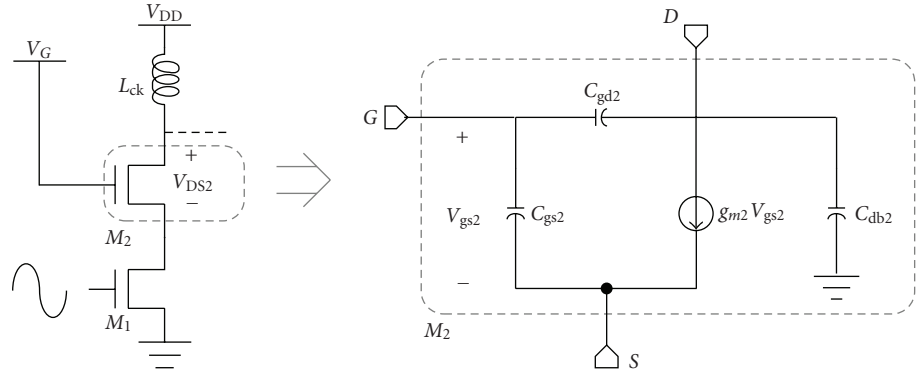

Figure 3: Equivalent model of the transistor M_2.

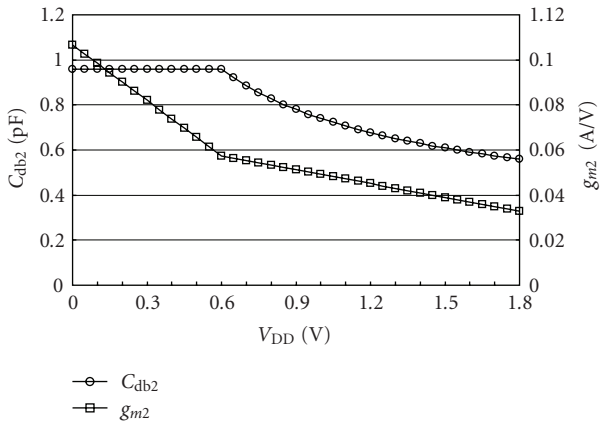

Figure 4: Theoretical results of C_{db2} and g_{m2}.

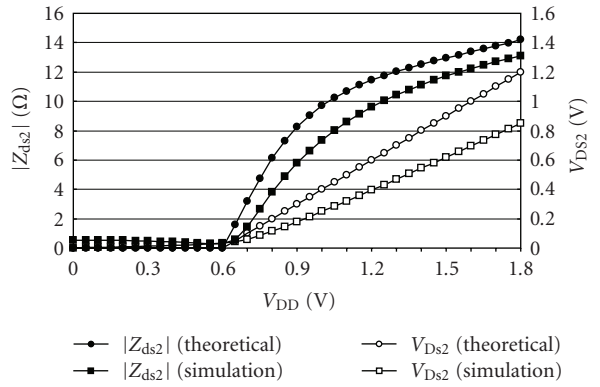

Figure 5: Theoretical and simulated result of $|Z_{ds2}|$ and V_{DS2} against supply voltage.

3.2. Efficiency Analysis. One more advantage of the transistor M_2 operating as a resistor is to pull up drain efficiency in low supply voltage and extend the operating supply range. The DC current (I_{DC}) in [16] can be rewritten by (6), where V_{dmin} means the finite drain-to-source voltage during the transistor conducting and R_s is the source terminal resistance. Drain efficiency of the PA can be expressed by (7). When the PA with or without the proposed compensation methodology is

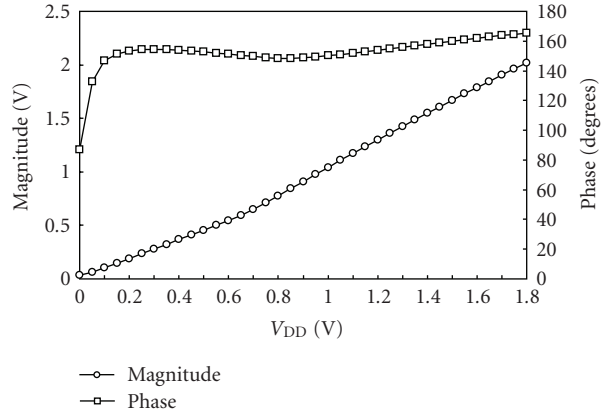

Figure 6: AM-AM and AM-PM distortion.

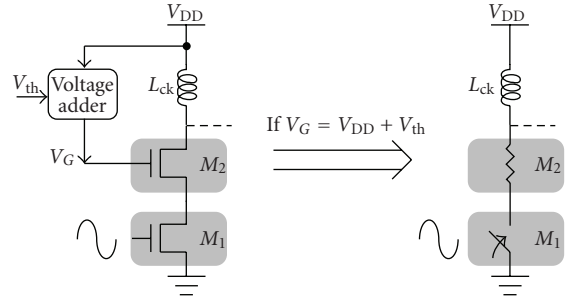

Figure 7: Equivalent schematic of the PA when the PA with AM-AM and AM-PM compensation.

operating on the identical conditions of P_{out} and V_{DD}, drain efficiency is inversely proportion to I_{DC}:

$$I_{DC} = \frac{\pi\omega\left(C_{db2} + C_{gd2}\right)(V_{DD} - V_{dmin})}{1 + 2\pi\omega R_s\left(C_{db2} + C_{gd2}\right)}, \quad (6)$$

$$\text{Efficiency} = \frac{P_{out}}{P_{DC}} \times 100\% \propto \frac{P_{out}}{V_{DD}I_{DC}} \propto \frac{1}{I_{DC}}. \quad (7)$$

Figure 10 shows the results of I_{DC} and drain efficiency versus the supply voltage. In small supply voltage, the I_{DC} value of the PA with compensation is less than the PA without

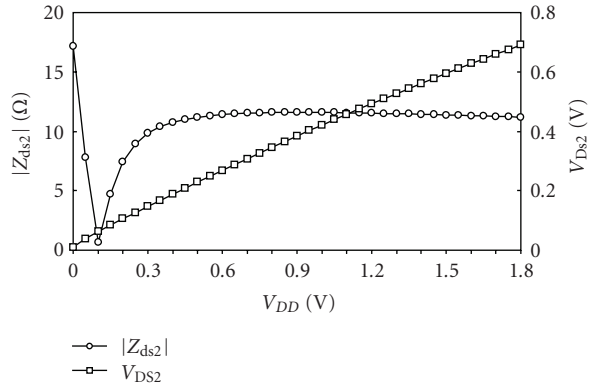

Figure 8: Simulated $|Z_{ds2}|$ and V_{DS2} against supply voltage when the PA with compensation.

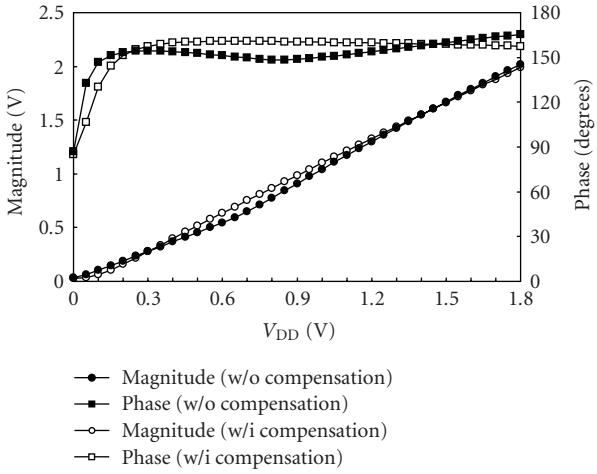

Figure 9: Compared AM-AM and AM-PM distortion.

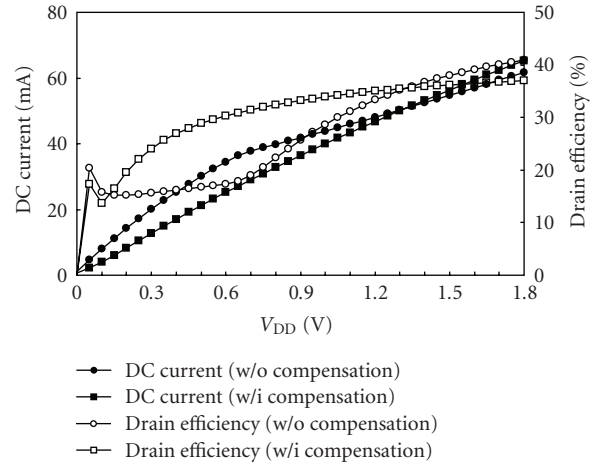

Figure 10: Compared DC current and drain efficiency.

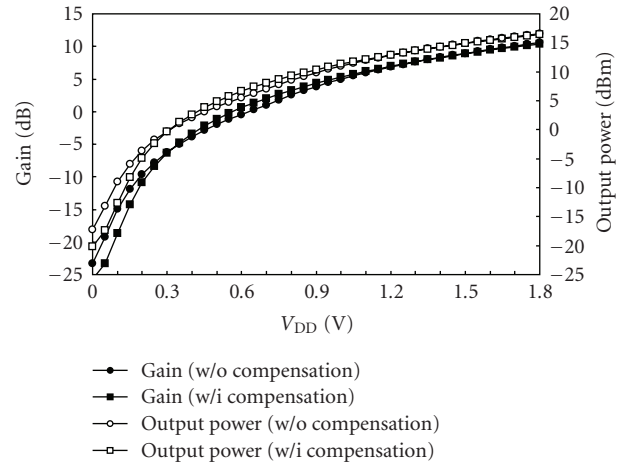

Figure 11: Gain and output power against supply voltage.

compensation and therefore drain efficiency of the PA is increased. The maximum improvement of 15% is achieved at $V_{DD} = 0.65$ V. This improvement benefits the operation of the PA in low supply voltage. In other words, the proposed methodology can extend the operating supply range during supply modulation since the PA has the slightly degradation in drain efficiency in high supply voltage. The results of power gain and output power against the supply voltage are also reported in Figure 11, where the input driving power is 6 dBm. When the amplifier is compensated, the power gain and output power of the PA are not degraded. The result indicates that the AM-AM and AM-PM distortion of the class-E power amplifier is compensated without degrading the circuit performance.

4. Implementation

A fully integrated cascode class-E power amplifier with a self-biased control circuit for compensating the AM-AM and AM-PM distortion has been implemented in a 0.18 μm CMOS technology, as shown in Figure 12. The amplifier operates at 2.6 GHz from a 1.8 V supply voltage and, to obtain the expected voltage V_{co}, the self-biased control circuit is applied by 3.3 V supply voltage. The 50 Ω load resistance is downconverted by means of the L_m-C_m network. The series of L_a-C_a are implemented to improve power efficiency [8]. A way to minimize the power loss is to tune out the capacitive parasitics by the inductor L_a, resonating parasitic capacitances on node P at the desired frequency of operation. A blocking capacitor C_a is inserted between the inductor L_a and ground. For highly integration, all of passive devices are implemented by the internal components. Considering the electrical performance of internal inductors, they have an allowed current density of 1 mA/μm at the temperature of 85°C and internal inductors have a maximum metal width of 20 μm, a thickness of 2 μm. Therefore, avoiding the metal damage of L_{ck}, the PA was designed to have an allowed current capacity. Hence, the large output power and drain efficiency are not the major design targets in this amplifier. The aspect sizes of the transistor M_1 and M_2 are 1080/0.18 μm/μm.

The self-biased control circuit tends to produce a voltage, the sum of a DC voltage and an analogue voltage. It is

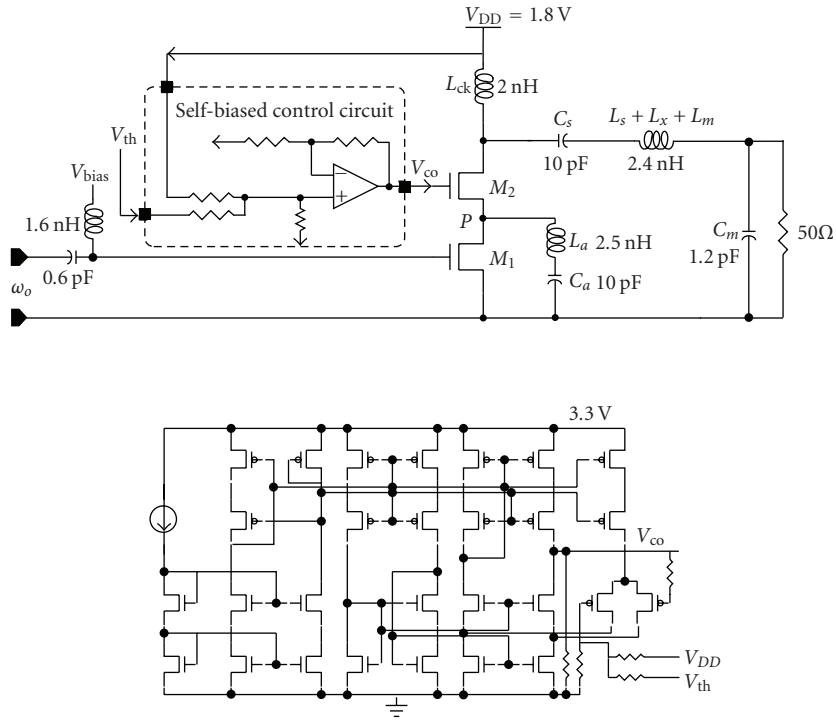

Figure 12: Detailed schematic of proposed PA.

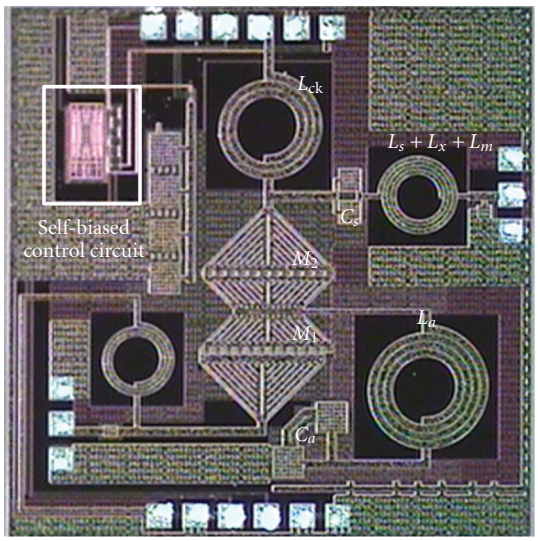

Figure 13: Die photo.

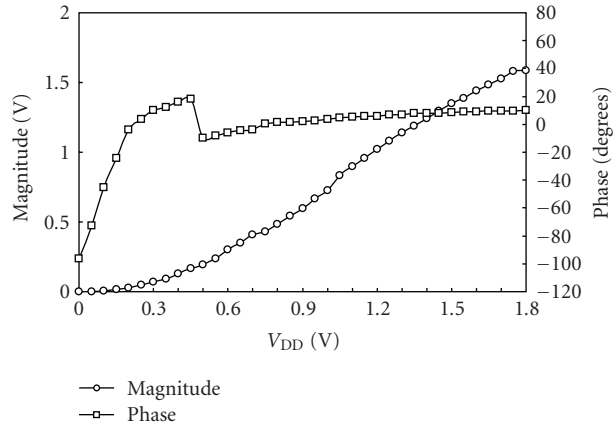

Figure 14: Measured AM-AM and AM-PM effect.

implemented by a voltage adder, including an operating amplifier with several resistors. Selecting the ratio of resistors, the expected output voltage is obtained. Besides, the operating amplifier has the unit-gain frequency of 100 MHz for achieving a correct output voltage of the self-biased control circuit during supply modulation. The control circuit is just to produce a gate biasing voltage of M_2, so that it only draws few micro amperes from the 3.3 V supply.

5. Experimental Results

Fabricated prototypes have been measured by the probe testing. The chip photomicrograph is reported in Figure 13. Total die area is 1.6 mm^2. Figure 14 shows the measured characteristics of the AM-AM and AM-PM of the PA. The phase error is reduced down to 5° as V_{DD} is swept from 0.7 V to 1.8 V. A linear voltage relationship is also obtained and there is a small deviation in low supply voltage, from 0 V to 0.3 V. As expected, the AM-AM and AM-PM distortion of the class-E PA has been compensated by using proposed design methodology. The prototype delivers an output power of 12 dBm with a 1.8 V supply voltage and an input driving

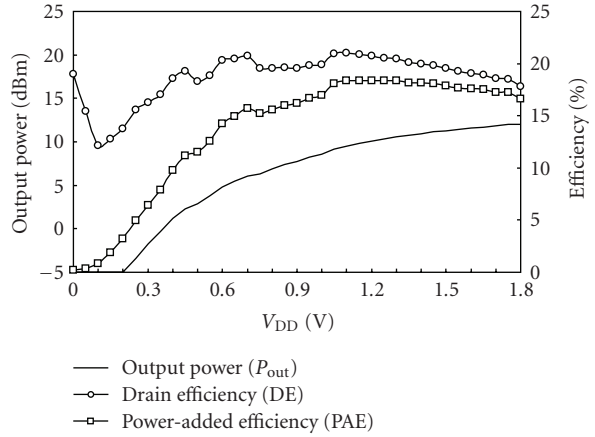

Figure 15: Measured output power (P_{OUT}), PAE, and drain efficiency (DE) versus V_{DD}.

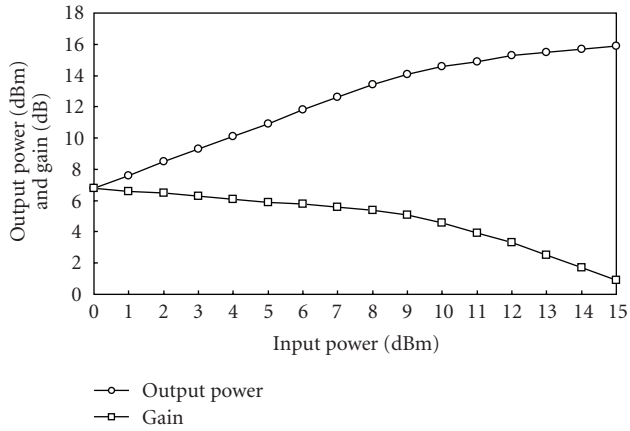

Figure 16: Measured output power and power gain versus input power.

power P_{IN} of 6 dBm. The output power can be regulated by changing the supply voltage of the amplifier. Figure 15 shows the measured output power (P_{OUT}), drain efficiency (DE), and power-added efficiency (PAE) versus V_{DD}. Drain and power-added efficiencies are defined as follows [17, 18]:

$$\text{DE} = \frac{P_{\text{OUT}}}{P_{\text{DC-PA}}} \times 100\%,$$
$$\text{PAE} = \frac{P_{\text{OUT}} - P_{\text{IN}}}{P_{\text{DC-BIAS}} + P_{\text{DC-PA}}} \times 100\%, \quad (8)$$

where $P_{\text{DC-BIAS}}$ and $P_{\text{DC-PA}}$ are the power drawn from the supply by the control circuit and PA stage, respectively.

The output power increases proportionally to $V_{DD}{}^2$, varying from −2 dBm to 12 dBm, as V_{DD} is swept from 0.3 V to 1.8 V. In small supply voltage, the transistors can not be completely on so that the amplifications of the RF signal are not available. Drain efficiencies are close to 20% in V_{DD} of 0.5 V to 1.8 V. As the supply voltage below 0.6 V, the PAE has seriously reductions, whereas the PAE reduces when the output power becomes comparable to the input power. Due to the targeted output power reduced from 16 dBm to

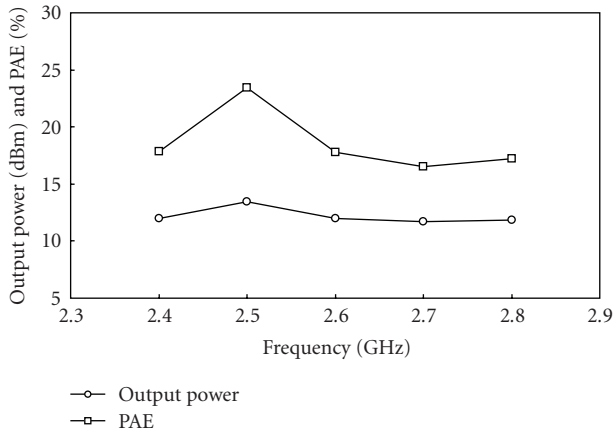

Figure 17: Measured output power and PAE versus frequency.

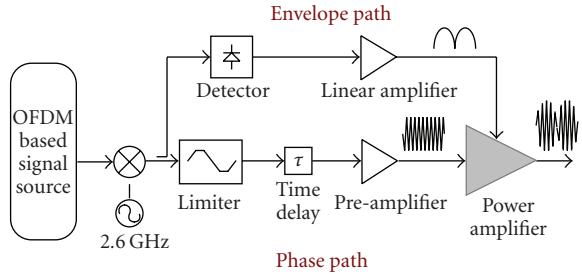

Figure 18: System cosimulation platform of EER.

12 dBm, the maximum PAE is also reduced to 16.6%. The output power and power gain versus the input power are also reported in Figure 16. The PA has the output power of 12 dBm and power gain of 6 dB with an input driving power of 6 dBm. When P_{IN} is above 7 dBm, the power gain of the PA is degraded to 5 dB. The result of the output power versus frequency is shown in Figure 17. The output power is above 12 dBm in the 2.3 GHz to 2.8 GHz frequency band, leading the power amplifier to operate in a wide frequency band. The maximum PAE in this wide frequency band is 23.5%.

The design proposed here shows that the AM-AM and AM-PM distortion of the cascode class-E PA has been compensated by a self-biased control circuit without dissipating more power. However, because of the concern of an allowed current capacity on the top metal layer, the aspect sizes of the transistors for efficiency optimization are difficult to achieve. Therefore, the equivalent series resistances of the transistor are large when the transistor is on, so that there is reduction on the drain voltage waveform and the output power. Due to the reduction of the output power, the efficiency of the amplifier is also reduced.

6. System Verification

A system cosimulation platform of envelope elimination and restoration (EER) architecture shown in Figure 18 was established to determine the influence of the AM-AM and AM-PM distortion of the cascode class-E PA on

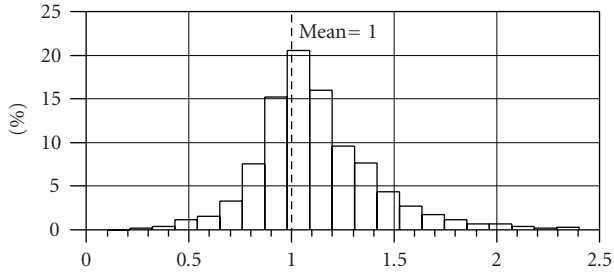

Figure 19: Histogram of the envelope voltage.

Table 1: Performance summary.

	Simulation (AM-PM)	Cosimulation	Measurement (AM-PM)
w/o compensation	18° (0.5 V–1.8 V)	EVM = −17 dB	N/A
w/i compensation	3° (0.5 V–1.8 V)	EVM = −19 dB	5° (0.7 V–1.8 V)

system performance. The signal source, an IEEE802.11a-like broadband OFDM transmission with 20 MHz bandwidth and operating at a 2.6 GHz frequency, is generated by an ADS Ptolemy simulator. The histogram of envelope voltage in Figure 19 shows that 93% of envelope voltages are in the range from 0.5 V to 1.8 V with a mean voltage of 1 V, while the request time delay is 2.8 nanoseconds [19]. Using the distortion compensation technique of the cascode class-E PA, the EVM can be improved from −17 dB to −19 dB, and the obtained constellation is shown in Figure 20.

All of results have been summarized on Table 1. It shows that the proposed methodology can effectively compensate the distortion of the PA while the measurement result is also in good agreement with the simulation result.

7. Conclusions

A cascode class-E PA with a self-biased circuit has been proposed in this paper to achieve the reduction of the AM-AM and AM-PM distortion. We carefully investigated the distortion in cascode class-E PAs, finding that an equivalent triode-resistor by the common-gate transistor is a way to cancel the nonlinear capacitance and the transconductance for the reduction of the AM-AM and AM-PM distortion. A simplified equivalent model is introduced to illustrate the mechanisms of the distortion. Furthermore, a design methodology for compensating this distortion has been identified and a circuit solution has also been proposed. The prototype of 2.6 GHz class-E amplifier, realized in a 0.18 μm CMOS technology, has demonstrated that the phase error is reduced down to 5° in the supply voltage of 0.7 V to 1.8 V and the output power of 12 dBm over the 2.3 GHz to 2.8 GHz frequency band from a 1.8 V supply voltage. The EVM of an EER on a system cosimulation is improved from −17 dB to −19 dB.

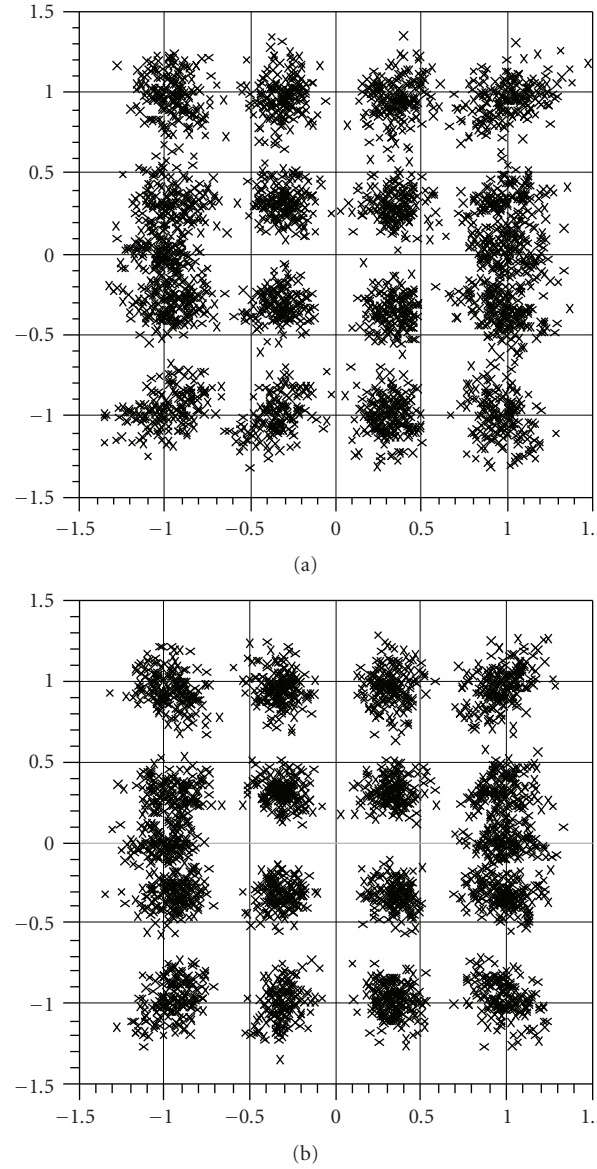

Figure 20: Obtained constellations (a) without compensation and (b) with compensation.

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