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Research Article

Low Phase Noise and High Conversion Gain Oscillator Mixer Constructed with a 0.18-μm CMOS Technology

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This paper presents a compact down-conversion oscillator mixer fabricated with a 0.18-μm CMOS technology. The oscillator mixer consists of a conventional nMOS differential coupled oscillator, a switch stage, and a pMOS cross-coupled pair which is used to release the design constraint between the conversion gain and the start-up condition. Since the switch stage and the pMOS cross-coupled pair are stacked on the nMOS differential oscillator, the bias currents of the switch stage and the pMOS cross-coupled pair can be entirely reused, so as to reduce the power dissipation. The experimental results show a conversion gain of 6.5 dB at 2.1 GHz associated with a single-sideband (SSB) noise figure of below 13 dB. The oscillator mixer also exhibits a tuning range of 184 MHz and a phase noise of −116 dBc/Hz at 1-MHz offset from the LO frequency of 6.8 GHz, and it consumes 11 mA from 1.8 V bias voltage.

1. Introduction

Low power and highly integrated circuits (ICs) are key issues for developing components or modules of wireless communications systems. Hence, work undertaken during the past few years has focused on achieving higher levels of integration and low current consumption. Many efforts have been made to combine the oscillator and mixer into a single unit for such purposes [1–5].

In the work [2], a 2-GHz 1.6-mW phase-locked loop (PLL) fabricated by using a 0.6-μm BiCMOS technology was proposed. The oscillation and mixing function is achieved by stacking two differential pairs on ring oscillator for low power consumption. However, the oscillator mixer employs inductive peaking, level shift, and extra speed-up current sources to improve start-up condition and fasten speed of VCO core; these additional circuits make the design more complicated and increase parasitic capacitances which will reduce VCO's tuning range.

Another double-balanced oscillator mixer constructed with a 0.18-μm CMOS technology has been reported to exhibit good performance and a compact configuration [3]. In such a CMOS oscillator mixer, the LO output signal is generated by the nMOS-only differential VCO which is directly fed into the source of the switching pair. Although, the configuration can be operated under low voltage supply, an extra bias voltage is needed for appropriate circuit operation. And the characteristics, for example, linearity and conversion gain, may be limited due to the demand for the low power dissipation.

To further reduce power consumption for global positioning system (GPS) applications, a RF front-end receiver topology merging LNA, mixer, and VCO into a single stage called the LMV cell is presented [4]. The LMV cell utilizes the intrinsic mixing functionality of a LC-tank oscillator to provide a compact and low-power solution. The virtual short-circuit is used to sense the output IF current for that to reduce conversion gain is sensitive to parasitic capacitors present at the IF nodes. However, to avoid a design trade-off between LNA and VCO, a low-frequency degeneration circuit must be introduced, attenuating the $1/f$ noise injected by the LNA core into the VCO.

In [5], a similar work has made to integrate a third-harmonic self-oscillating mixer with an antenna to form

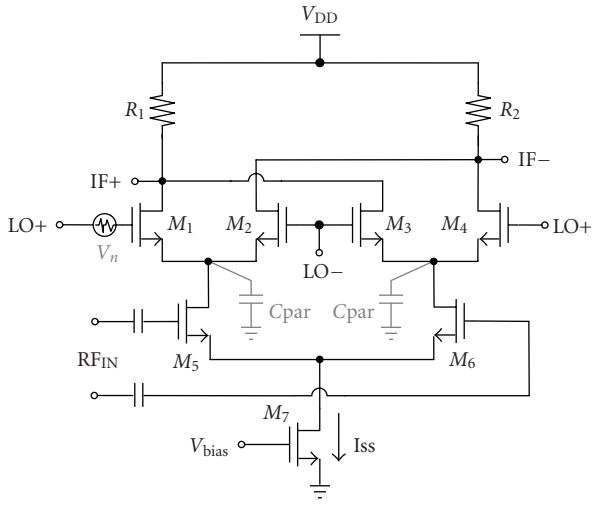


Figure 1: Conventional double-balance Gilbert mixer.

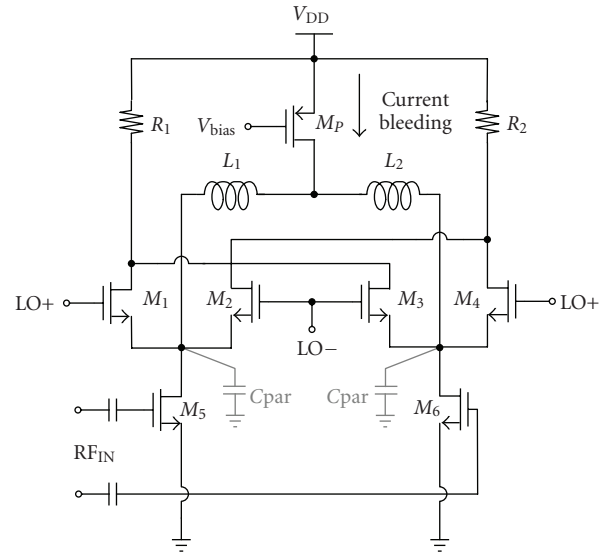


Figure 2: Circuit schematic of a mixer with static current injection.

high-performance receiver on a low-loss printed circuit board (PCB). However, the communication system may still be implemented using an MMIC technology as operation frequency significantly increases.

In this paper, a new circuit architecture that consists of a mixer and a VCO is proposed. Among this study procedure, we know that the proposed oscillator mixer cannot be synthesized by directly connecting an nMOS-only VCO and a mixer stage, however, the match problem and the amount of the bias current between the two circuits must be carefully considered. By using an additional pMOS cross-coupled pair to separate their bias currents and to compensate the loss of the LC-tank, it still preserves the characteristics of the low phase noise and the high conversion gain.

2. Circuit Design and Analysis

2.1. Oscillator Mixer Topology. Since active mixer has a larger gain than a passive mixer and relax noise performance of following circuit blocks, most down-converter ICs employ active mixer configurations. One of the commonly used active mixers is the double-balanced Gilbert mixer which mainly comprises an input transconductance stage, an LO switch stage, and output loads shown in Figure 1. The transconductance stage is applied to translate voltage-form RF signals into current-form RF signals. The switch stage is used to mix the RF currents with LO signals to generate IF signals. However, the parasitic capacitances (C_{par}) between the switch's sources and ground not only provide leakage paths that degenerate Gilbert mixer's conversion gain, but also corrupt input third-order intercept point (IIP3) due to the nonlinear characteristics of the parasitic elements. The above drawbacks will become more and more serious as circuit's operation frequency increases. Moreover, the parasitic capacitances also form an indirect mechanism that causes noise pulse to appear at output of Gilbert mixer and have been quantitatively derived as follows [5]:

$$i_{o,n} = \frac{2C_{\text{par}}}{T} V_n \cdot \frac{\left(C_{\text{par}}\omega_{\text{LO}}\right)^2}{g_{ms}^2 + \left(C_{\text{par}}\omega_{\text{LO}}\right)^2}, \tag{1}$$

where T is the period of the LO signal, g_{ms} is the transconductance of the LO switches, and V_n is the equivalent flicker noise of the switching pair. Based on (1), one can know that it rapidly goes up as the capacitances and the LO frequency increase. To alleviate the effect of the parasitic capacitances, a direct-conversion mixer to use current bleeding circuit and two resonating inductors has been proposed [6, 7], as shown in Figure 2. It had demonstrated that conversion gain and flicker noise performance of a Gilbert mixer are improved simultaneously by making the inductors ($L_{1,2}$) to resonate with the capacitors (C_{par}), and the transistor M_p conduct the most parts of the bias current for improving flicker noise of the switch stage (V_n). Nevertheless, the main goal in this paper is to preserve the above superior mechanism and to merge VCO and mixer into a single block for low power application.

A new configuration of oscillator mixer is obtained by translating the transistors (M_5 and M_6) of Figure 2 into a cross-coupled pair. Based on this structure, the transistors (M_5-M_6) and the inductors (L_1-L_2) construct the nMOS-only VCO that provides oscillation signal to drive the sources of the switch pairs, of which gates are controlled by the RF signals. However, to guarantee that the oscillator mixer can work properly, a fundamental design criterion is to make the VCO's start-up condition hold. Such a condition may be satisfied if the negative resistance provided by the nMOS cross-coupled pair is enough to compensate the loss caused by the lossy LC tank. Moreover, we also have to reduce the parasitic capacitors (C_{par}) so as to improve the phase noise of the VCO core due to its bad quality factors. Thus, it is straightforward that the transistor sizes (M_1–M_4) must

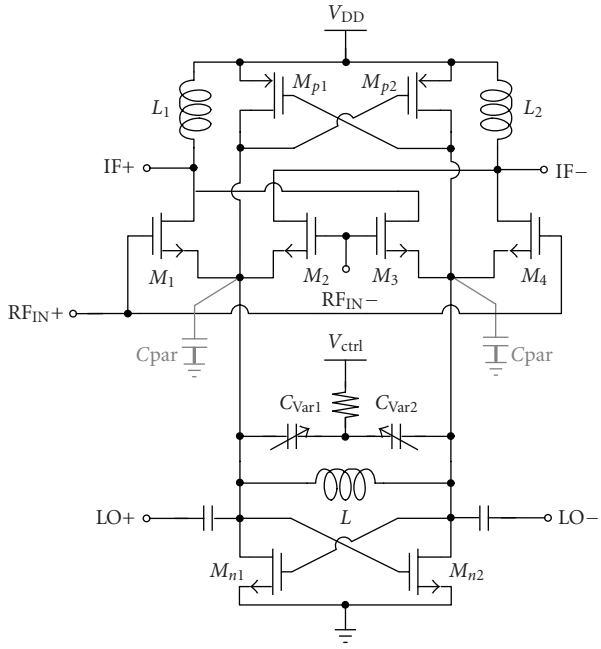


Figure 3: Circuit implementation of the proposed oscillator mixer.

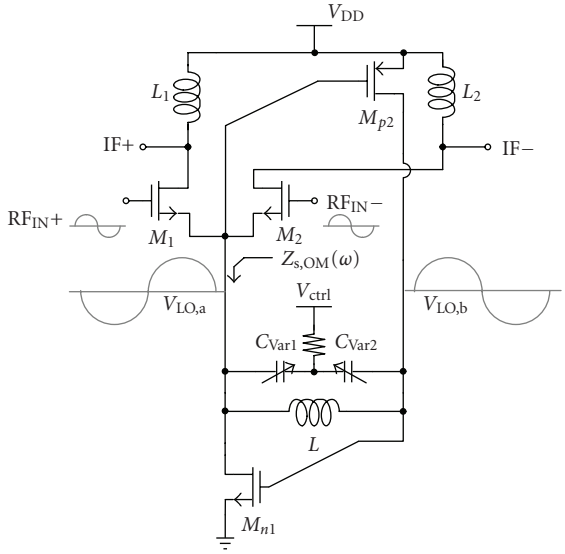


Figure 4: Half-circuit diagram of the oscillator mixer.

be reduced and high-Q inductors must be adopted. But Q factors of integrated inductors on CMOS substrate are quite low, and the use of small-sized switching transistors will degenerate the conversion gain of the mixer. To resolve the problem, one useful design strategy is to increase the bias current of nMOS cross-coupled pair through a current source realized by pMOS (M_p). However, based on experimental results, the architecture still needs an excess bias current to maintain good performance for higher frequency applications. Therefore, a new structure of oscillator mixer that employs a pMOS cross-coupled pair to alleviate the

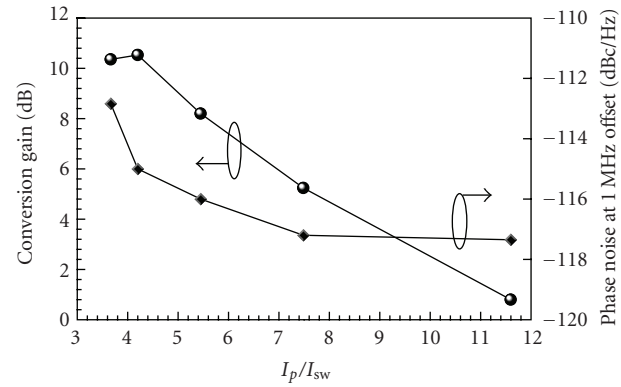


Figure 5: Conversion gains and phase noises versus different current ratio.

Table 1: Component design values of the proposed circuit.

Components	Value
$M_{p1,P2}$	$4\,\mu$m/$0.18\,\mu$m, $m = 25$
$M_{n1,P2}$	$4\,\mu$m/$0.18\,\mu$m, $m = 12$
$M_{1,4}$	$5\,\mu$m/$0.18\,\mu$m, $m = 20$
$L_{1,2}(W, \text{space}, r, N)$	7.79 nH ($15\,\mu$m, $2\,\mu$m, $90\,\mu m$, 5)
L (W, space, r, N)	0.552 nH ($15\,\mu$m, $2\,\mu$m, $110\,\mu$m, 1)
V_{DD}, V_{RF}	1.8 V, 1.35 V

confined design between the conversion gain and the start-up condition, and uses the inductors (L_1-L_2) for the free of voltage headroom and flicker noise is proposed, as shown in Figure 3. The oscillator mixer plotted in the figure ignores the gate bias (V_{RF}) of the switching pair.

2.2. Voltage Gain Analysis. We assume that the differential LO signal of the VCO core is big enough to turn on or off the switch transistors. Thus, the circuit of Figure 3 is substituted with the half circuit of Figure 4. The frequencies of RF signals are assumed to be higher than those of the LO signals and to be considered as small signals. So, the switch time-variant conductance $g(t)$ can be derived as

$$\begin{aligned} g(t) &= \frac{\partial}{\partial V_{GS}}\left\{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{RF} - V_{LO,a}) - V_{TH}\right]^2\right\} \\ &= \mu_n C_{ox}\frac{W}{L}\left[V_{RF} - V_{LO}\sin(\omega_{LO}t) - V_S - V_{TH}\right], \end{aligned} \tag{2}$$

where V_{LO} is the LO magnitude and V_S is the source voltage of the transistors (M_1-M_2), V_{RF} is the dc bias for RF. Although the poor-quality parasitic capacitors, varactor and inductor losses are compensated by the cross-coupled pairs and are resonated at the frequency ω_{LO}, the resonant condition is not suitable for the RF signals. In other words, to calculate the voltage gain of the half-circuit should include the source impedance ($Z_{s,OM}(\omega)$). By following an analogous

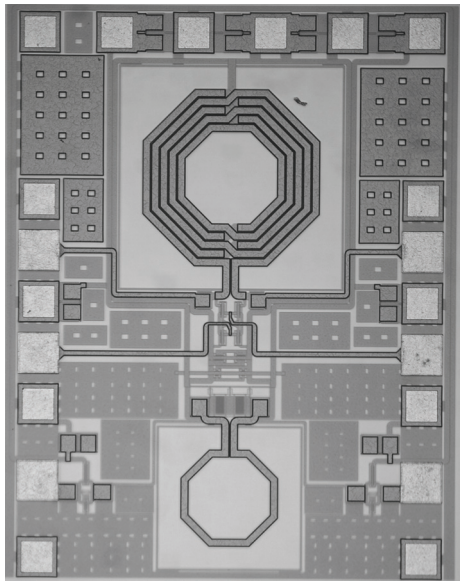


Figure 6: Photograph of the oscillator mixer with a size of 0.88 mm × 1.12 mm.

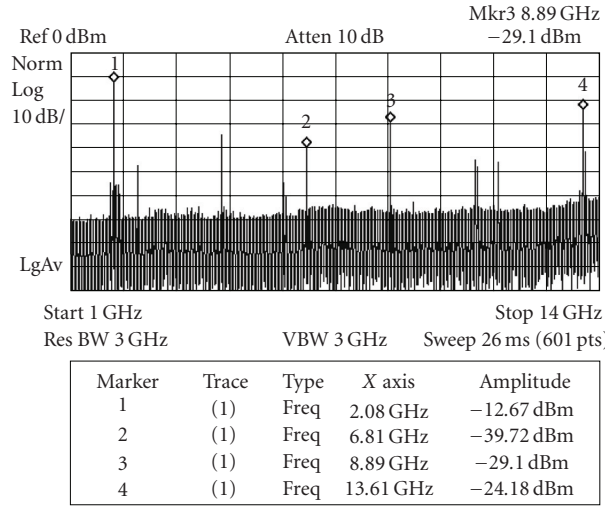
deviation of differential amplifier, the IF voltage gain is written as

$$\left|\frac{v_{\text{if}}(t)}{v_{\text{rf}}(t)}\right| = \frac{2\omega_{\text{IF}}L_{1,2}\,p(t)}{\frac{1}{\frac{1}{\left|Z_{s,\text{OM}}(\omega)\right|}+g_1(t)} + \frac{1}{\frac{1}{\left|Z_{s,\text{OM}}(\omega)\right|}+g_2(t)}}, \tag{3}$$

where $g_{1,2}(t)$ is the conductance of the differential pair ($M_{n1,n2}$), $p(t)$ is polarity of the differential IF voltage, and $L_{1,2}$ is the output load. According to (3), we know that the channel resistance of the nMOS cross-coupled pair (M_{n1},M_{n2}) and the LC-tank has critical effects for the voltage gain of the oscillator mixer. So, for improving the voltage gain of the oscillator mixer, it is preferred to adjust the widths of the nMOS cross-coupled pair as the LC-tank value must be chosen to be resonated at the required LO oscillation frequency in the proposed circuit. However, altering the sizes of the nMOS transistors affords a tradeoff between low phase noise and high conversion gain. Hence, a largely inductive load may be a better choice for the oscillator mixer.

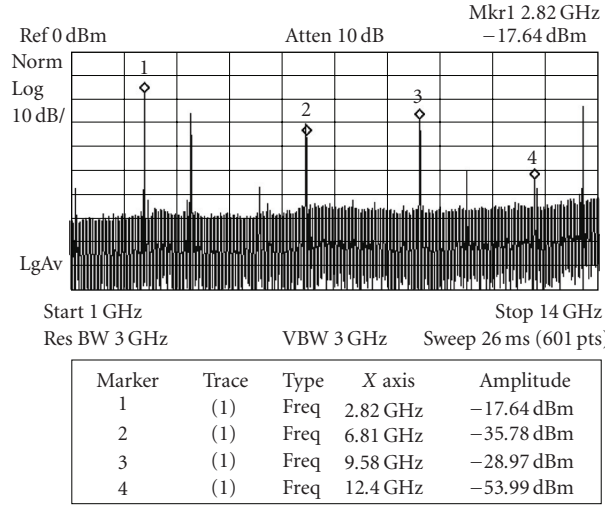
2.3. Phase Noise Analysis. The phase noise is another important issue for designing the oscillator mixer, because the actual spectrum of the VCO exhibits skirts around the carrier frequency that may allow the strong unwanted signal or noise to corrupt the IF signal via modulation mechanism. According to the phase noise model proposed by Hajimiri and Lee, the phase noise of LC- tank VCO operated in the current-limited regime for the $1/f^2$ region is given by [8, 9]

$$L(\Delta\omega) = \frac{\gamma g_{n,p} + \left(1/Q_{\text{ind}}r_p\right)}{C_{\text{var}}I_B Q_{\text{ind}} r_p}\,\frac{2kT\Gamma_{\text{rms}}^2}{\Delta\omega^2}, \tag{4}$$



Marker	Trace	Type	X axis	Amplitude
1	(1)	Freq	2.08 GHz	−12.67 dBm
2	(1)	Freq	6.81 GHz	−39.72 dBm
3	(1)	Freq	8.89 GHz	−29.1 dBm
4	(1)	Freq	13.61 GHz	−24.18 dBm

(a)



Marker	Trace	Type	X axis	Amplitude
1	(1)	Freq	2.82 GHz	−17.64 dBm
2	(1)	Freq	6.81 GHz	−35.78 dBm
3	(1)	Freq	9.58 GHz	−28.97 dBm
4	(1)	Freq	12.4 GHz	−53.99 dBm

(b)

Figure 7: (a) Measured IF output spectrum of the oscillator mixer using the RF frequency of 8.9 GHz, and (b) the RF frequency of 9.6 GHz.

where r_p is the parasitic resistance of the inductor, $g_{n,p}$ is the conductance of the cross-coupled pairs, Q_{ind} and I_B are the Q factor of the inductor (L) and the bias current of the VCO, respectively. $\Delta\omega$ is the offset frequency from the carrier, and Γ_{rms} is the rms value of the effective impulse sensitivity function (ISF) which represents the time-varying sensitivity of the distributions of phase noise. The parameter γ has a value of unity at zero V_{DS} and 2/3 in saturation region with long channel devices. Equation (4) demonstrates that $L(\Delta\omega) = f(Q_{\text{ind}}, I_B, C_{\text{var}})$ can be improved by increasing Q_{ind}, or designing I_B near the maximum position in current-limited regime. By taking derivation of (4) with respect to the varactor C_{var}, we can know that VCO's phase noise is associated with tuning range. In this work, a narrow-tuned varactor is chosen to reduce the variation of the phase noise in the range of the control voltage (V_{ctrl}).

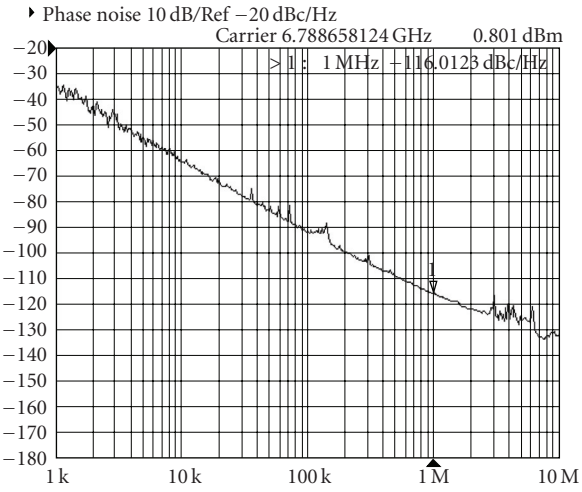


Figure 8: Measured phase noise of the oscillator mixer.

2.4. Oscillator Mixer Design Analysis. Based on (3) and (4), we realize that the performance of the conversion gain and phase noise is related to the conductances of the switching and the pMOS cross-coupled pairs. To gain deeply insight into the problem, Figure 5 reports the simulations of the conversion gain and the phase noise versus the ratio of I_p/I_{sw}. Here, I_{sw} and I_p stand for the bias currents of the switching transistors and the pMOS cross-coupled pair, respectively. Notice that we must ensure the sum of I_{sw} and I_p to be as consistent as possible through all simulated cases in despite of resulting a little difference for the wanted oscillation frequency (the variation approximate ±75 MHz at the center frequency of 6.8 GHz). Since the summed current is entirely reused by the nMOS cross-coupled pair, the percentage of the current reuse is 100%. Based on simulated results, the oscillator mixer can provide good performance while maintaining suitable bias points; that is, V_{DD} and V_{RF} should be set to 1.8 V and 1.35 V, respectively. The detail design parameters of the proposed oscillator mixer are listed in Table 1. The simulated results of Figure 5 shows that the conversion gain drops rapidly as the bias currents in the switch stage reduces, and the phase noise has not obvious variation while the ratio is larger than 7. The quick attenuation of the conversion gain is that it mainly depends on the switch's transconductance under the assumption of the fixed source impedance ($Z_{s,\mathrm{OM}}(\omega)$). The slow variation of the phase noise is that the VCO core has been operated at the current-limited regime while I_p/I_{sw} is set to 7. For optimizing phase noise, besides to alter VCO's bias current, channel noise in active transistors and output parasitic capacitors (C_{par}) must also be considered [10]. This paper mentioned that the ISFs (Γ_{rms}) of the VCO's cross-coupled pairs strongly depend on the parasitic capacitances between LC-tank outputs and ground if high impedance levels at the sources of nMOS and pMOS cross-coupled pairs is absent.

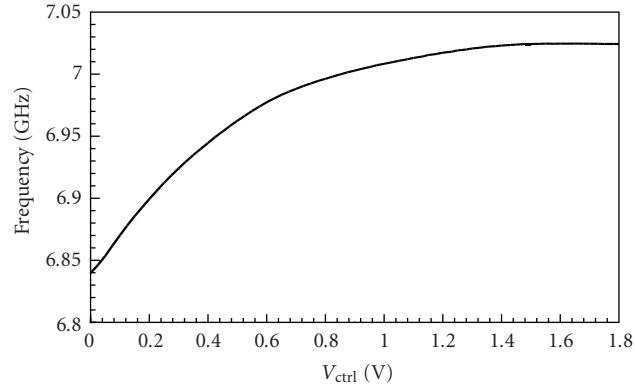


Figure 9: Measured tuning range of the VCO core.

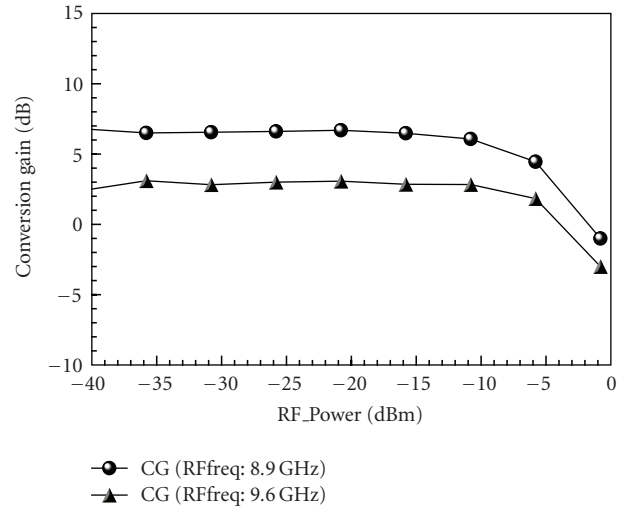


Figure 10: Measured conversion gain and outputted power versus input RF power.

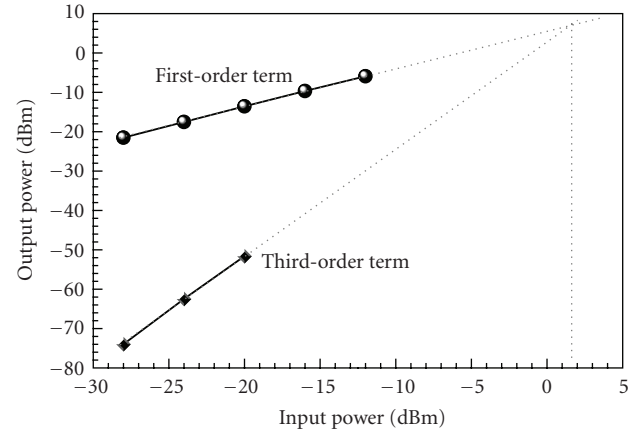


Figure 11: Measured IIP3 of the prototype.

3. Experimental Results

Figure 6 shows die photograph of the prototype, of which chip area including probe pads is 0.88 mm × 1.12 mm.

Table 2: The performance comparisons of other oscillator mixers and the proposed circuit.

Ref.	[2]	[3]	[4]	This work
IF Freq. (MHz)	55	3–5	140	2.1×10^3-2.8×10^3
Oscillation Freq. (GHz)	4.05–4.55	n.a.	1.863	6.79–7.01
Phase Noise (dBc/Hz)	−113 at 1 MHz	−104 at 1 MHz	n.a.	−116.6 at 1 MHz
SSB Noise Figure (dB)	14.5	4.8	6.9	13
Down-Conversion Gain (dB)	2.5	36	11.1	6.5
IIP3 (dBm)	−11.8	−19	4.5	1.5
1dB Comp. Point (dBm)	−24	−31	n.a.	−11
LO-to-IF Isolation (dB)	>35	n.a.	n.a.	>16
RF-to-IF Isolation (dB)	n.a.	n.a.	n.a.	>18
LO-to-RF Isolation (dB)	>29	n.a.	n.a.	>12.7
Technology	0.18-μm CMOS	0.13-μm CMOS	NE34018 FETs	0.18-μm CMOS
Area (mm^2)	0.96	1.5	n.a.	0.99
Power Consumption (mW)	3.34	11	32	21

The prototype was fabricated in 0.18 μm 1P6M CMOS technology provided by TSMC foundry. The chip was tested by mounting the prototype on a low-loss Teflon PCB board, which contains one RF rat-race hybrid and two bias-tees. The total drawing currents that exclude the LO buffers are 11 mA. Figures 7(a) and 7(b) depict the IF output spectrums of the oscillator mixer without using additionally integrated IF buffer amplifiers. In the measurements, the RF test signals that have the same input power of −15 dBm are set to 8.9 and 9.6 GHz, respectively. To yield the IF signals of 2.1 and 2.8 GHz, the self-generated oscillation signal is adjusted to 6.9 GHz by using $V_{\text{ctrl}} = 0.2$ V. The power consumption of the switching pair is about 3.13 mW and a higher power of 17 mW is consumed by the VCO core to obtain the request amplitude level for achieving the high conversion gain and low phase noise. These measured results also reveal that the LO-to-IF isolation and RF-to-IF isolation in both cases are higher than 18 and 16.4 dB, respectively. The suppressed capability of the oscillator mixer that relates to LO and RF signal leakages is not good enough. It may be due to the merged mixer-VCO structure and the imperfect layout of the switching pair.

Both phase noise and tuning range were measured using an Agilent E5052A Signal Source Analyzer and an E5053A Downconverter. Figures 8 and 9 show the measured phase noise and tuning range of the oscillation signal which is delivered from CMOS buffers, respectively. The measured phase noise is −116 dBc/Hz at 1-MHz offset from the LO carrier, and the tuning range is 184 MHz. The performance of VCO is evaluated with a figure of merit defined in the work [11]

$$\text{FOM}(\text{dB}c) = S_{\text{SSB}} \cdot \left(\frac{f_{\text{offset}}}{f c}\right)^2 \cdot P_{\text{diss}}(\text{mW}), \tag{5}$$

where S_{SSB} is the signal sideband noise at offset frequency f_{offset}, and f_c and P_{diss} are the carrier frequency and DC power consumption of a voltage-controlled oscillator. The figure of merit (FOM) of the prototype is about −180 dBc/Hz. Figure 10 plots the measured 1-dB compression point (P1dB) that is about −11 dBm associated with a conversion gain of 6.5 dB while the RF input signal is 9.6 GHz. The two-tone test for third-order intermodulation distortion (IIP3) is shown in Figure 11. The test is performed at the RF frequency of 9.2 GHz, and tone spacing is 10 MHz. The measured IIP3 is about 1.5 dBm.

4. Conclusion

A compact down-conversion oscillator mixer operated in X-band is proposed. The oscillator mixer mainly constructed with an nMOS-only VCO and a switch stage. However, to improve start-up condition and achieve high conversion gain, an additional pMOS cross-coupled pair is employed. In this work, it was demonstrated by adjusting the ratio of I_p/I_{sw}, which is the ratio of the currents that flows into the pMOS transistors and the switching transistors, the oscillator mixer can achieve the high conversion gains and low phase noises as well. As the pMOS cross-coupled pair and the switch stage are stacked on the VCO core, these bias currents are entirely reused by the nMOS cross-coupled pair so that the total power consumption maybe reduced. A prototype was fabricated using CMOS 0.18-μm technology to validate the design concept. A summary of the measured results is provided in Table 2 along with a comparison to other oscillator mixer; it shows that the proposed configuration of the oscillator mixer demonstrates the characteristics of an moderate conversion gain and power consumption, and a low phase noise.

Acknowledgments

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