

## Research Article

# A Discrete-Time Downsampling FIR Filter for Windowed Integration Samplers

Karthik Raviprakash,<sup>1</sup> Mandar Kulkarni,<sup>1</sup> Xi Chen,<sup>1</sup>  
Sebastian Hoyos,<sup>1</sup> and Brian M. Sadler<sup>2</sup>

<sup>1</sup> Analog and Mixed Signal Center (AMSC), Department of Electrical and Computer Engineering,  
Texas A&M University, College Station, TX 77843, USA

<sup>2</sup> Army Research Laboratory, AMSRD-ARL-CI-NT, Adelphi, MD 20783, USA

Correspondence should be addressed to Sebastian Hoyos, hoyos@ece.tamu.edu

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A novel technique to reduce die area on a discrete-time sinc<sup>2</sup> filter for charge sampling is proposed. An SNR comparison of the conventional and the proposed topology reveals that the new technique saves 25% die area occupied by the sampling capacitors of the filter. The idea is also extended to implement higher downsampling factors, and greater percentage of area is saved as the downsampling factor is increased. The proposed filter also has the topological advantage over previously reported works of allowing the designers to use active integration to charge the capacitance, which is critical in obtaining high linearity.

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## 1. Introduction

THE need for integration of multiple wireless standards on a single handset calls for the development of a flexible receiver architecture, more popularly known as Software Defined Radio (SDR). Mitola [1] defined the SDR as a receiver that digitizes all the channels that are incident on the antenna so that all the radio functions can be programmed in a digital signal processor. Although very idealistic in principle, the SDR concept has led to numerous advances in CMOS transceiver design. Key building blocks in the design of this new generation of SDR receivers are the antialiasing filter and ADC. The choice of the antialiasing filter plays a fundamental role in the requirements on the ADC. For instance, in [2] the channel of interest has to be down-converted to zero IF and an antialiasing filter is required before baseband voltage sampling in order to isolate the wanted channel from a multitude of unwanted channels. Taking into consideration the bandwidths and blocker profiles of different standards, it is difficult to reconfigure an analog antialiasing filter to meet the wide range of requirements. The inherent sinc antialiasing filtering

provided by the windowed integration operation in charge sampling takes advantage of the frequency response nulls to eliminated unwanted interference. References [3–5] are other examples of receivers using charge sampling techniques.

The initial sampling rate for the windowed integration sampler is determined by the stop-band attenuation required for antialiasing and it can be much higher than the Nyquist rate for the input signal. To reduce the sampling rate to the Nyquist rate or the oversampled rate depending on the ADC architecture, downsampling operation has to be performed. After downsampling, the spectrum folds back again with the new sampling frequency equaling the sampling rate divided by the downsampling factor. The antialiasing specification now needs to be met at the multiples of this new sampling frequency. A simple approach is to create a sinc downsampling filter, which can be achieved by just summing up previous samples on capacitors and reading them out simultaneously. However, the attenuation provided by sinc downsampling might not be sufficient and better filtering is necessary. By weighting previous samples with appropriate factors prior to summing up operation, sinc<sup>2</sup> and sinc<sup>3</sup> downsampling filters can be created [2, 3]. These

filters provide much deeper and wider nulls at the sampling frequency but require a large number of switches and capacitors. In multi-standard applications, many filters may be needed to select the channels of interest. Optimizing the filters area becomes critical in lowering the production cost.

In this paper, a novel topology for the implementation of a  $\text{sinc}^2$  filter with a downsampling factor of two is proposed and compared to the conventional topology adopted in [2, 3]. The proposed topology requires less number of switches and capacitors. To get the same SNR performance, the proposed topology requires 25% less die area for the sampling capacitors. The proposed topology also allows for the implementation of the filter using an active-integrator based sampler, which is difficult in previously proposed topologies. This has the advantage of improved overall linearity and insensitivity to output impedance of the Gm-stage.

The organization of the paper is as follows. The theory of discrete-time downsampling filters and its implementation with conventional topology is explained in Section 2. The proposed filter is introduced in Section 3 and it is compared with the conventional topology. In Section 4, the extension of the proposed filter to get higher downsampling factor is explained. In Section 5, the circuit level simulations of both the topologies are illustrated and the results are compared. The conclusions are provided in Section 6.

## 2. Discrete-Time Downsampling Filters for Charge Sampling

*2.1. Theory of Discrete-Time Downsampling Filters.* Windowed integration of current signal on a capacitor  $C$  for a time  $\Delta t$ , reading out the charge, and discharging the capacitor after each readout is equivalent to sinc filtering the signal and sampling it at  $T_s = \Delta t$ . A narrowband signal centered at DC, surrounded by unwanted signals, when sampled at  $f_s = 1/\Delta t$ , the unwanted signals around  $f = n f_s$ ,  $n = 1, 2, 3, \dots$  gets aliased to the signal of interest. This is taken care of in windowed integration by the nulls which occur at multiples of  $f = 1/\Delta t$  due to sinc filtering. These nulls however offer limited attenuation as the interference bandwidth increases. The attenuation  $\alpha$  due to sinc filtering, for a bandwidth  $B$  at  $N$ th null is given by [2]

$$\alpha = \frac{B}{2N f_s}, \quad \text{where } f_s \text{ is the sampling rate.} \quad (1)$$

In order to meet the attenuation specification for a particular standard, the sampling frequency needs to be very high. Since the design of the ADC would pose extremely challenging specifications at such a high frequency, the sampled signal need to be down-sampled before digitization.

Downsampling causes spectral folding that in turn results in aliasing. The sampled signals which are now stored as charges on capacitors can be down-sampled by adding the current charge-sample with  $(N - 1)$  previous samples (Figure 1). This operation gives rise to a moving sum FIR filter that takes care of aliasing, followed by  $\downarrow N$  operation.

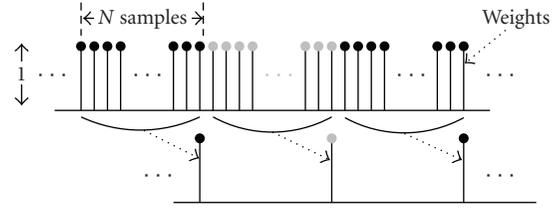


FIGURE 1: Moving sum FIR filter,  $H(z) + \downarrow N$ .

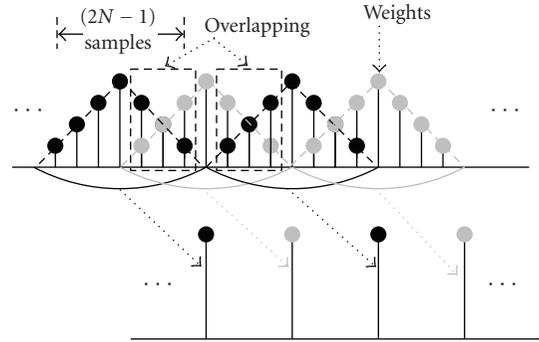


FIGURE 2: Triangular windowing +  $\downarrow 4$ . [2].

Equation (2) shows the  $z$ -domain transfer function and the magnitude response of the filter, respectively,

$$H(z) = \sum_{i=0}^{N-1} z^{-i} \quad (2)$$

$$H(f) = \frac{\sin(N\pi f/f_s)}{\sin(\pi f/f_s)}.$$

$H(f)$  has nulls at  $m(fs/N)$ , where  $m$  varies from 1 to  $(N - 1)$ . The attenuation provided by such a filter may not be sufficient for many applications and there is a need for a better filter. Instead of rectangular windowing, if triangular windowing is applied, the following results are obtained for the transfer function of the filter and frequency response, respectively:

$$H(z) = 1 + 2z^{-1} + \dots + Nz^{-(N-1)} + \dots + 2z^{-(2N-3)} + z^{-(2N-2)}, \quad (3)$$

$$H(f) = \left( \frac{\sin(N\pi f/f_s)}{\sin(\pi f/f_s)} \right)^2.$$

The magnitude response is the square of that obtained for moving sum. This gives rise to a better null attenuation compared to the previous case. The disadvantage is that  $(2N - 1)$  samples are needed to obtain  $\downarrow N$ . Unlike rectangular windows, triangular windows have to overlap in order to give the required performance, making the implementation complex. Triangular windowing for  $\downarrow 4$  is explained in Figure 2.

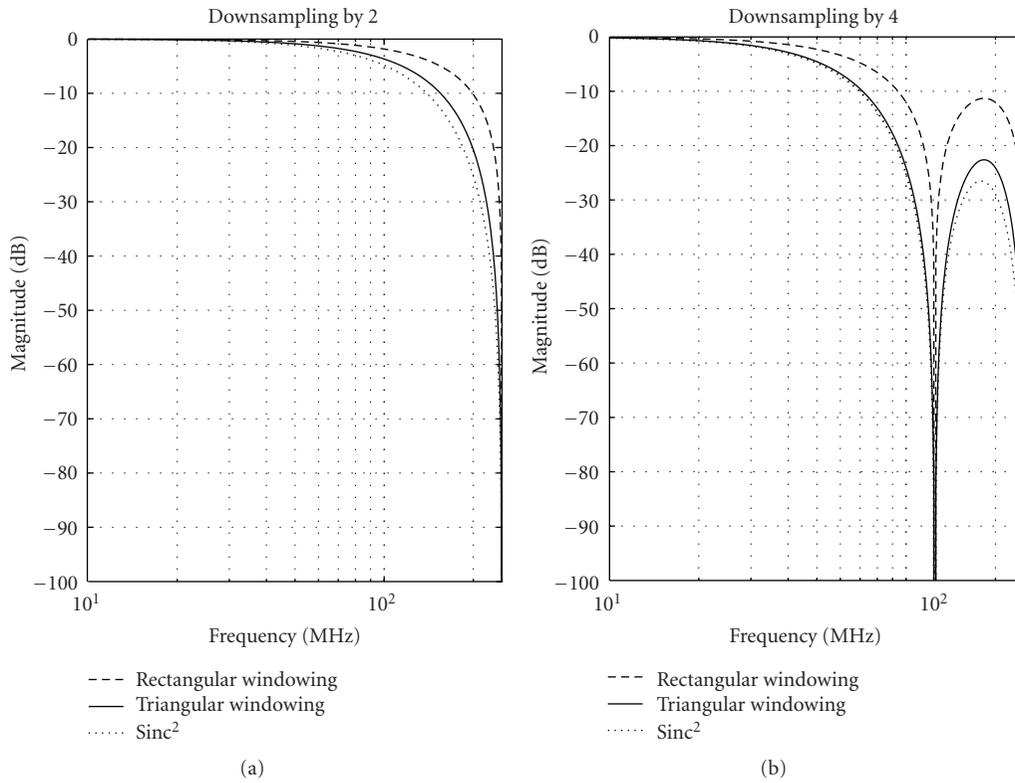


FIGURE 3: Comparison of frequency response of discrete time rectangular windowing, discrete time triangular windowing and sinc<sup>2</sup> for 12 and 14.

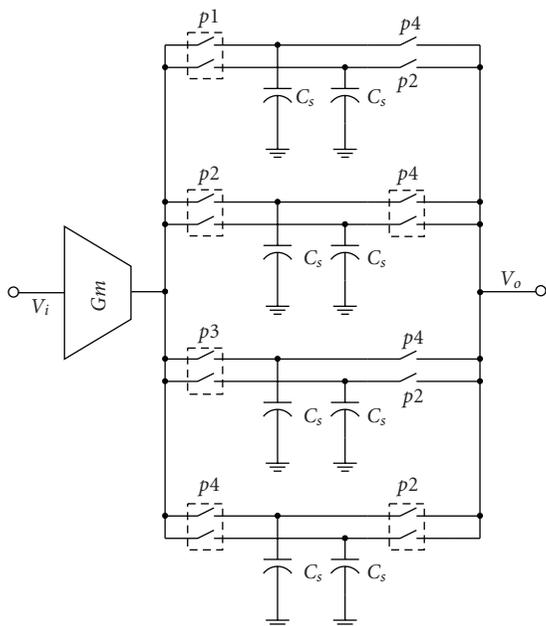


FIGURE 4: Conventional topology for sinc<sup>2</sup> 12 filter [2, 3].

2.2. A Note on Frequency Response. In some work [2, 3], discrete time triangular windowing is described as sinc<sup>2</sup> filtering. This is often misleading as the response is  $(\sin(N\pi f/fs)/\sin(\pi f/fs))^2$  and not  $(\sin(N\pi f/fs)/(\pi f/fs))^2$ . For  $N = 2$ ,

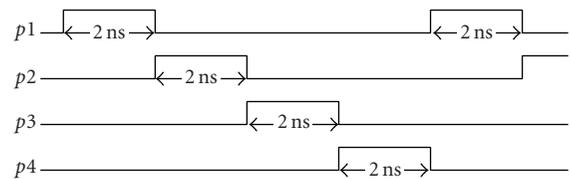


FIGURE 5: Clock scheme for the topology.

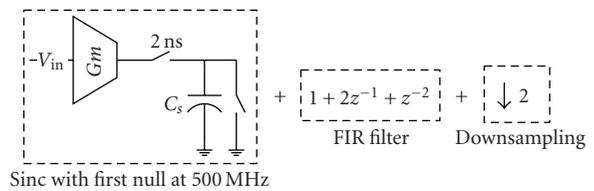


FIGURE 6: Step by step explanation for conventional sinc<sup>2</sup> 12 filters.

it is  $(\sin(2\pi f/fs)/\sin(\pi f/fs))^2 = 4\cos^2(\pi f/fs)$  and not  $\text{sinc}^2(2\pi f/fs)$ . Thus, it is more appropriate to call the filter  $\cos^2$  than  $\text{sinc}^2$ . For a sampling frequency of 500 MHz, Figure 3 compares the frequency response of discrete time rectangular windowing, discrete time triangular windowing and sinc<sup>2</sup> for 12 and 14 up to  $fs/2$ . It should be noted that triangular windowing has better null attenuation compared

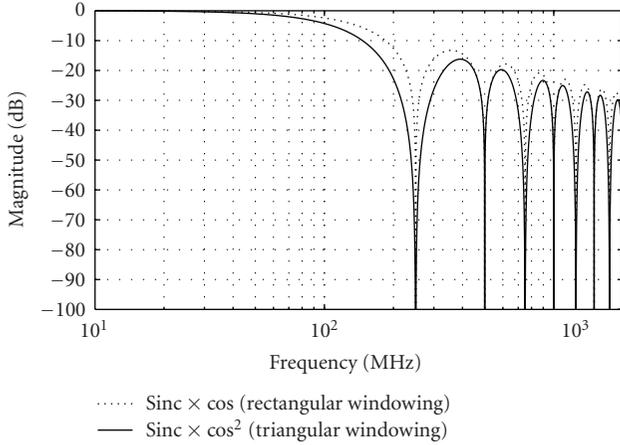


FIGURE 7: Comparison of Magnitude response of Rectangular and Triangular windowing. When decimated by 2, the components at 250 MHz, 750 MHz aliases to DC.

to rectangular windowing. As triangular windowing approximately follows  $\text{sinc}^2$  until  $f_s/2$ , such filters can be called as  $\text{sinc}^2$  filters.

**2.3.  $\text{Sinc}^2$  1/2 Downsampling Filter: Conventional Topology.** The conventional topology of downsampling filter [2, 3] is shown in Figure 4. Figure 5 shows its clock scheme. The capacitor discharge switches are not shown for simplification. The sampling rate at the output is chosen to be 250 MHz.

The signal current is integrated for a time window of 2 ns on each capacitor pair. The signal charge, integrated in phase  $p1$  and  $p3$  on a single unit capacitor  $C_s$ , and on two unit capacitors during  $p2$  is read out during phase  $p4$ . Similarly, the charge during  $p3$ ,  $p4$  and  $p1$  is read out during  $p2$ . A total of four capacitors are connected together and readout simultaneously during each sampling phase. As the signal is sampled already, the filter function can be written in  $Z$ -domain as

$$H(z) = \left(\frac{1}{4}\right)(1 + 2z^{-1} + z^{-2}). \quad (4)$$

The factor 1/4 comes from the fact that four unit capacitors are connected together during readout. The integration for 2 ns will create a sinc filter with first null at 500 MHz. The filter magnitude response for  $H(z)$  is  $\cos^2(\pi f \Delta t)$  where  $\Delta t = 2$  ns which will have two zeros at  $f_s/2$ .

The operation of the filter is explained in Figure 6. The overall filter response will be a cascade of the two filter responses mentioned before and is plotted in Figure 7. The wider nulls at 250 MHz, 750 MHz and so on, are due to the  $\text{cos}^2$  filter magnitude response as explained before.

### 3. Proposed Topology

**3.1. Operation of the Filter.** The proposed topology for the downsampling filter is shown in Figure 8 along with the clock

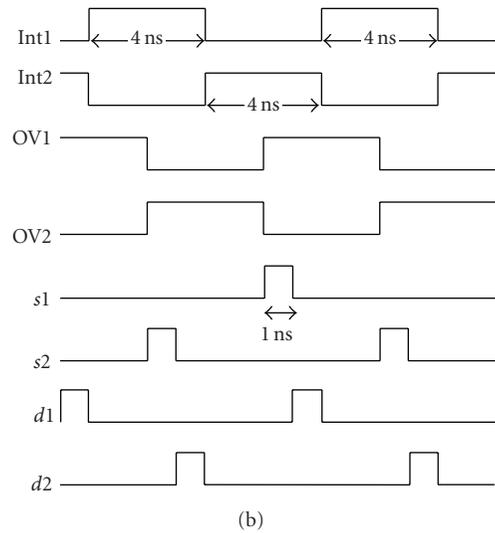
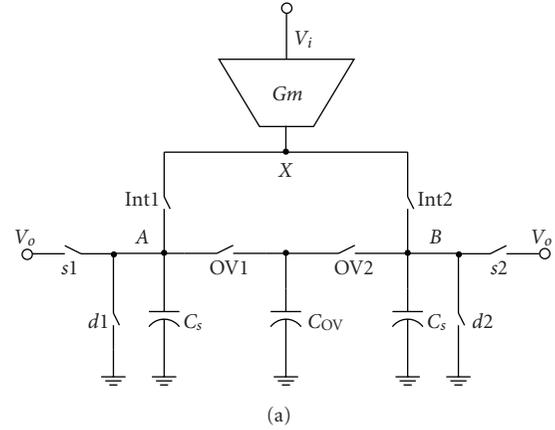


FIGURE 8: (a) Novel topology for the implementation of Overlap. (b) Clock scheme for the topology.

diagram. An extra overlap capacitor,  $C_{ov}$  is added along with the sampling capacitors  $C_s$ . The size of the overlap capacitor is equal to that of the sampling capacitor. The operation of the filter is as follows. During first 2 ns, the current is integrated on  $C_s$  and  $C_{ov}$ . For the next 2 ns, the overlap capacitor is disconnected while the sampling capacitor continues to integrate the charge. As the capacitance seen by the transconductor is now half the value compared to first 2 ns, the voltage gain is now doubled. In the meantime,  $C_{ov}$  is connected to the other sampling capacitor for readout and discharge. The same process is carried out on the other sampling capacitor and the overlap capacitor reconnects to the first sampling capacitor for readout. Switches  $d1$  and  $d2$  discharge the sampling capacitors after readout through switches  $s1$  and  $s2$ .

Effectively, the integration window in steady state looks like a stepwise approximation of a triangular window as shown in Figure 9. The filter response of such a window can be easily plotted and it is a very good match with the response of the conventional filter shown in Figure 7.

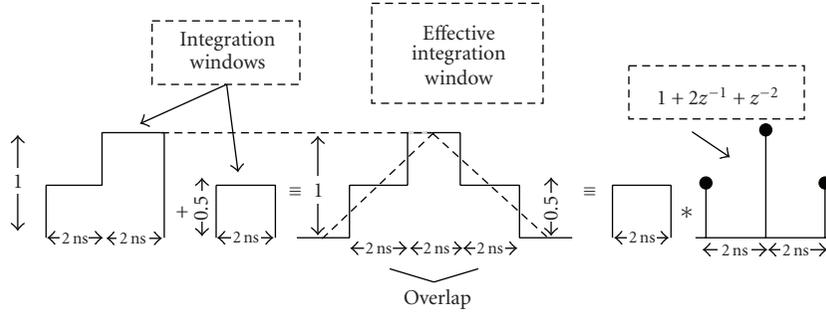


FIGURE 9: Effective Integration window for the proposed filter and its correspondence to the required function.

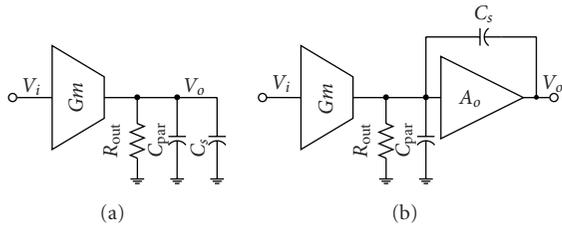


FIGURE 10: (a) Basic passive integrator. (b) Active integrator.

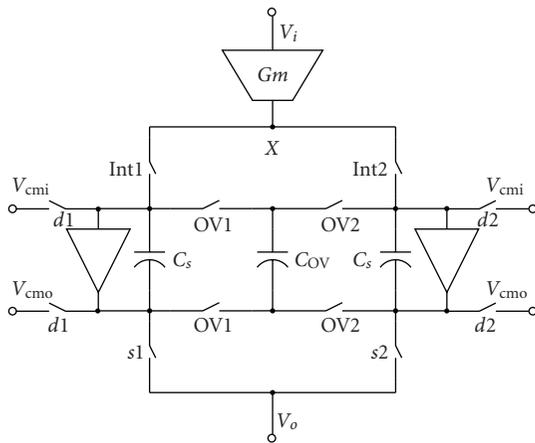


FIGURE 11: Sinc<sup>2</sup> 12 filter implemented with active integrator. Clock scheme is shown in Figure 8(b).

### 3.2. Comparison of Performance of the Two Filters

3.2.1. Area Savings. For both filter topologies, the size of the unit sampling capacitor is determined by the noise requirements at the output. For the same peak to peak voltage range and the same SNR specification, the relation between the sampling capacitor size and transconductance value of the topologies can be determined.

The total integrated noise of the windowed integration sampling circuit is given by [6]

$$N = \frac{KT * 2Gm\Delta t}{C_s^2}, \quad (5)$$

where  $\Delta t$  is the integration window duration. This expression holds under the condition that  $\Delta t \ll C_s \cdot r_{out}$ , where

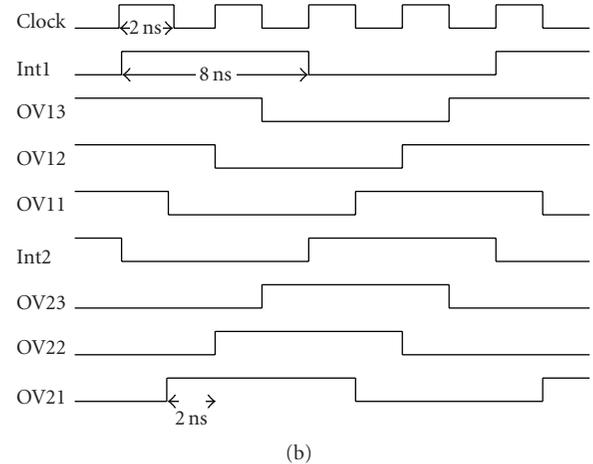
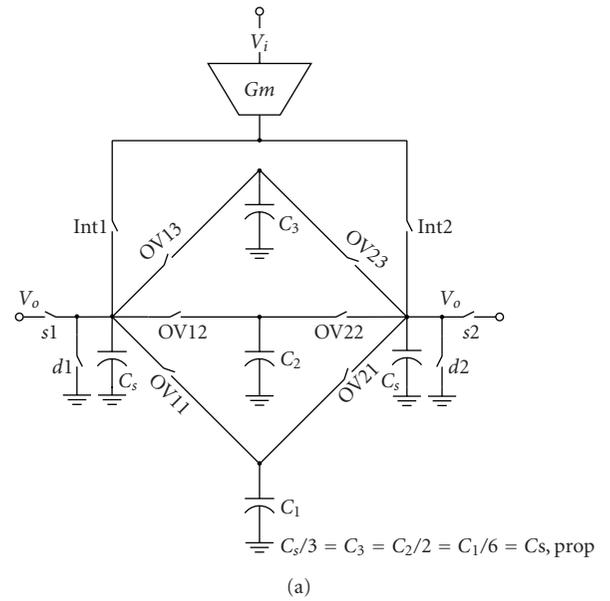


FIGURE 12: (a) Sinc<sup>2</sup> 14 filter. (b) Clock Scheme.

$r_{out}$  is the output impedance of the transconductor. In the expression for channel noise of MOS device,  $\overline{i_n^2} = 4KT\gamma gm$  used in (5),  $\gamma$  is assumed to be 1 for simplicity. The gain of the sampling circuit is given as  $G = Gm\Delta t/C_s$ .

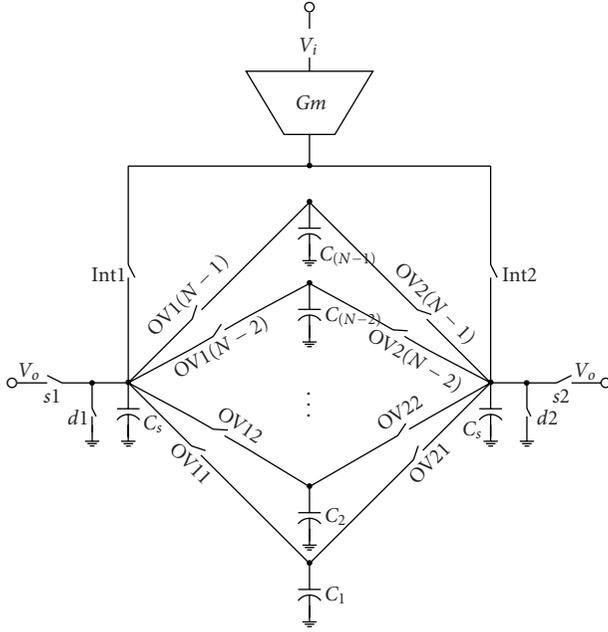
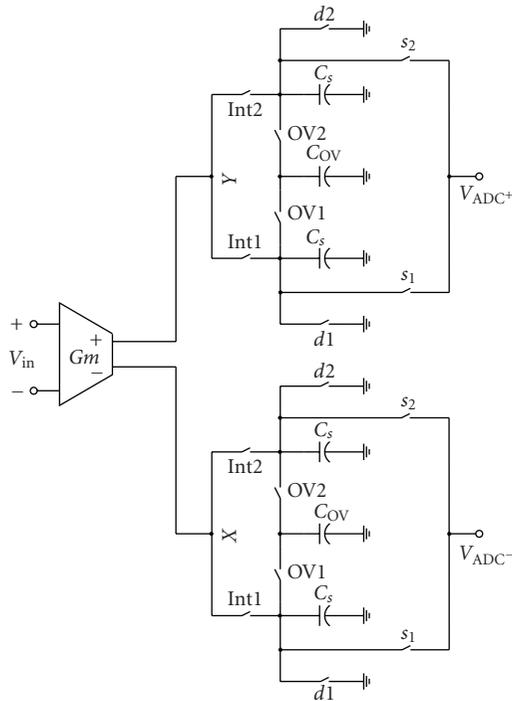
FIGURE 13:  $\text{Sinc}^2$  1N filter.

FIGURE 14: Differential Implementation of the filter.

$G_{m_{\text{conv}}}$  and  $C_{s_{\text{conv}}}$  denote the transconductance and sampling capacitor values of the conventional topology and  $G_{m_{\text{prop}}}$  and  $C_{s_{\text{prop}}}$  for the proposed topology, respectively.

To get the same SNR, the signal gain and overall noise of both the samplers should be the same. If the noise is reduced by increasing the capacitance, then  $G_m$  needs to be increased proportionally to keep the gain and hence the output peak

to peak range constant. From the noise expression, it can be seen that, integrated output noise is inversely proportional to square of the sampling capacitor and proportional to  $G_m$ . Therefore, the total noise reduces and overall SNR increases.

In the conventional topology, three windows of 2 ns are added together with a scaling factor of 1/4 due to charge sharing. It can be seen that only half of the current is integrated on each sampling capacitor. This means that the effective transconductance for each capacitor will be half of the actual value, that is,  $G_{m_{\text{conv}}}/2$ :

$$G_{\text{conv}} = \frac{1}{4} \left( \frac{G_{m_{\text{conv}}}\Delta t}{2C_{s_{\text{conv}}}} + \frac{2G_{m_{\text{conv}}}\Delta t}{2C_{s_{\text{conv}}}} + \frac{G_{m_{\text{conv}}}\Delta t}{2C_{s_{\text{conv}}}} \right) \quad (6)$$

$$= \frac{1}{2} \left( \frac{G_{m_{\text{conv}}}\Delta t}{C_{s_{\text{conv}}}} \right).$$

In case of our proposed topology, the signal integrates on  $2C_{s_{\text{prop}}}$  for the first 2 ns, then integrates on  $C_{s_{\text{prop}}}$  for the next 2 ns and finally again integrates on  $2C_{s_{\text{prop}}}$  for the last 2 ns. A factor of 1/2 is introduced during the readout operation. Therefore,

$$G_{\text{prop}} = \frac{1}{2} \left( \frac{G_{m_{\text{prop}}}\Delta t}{2C_{s_{\text{prop}}}} + \frac{G_{m_{\text{prop}}}\Delta t}{C_{s_{\text{prop}}}} + \frac{G_{m_{\text{prop}}}\Delta t}{2C_{s_{\text{prop}}}} \right) \quad (7)$$

$$= \left( \frac{G_{m_{\text{prop}}}\Delta t}{C_{s_{\text{prop}}}} \right).$$

Equating (6) and (7) yields,

$$\frac{1}{2} \left( \frac{G_{m_{\text{conv}}}\Delta t}{C_{s_{\text{conv}}}} \right) = \left( \frac{G_{m_{\text{prop}}}\Delta t}{C_{s_{\text{prop}}}} \right). \quad (8)$$

Similarly the noise for each topology can be calculated as,

$$N_{\text{conv}} = \frac{2KT}{16} \left( \frac{G_{m_{\text{conv}}}\Delta t}{4C_{s_{\text{conv}}}^2} + \frac{G_{m_{\text{conv}}}\Delta t}{C_{s_{\text{conv}}}^2} + \frac{G_{m_{\text{conv}}}\Delta t}{4C_{s_{\text{conv}}}^2} \right) \quad (9)$$

$$= \frac{3KT}{16} \left( \frac{G_{m_{\text{conv}}}\Delta t}{C_{s_{\text{conv}}}^2} \right).$$

The factor of 16 here is the square of the gain 1/4.

$$N_{\text{prop}} = \frac{2KT}{4} \left( \frac{G_{m_{\text{prop}}}\Delta t}{4C_{s_{\text{prop}}}^2} + \frac{G_{m_{\text{prop}}}\Delta t}{C_{s_{\text{prop}}}^2} + \frac{G_{m_{\text{prop}}}\Delta t}{4C_{s_{\text{prop}}}^2} \right) \quad (10)$$

$$= \frac{3KT}{4} \left( \frac{G_{m_{\text{prop}}}\Delta t}{C_{s_{\text{prop}}}^2} \right).$$

The factor of 4 here is the square of the gain 1/2. Equating (9) and (10),

$$\left( \frac{G_{m_{\text{conv}}}\Delta t}{C_{s_{\text{conv}}}^2} \right) = 4 \left( \frac{G_{m_{\text{prop}}}\Delta t}{C_{s_{\text{prop}}}^2} \right). \quad (11)$$

Substituting (8) in (11),

$$C_{s_{\text{prop}}} = 2C_{s_{\text{conv}}}, \quad (12)$$

$$G_{m_{\text{prop}}} = G_{m_{\text{conv}}}.$$

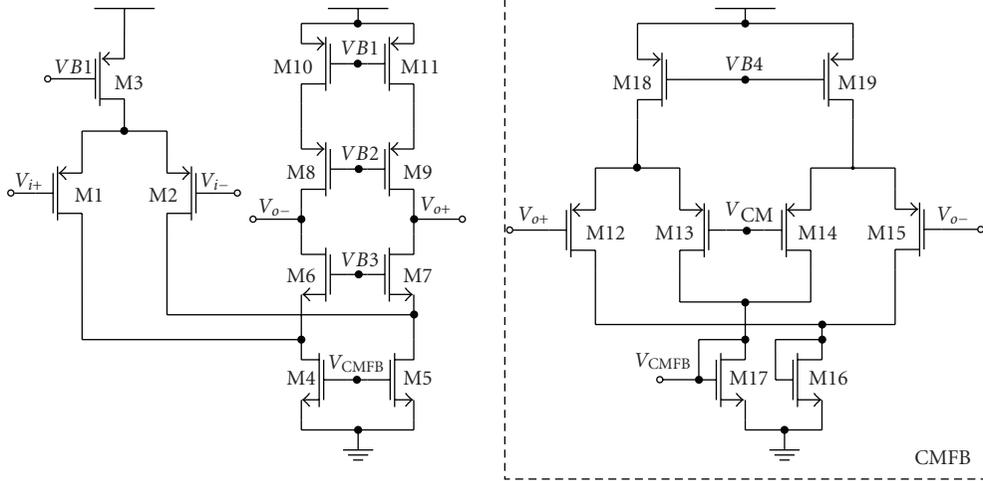


FIGURE 15:  $G_m$ -stage: Folded-Cascode Topology.

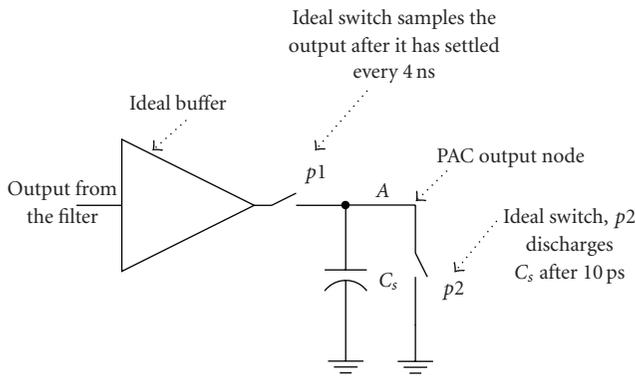


FIGURE 16: Setup for finding the transfer function of the filter using PAC analysis.

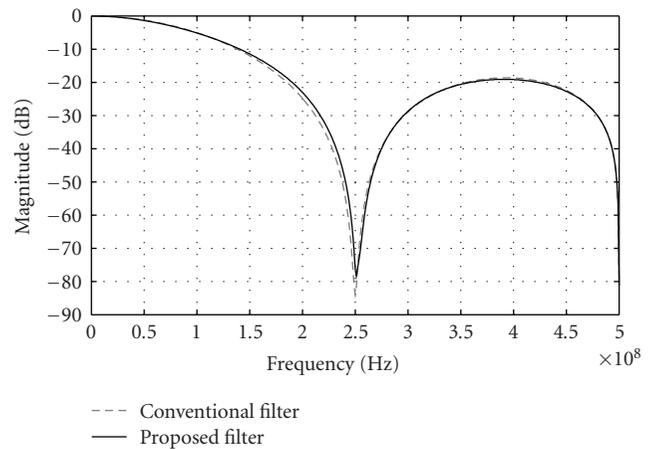


FIGURE 17: Magnitude Response of conventional and proposed filter using PAC analysis in Spectre.

The total area in the conventional filter is  $8C_{s,conv}$  (Figure 4), whereas it is only  $3C_{s,prop}$  (Figure 8) for the proposed filter. Therefore, 25% of the area from the dominant area consuming factor, the sampling capacitors, can be saved in the proposed filter when compared to the conventional filter.

**3.2.2. Benefit of Linearity in Proposed Topology.** The basic passive integrator consisting of just an integrator driving a capacitor has some certain disadvantages. In addition to sampling capacitor  $C_s$ , it has parasitic capacitance  $C_{par}$  (Figure 10(a)), which is the result of parasitic diodes, overlaps, crossings, strays and fringing effects [7]. The voltage dependence of the parasitic capacitance makes the response sensitive to power supply variations and degrades the distortion performance [7, 8]. Also, the finite output impedance of the  $G_m$  stage gets modulated by the swing of the voltage signal at its output. This creates nonlinearity in the overall performance.

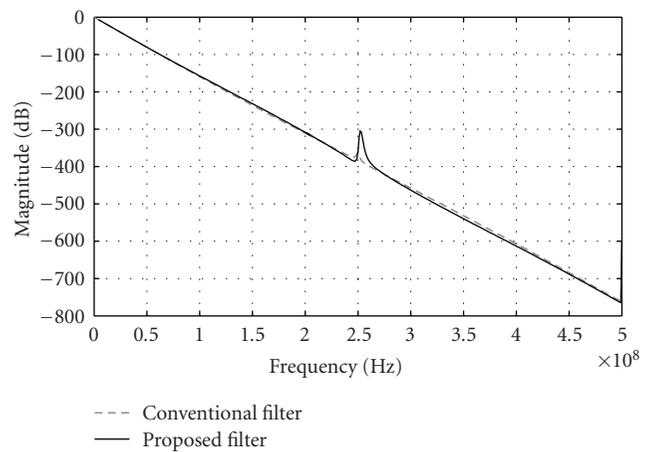


FIGURE 18: Phase Response of conventional and proposed filter using PAC analysis in Spectre.

TABLE 1: Specification of the transconductor.

Specification	Value
$Gm$	665.65 $\mu A/V$
$r_{out}$	818 K $\Omega$
Integrated Input Referred Noise (0–20 MHz)	18.36 nV <sup>2</sup>
Maximum Differential Input Signal (THD = 5% @ 20 MHz)	83.2094 mV
Excess Phase at 20 MHz	2°
Supply Voltage	1.2 V
Current Consumption	282 $\mu A$

TABLE 2: Summary of simulation results.

Specification	Conventional Filter	Proposed Filter
Null attenuation for 20 MHz	41.55 dB	38.26 dB
Integrated Output Noise (0–20 MHz)	25.02 nV <sup>2</sup>	25.66 nV <sup>2</sup>
THD (1mV sine, 20 MHz)	0.972%	0.972%
Overall Capacitor for sampling	8 pF	6 pF

The above mentioned problem can be dealt with by using an active integrator based sampler as shown in Figure 10(b) at the cost of power consumption and complexity.

For  $A_o \rightarrow \infty$ , the effect of  $C_{par}$  and  $R_{out}$  is neglected. The use of an active integrator can be well justified for use in the application discussed in this paper. Here the signal is at baseband where the above benefits can be obtained without spending so much power. In charge sampling circuits, usually a buffer is required before the ADC to drive low impedance. Here the OTA provides driving capability and hence the output can be read out directly at the sampling capacitor. Figure 11 shows the block diagram of  $\text{sinc}^2 \downarrow 2$  filter implemented with active integrator and Figure 8(b) shows its clock scheme. In Figure 11,  $V_{cmi}$  and  $V_{cmo}$  denote the input and output common voltages of the OTA used for active integration, respectively.

The benefits of active integration are obtained in the proposed topology only because the current is integrated at and read out from only two nodes. This is applicable for any order of decimation filter in the proposed topology. In the conventional topology, current is integrated and read out from multiple capacitors and depending on the order of decimation, it varies. This complicates the active integration implementation and increases power consumption.

#### 4. Extension of the Proposed Topology to Achieve a Higher Downsampling Factor

There are cases where it is needed to integrate and sample the signal at a very high frequency to achieve the required null attenuation. In such a case, it is necessary to down-sample by a higher factor. In this section, the implementation of  $\text{sinc}^2 \downarrow N$  filter using the proposed topology is discussed and compared with the conventional topology.

The conventional topology for the implementation of  $\text{sinc}^2 \downarrow N$  is just a straight forward extension of  $\text{sinc}^2 \downarrow 2$  (Figure 4). Figure 12 shows  $\text{sinc}^2 \downarrow 4$  filter and its clock scheme. The clock scheme of readout switches  $s1$  &  $s2$  and discharge switches  $d1$  &  $d2$  is not shown in the figure. The  $\text{sinc}^2 \downarrow N$  filter using the proposed topology is shown in Figure 13. Here the capacitors have to satisfy the following equations:

$$\begin{aligned}
 C_{N-1} &= C_{s,prop}, \\
 C_s &= (N-1)C_{s,prop}, \\
 C_{N-2} &= \frac{N(N-1)}{(N-1)(N-2)} C_{s,prop}, \\
 C_{N-3} &= \frac{N(N-1)}{(N-2)(N-3)} C_{s,prop}, \\
 &\vdots \\
 C_2 &= \frac{N(N-1)}{(2)(3)} C_{s,prop}, \\
 C_1 &= \frac{N(N-1)}{(1)(2)} C_{s,prop}.
 \end{aligned} \tag{13}$$

The proposed and the conventional topologies can be compared in the same way as done in Section 3, to obtain

$$\begin{aligned}
 G_{conv} &= \frac{1}{N} \left( \frac{Gm_{conv} \Delta t}{C_{s,conv}} \right), \\
 G_{prop} &= \frac{1}{(N-1)} \left( \frac{Gm_{prop} \Delta t}{C_{s,prop}} \right).
 \end{aligned} \tag{14}$$

Using (14),

$$\left( \frac{Gm_{conv}}{C_{s,conv}} \right) = \frac{N}{(N-1)} \left( \frac{Gm_{prop}}{C_{s,prop}} \right). \tag{15}$$

Proceeding in the same way as Section 3, from noise calculations, it can be shown that

$$\left( \frac{Gm_{conv}}{C_{s,conv}^2} \right) = \left( \frac{N}{N-1} \right)^2 \left( \frac{Gm_{prop}}{C_{s,prop}^2} \right). \tag{16}$$

Using (15) and (16),

$$\frac{C_{s,prop}}{C_{s,conv}} = \frac{N}{N-1}. \tag{17}$$

The total area required by the two filters is

$$\begin{aligned} A_{\text{conv}} &= 2N^2 C_{s,\text{conv}}, \\ A_{\text{prop}} &= (N^2 - 1) C_{s,\text{prop}}. \end{aligned} \quad (18)$$

Using (17) and (18),

$$\begin{aligned} \% \text{ of area savings} &= \frac{(A_{\text{conv}} - A_{\text{prop}})}{A_{\text{conv}}} \times 100\% \\ &= \frac{N - 1}{2N} \times 100\%. \end{aligned} \quad (19)$$

From (19), it can be noted that as the decimation factor is increased, the percentage of area saved compared to the conventional topology also increases. For large values of  $N$ , the area savings rapidly approaches 50%.

## 5. Results

Prototype filters of the conventional and proposed technique are simulated in 45 nm technology and the results are compared. A differential version of the filter is shown in Figure 14. A PMOS input fully differential folded cascode structure with active common mode feedback is used as Gm-stage (Figure 15). For a fair comparison, the same Gm-stage is used for both the topologies. The specification of the transconductor is given in Table 1. The transistors M1 and M2 have overdrive and threshold voltages of 80 mV and 0.4 V, respectively.

Ideally a transconductor with infinite output impedance is needed. Finite output impedance might limit either the null depth or null bandwidth [2]. If the signal is at DC with a bandwidth of  $\Delta f$ , depending on the requirement of attenuation of the aliasing signal, the value of  $r_{\text{out}}$  is chosen.

The Gain, Linearity and NF of the filter are mainly determined by the transconductor. In order to arrive at the required value of these parameters for the filter, various factors need to be considered. Some of them are

- (1) SNR requirement of the receiver for each standard under consideration,
- (2) Linearity Requirement of the receiver,
- (3) Gain, Noise Figure and Linearity Allocation to LNA and Mixer,
- (4) Blocker's profile.

The aim is to show that the proposed filter occupies less area on sampling capacitors when compared to the conventional filter. For a fair comparison in simulations, active integration is not used for proposed topology.

Channel Bandwidth and Blocker's profile determines the clock frequency. For example, in the analysis carried out in [9, Chapter 3], the initial sampling rates of the two extreme cases of bandwidths, GSM (200 KHz) and 802.11g (20 MHz) are taken to be 72 MHz and 480 MHz, respectively. Here, a sampling frequency of 500 MHz is assumed for comparison of the two topologies.

PAC analysis of Spectre is used to find the transfer function of the discrete-time filters. In discrete-time filters, the output is valid only at one instant of time every  $T_s$  (here 4 ns). For the remaining duration, the output is some random value. If PAC analysis is used directly at the output node to find the transfer function, the response obtained would not be accurate [10]. Reference [10] suggests sampling the output at the required instant and holding it for  $T_s = 4$  ns using ideal analog blocks in Spectre. This is a useful simulation technique for switched capacitor circuits where the frequency of interest,  $f \ll 1/T_s$ . In charge sampling circuits, in order to find the null performance, the frequency of interest also includes  $f = 1/T_s, 2/T_s$  and so on. As suggestion in [10], if the output is sampled and held for 4 ns, then it is equivalent to multiplying the response of the filter with a sinc filter having null at 250 MHz, which is the frequency where null of the discrete time filter occur. The two nulls get mixed up and cannot be differentiated. The solution is to sample the output at the required instant every 4 ns using ideal switches, discharge the output immediately (say, after 10 ps) and find PAC at this node. This is equivalent to multiplying the output with a sinc having null at 100 GHz ( $=1/10$  ps) and the response of the sinc is almost a straight line in the frequency of interest (0–250 MHz). The simulation setup is shown in Figure 16.

The Magnitude Responses of the proposed and conventional filter are shown in Figure 17, and their phase responses are shown in Figure 18.

Table 2 shows the summary of results. The filter responses are very nearly identical, with some small degradation in the null attenuation at 20 MHz.

## 6. Conclusion

A novel technique to implement a  $\text{sinc}^2$  filter has been proposed. Both the conventional and proposed filters have been simulated in 45 nm technology and the results are compared. The results show that the proposed filter gives the same performance as the conventional topology with 25% area savings on sampling capacitors, which dominates the area occupied by the filter. The proposed topology can also be extended to achieve  $\text{sinc}^2$  function with higher downsampling factor. The higher the downsampling factor, the greater is the area savings compared to conventional filter. The proposed filter topology has an additional benefit; it allows charging and reading the sampling capacitor in closed loop with an OTA. In a software defined radio, when linearity and area are of main concern, the usefulness of the proposed filter is evident.

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