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Review Article

"RF-SoC": Integration Trends of On-Chip CMOS Power Amplifier: Benefits of External PA versus Integrated PA for Portable Wireless Communications

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RFIC integration has seen dramatic progress since the early 1990s. For example, Si-based single-chip products for GSM, WLAN, Bluetooth, and DECT applications have become commercially available. However, RF power amplifiers (PAs) and switches tend to remain off-chip in the context of single-chip CMOS/BiCMOS transceiver ICs for handset applications. More recently, several WLAN/Bluetooth vendors have successfully integrated less demanding PAs onto the transceivers. This paper will focus on single-chip RF-system-on-a-chip (i.e., "RF-SoC") implementations that include a high-power PA. An analysis of all tradeoffs inherent to integrating higher power PAs is provided. The analysis includes the development cost, time-to-market, power efficiency, yield, reliability, and performance issues. Recent design trends on highly integrated CMOS WiFi transceivers in the literature will be briefly reviewed with emphasis on the RF-SoC product design tradeoffs impacted by the choice between integrated versus external PAs.

1. Introduction

In a manner analogous to Moore's law for digital ICs, it is expected that one can significantly reduce the cost and the form factor of communication products by progressive integration of the RF/analog system. However, the RF portion of many advanced communication systems remains a mixture of components based on different technologies and interface requirements. For example, compound semiconductors (primarily in group III-V) predominate for low-noise amplifiers (LNAs), switches and power amplifiers (PAs) in cellular phones. This prevents progressive integration towards a true single-chip radio. Historically, one might argue that this is partly because, prior to the late 1980's, most RF circuits were designed for military applications. By natural market evolution, the RF component industry has moved rapidly from the low-volume discrete RF circuitry to the high-volume low-cost, highly integrated commercial products. Moreover, this trend has encouraged circuit topologies that are friendlier to integration. For example, differential-type circuit topologies such as the Gilbert balanced mixers that suffer from device mismatch issues in discrete RF design, have become very popular for integrated RFICs. While GaAs-based devices can be inexpensive and highly efficient at GHz frequencies, they offer a limited ability to integrate with CMOS baseband chips. Fueled by the recent wireless Internet explosion, rapidly growing broadband communication markets are driving the development of reliable, high performance and economical RF integrated circuits and devices with low power dissipation. Deep-submicron RF-CMOS and heterojunction Si/SiGe bipolar transistors (HBTs) have extended the high-frequency limit of Si-based technology with cut-off frequencies f_T well above 300 GHz—a frequency range that has been historically dominated by GaAs-based devices. Moreover, RF-CMOS has become a viable low-cost option for implementing highly integrated RFIC products, especially for applications below 5 GHz. The reader should note here that the term "RF-CMOS" does *not* mean pure digital CMOS with analog modeling. Rather, it requires careful RF/analog device modeling—up to and beyond the RF carrier frequency. Extra masks and thick metals process options are required for high Q

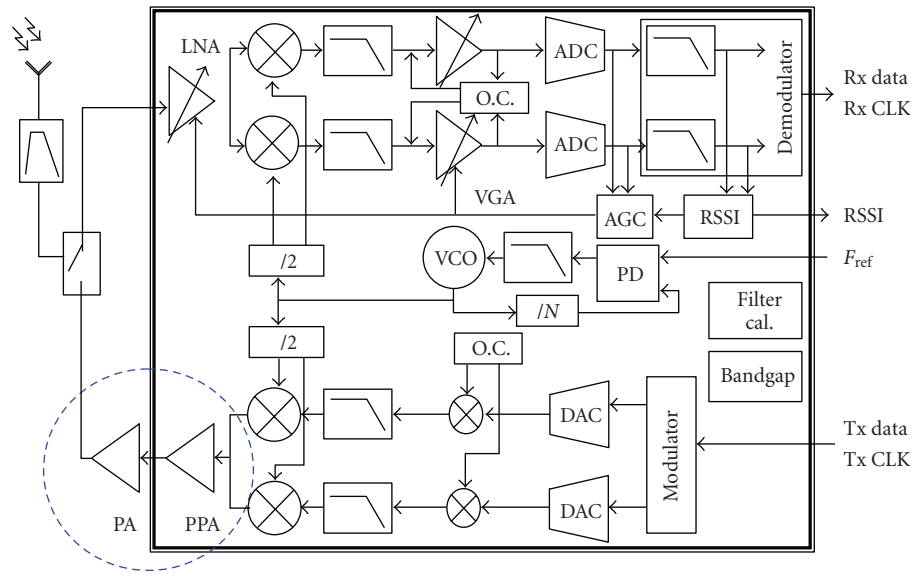

Figure 1: Block diagram of a single-chip direct-conversion BiCMOS DECT transceiver. Note that only the PA, antenna switch, some bypass capacitors, resistors, and filters are external to the chip. Adapted from Eynde et al. [1].

passives. In addition, deep N-well shielding for improved RF isolation and low switching-noise digital cell libraries are important technology improvements over "plain vanilla" CMOS processes.

RF-system-on-a-chip (i.e., "RF-SoC") means that the RF/analog/digital circuits are all integrated with memory blocks and microprocessors/DSP as a complex single-chip digital communication system. The primary advantage of a single-chip RF-SoC is that the component will be less susceptible to external noise pickup, have a smaller footprint, more simple assembly, and is likely to achieve lower system cost in the long run. Most experienced RFIC designers understand that the integration level of an RF circuit is highly determined by the selection of the radio architecture, the available device technology, on-chip crosstalk/isolation, package parasitics, cost, and time-to-market. Figure 1 shows the block diagram of a single-chip BiCMOS DECT transceiver as an example of an early RF-SoC product. Note that only the PA, antenna switch, some bypass capacitors, resistors, and filters are external to the chip. In view of the fact that most cellular phones today support multiband operation, a next target for integration may be the single-chip RF-SoC product that supports multiband, multistandard cellular standards (such as UMTS/GSM/EDGE/CDMA2000). Such a product may also feature capability for wireless personal-area-network (PAN) and wireless-local-area-network (WLAN). An idealized block diagram of this kind of system is shown in Figure 2. To achieve this high level of RFIC and system integration, one has to choose radio circuit architectures that require a minimal number of external components along with a careful selection of the IC technology and SoC design. Notwithstanding, the RF PA and switches are still not integrated into cellular CMOS/BiCMOS transceiver ICs. In sharp contrast, several vendors of WLAN/Bluetooth radios have integrated PAs onto the transceiver. It is a natural question to ask if this development represents a "first wave" for integrated PAs within portable wireless communication products. What are the benefits of an external PA versus integrated PA solutions? These important questions will be addressed in the paper following a brief discussion of some recent integration trends for WiFi products. Counter intuitively perhaps, it may be wiser *not* to integrate a CMOS PA onto the same transceiver IC in some situations.

2. RF-SoC: Pros and Cons of CMOS PA Integration

2.1. On-Chip PA Basics: GaAs versus Si/SiGe PAs. PAs are one of the most difficult RF components to be integrated on-chip for RF-SoC products. Some older cellular standards used a constant envelope modulation technique that allows the use of nonlinear PAs for higher efficiency. More recently, 3 G standards such as UMTS employ QPSK modulation for better spectral efficiency but resulting in envelope variations that require a linear PA. Maximizing the efficiency of a PA with high power and linearity, concurrent with robustness, is very challenging, especially if one also needs to integrate the PA on-chip. A simple example might be found by examining efficiency. The power-added-efficiency (PAE) of an amplifier is simply defined as

$$\text{PAE} = \eta \cdot \left(1 - \frac{1}{G}\right), \tag{1}$$

where $\eta \equiv P_{\text{RF,out}}/P_{\text{DC,in}}$ is the collector efficiency and G is the power gain [2]. According to (1), the PA gain maximization is needed to achieve good PAE. Devices based on III-V technology may be preferred for PA design because the high-frequency transistor gain (at a given current density) is superior to Si-based devices. Moreover, breakdown voltages tend to be higher in GaAs-based devices featuring a

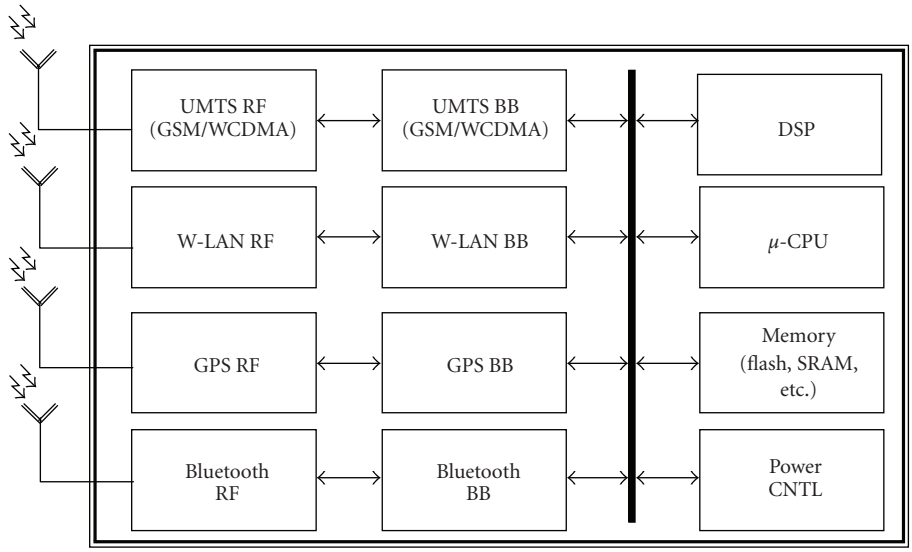

Figure 2: A schematic block diagram showing a future multistandard, multiband cellular RFIC product as a RF-SoC complex single-chip digital communication system. Note that the PA and switches are off-chip.

larger bandgap. Alternatively, assuming a comparable high-frequency transistor was available based on Si, one might argue that because the thermal conductivity of the silicon substrate is about three times higher than that of GaAs, Si should be the preferred substrate material for PA applications [3]. However, both GaAs and Si-based integrated PAs must all meet stringent specifications on gain, output power, PAE, linearity, and reliability. They also face a massive challenge in the face of the continual decrease in the power supply voltage. Notwithstanding, improved $f_T/f_{\max}$ of Si/SiGe HBTs and deep-submicron CMOS devices have resulted in some impressive Si-based PAs as reported in the literature. Recent device load-pull data using IS-95 modulation at $P_{\text{OUT}} = 28$ dBm (at the same ACPR performance), shows that the PAE and gain of the GaAs PAs outperform Si BJT and SiGe BJT PAs. This advantage of GaAs PAs is more pronounced at higher frequencies [4, 5]. When measured at 836.5 MHz, the PAE of GaAs PAs is only ~2% higher than that of Si BJT PAs; however, at 1800 MHz, the PAE of GaAs PAs can be ~4–10% higher than those of Si or SiGe BJT PAs [4, 5]. Since a high efficiency PA is one of the keys for longer operating time and reduced thermal stress in portable wireless products, extensive research efforts are required to prove that it makes sense to integrate PAs on-chip. Some of these efforts will be surveyed below.

2.2. Recent Trend of Integrated CMOS PAs. As discussed previously, integrating CMOS PAs on-chip has become attractive because it has the potential to provide lower cost and benefit with progressive technology scaling and concurrently improved $f_T/f_{\max}$. However, it is now well-established that the CMOS PA figures of merit (PAE, output power, etc.) do *not* improve with scaling [6]. For example, as the gate length and effective oxide thickness of a CMOS device decreases, its breakdown voltage also decreases and therefore the operating supply voltage V_{dd} needs to be reduced. Unfortunately, the output power P_{out} would decrease accordingly, and the peak PAE also degrades. Using unit cells connected in parallel can achieve higher P_{out} (power combining) but only up to a point (given layout parasitics, etc.) In addition, as CMOS device width increases to deliver more power, the $f_{\max}$ and f_t decrease such that the power gain is degraded. In effect, output power does not increase as much as one would like to see with wider devices. Increasing V_{dd} for the CMOS device can deliver more power, but it may cause significantly degraded device and circuit reliability [6]. Generally speaking, the peak PAE of a CMOS device also decreases as the operating frequency gets closer to $f_{\max}$, making it a difficult tradeoff between power and PAE in 5-6 GHz applications. Therefore, practical on-chip CMOS PA design often uses thick-oxide or dual oxide I/O CMOS devices, which underscores the hypothesis that integrated CMOS power transistor does *not* benefit in any real sense from Moore's Law. Recently, several new companies have worked on external stand-alone CMOS PA solutions, and one clear industry leader with qualified GSM external CMOS PA products using active transformer coupling structures (Axiom Inc.) has been sold to Skyworks in 2009. To date, no company has shipped integrated CMOS PAs for 1W^+ handset applications [4–7].

Can the performance of integrated CMOS PA be good enough for some other non-handset wireless applications? For example, is an integrated CMOS PA suitable for medium power (i.e., <20 dBm), low-RF frequency (i.e., sub-6 GHz), consumer products that are low-cost and high-volume? Currently, integrated CMOS PAs have been reported in WLAN SoC, Bluetooth SoC, and even a handset SoC as a *PA driver*. For example, Broadcom has reported a SoC 802.11b transceiver with integrated CMOS PA in 0.18 μm CMOS in 2005 [8]. In that work, the transmitter has an adjustable output-power range up to 20 dB in 0.5 dB steps,

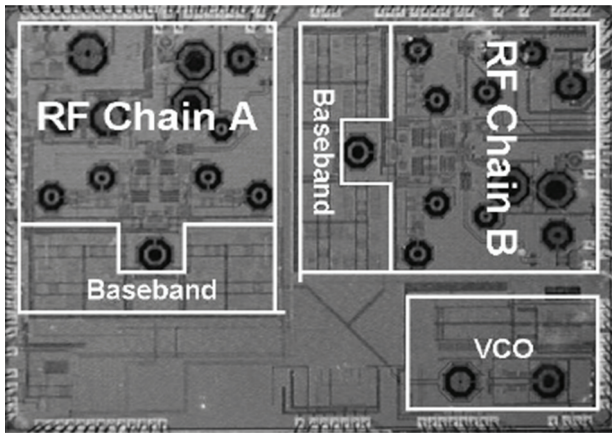

Figure 3: The die micrograph of a state-of-the-art 1 × 2 MIMO multiband CMOS transceiver with an integrated front-end in 90 nm CMOS for 802.11 a/g/n WLAN applications [10]. No switches are integrated and the output power is ∼3-4 dB lower than the external SiGe PAs currently available commercially. After Degani et al. [10].

and achieves a $P_{1\,\mathrm{dB}}$ of ∼18 dBm. The PA gain variation due to the process and temperature variations can be controlled within ∼1 dB by estimating the output power through an integrated transmit signal strength indicator (TSSI) and adjusting the preamplifier gain. To avoid PA pulling issues, a clock generator is exploited to produce a clock frequency at 2.4 GHz from the 1.6 GHz VCO. The channel selection is performed by an integer-N frequency synthesizer with an integrated loop filter. The resulting SoC delivers P_{out} = 13.1 dBm that passed the 802.11b TX mask with 24% EVM. That output power, though, does not compare favorably to the commercially available external SiGe 802.11b PA (i.e., 19.5 dBm) [7, 9]. In fact, the 24% EVM reported for that work is also much worse than what is typically offered by external GaAs or SiGe commercial PAs (∼3%). In addition, even though this 2005 paper did not disclose its PAE value, it is expected to be significantly lower than the 19% achieved by external SiGe PAs.

Recently, INTEL has reported a 1 × 2 MIMO multiband CMOS transceiver with an integrated front-end in 90 nm CMOS for 802.11 a/g/n WLAN applications [10]. This impressive work presents preliminary results of a radio IC design, which integrates the LNAs and PAs (and their matching networks) in a 1 × 2 scheme for 802.11 a/g/n protocols. The fully integrated class-AB CMOS PAs (operating from a 3.3 V supply) use a thin-oxide common-source device and a thick-oxide common-gate device, in a quasi-differential cascode topology to improve the RF performance and reliability. The 1 dB saturated output power of the 2.5 GHz and 5-to-6 GHz PAs are 25 dBm and 23-24 dBm, respectively, and their measured peak PAE is 50% and 30%, respectively. The better PAE at 2.5 GHz is probably due to the better gain of the NMOS devices at lower frequencies. To improve the EVM with the nonlinear Class-AB PA, a digital predistortion (DPD) algorithm is implemented, which uses a dynamic OFDM signal (but not static characteristics) for the calibration. Accelerated aging tests and thermal mappings of the PAs suggest that the PA can withstand extreme operation conditions and still maintain gain and power levels within the specifications. In preliminary 802.11n characterizations, the chip has achieved 47/90 Mbps (TX/RX) TPT in 20 MHz channel. The chip is housed in a QFN package and the die size is 15.5 mm^2. An EVM of −28 dB was achieved for an output power of 15.5 dBm (19% PA PAE) and 14.5 dBm (12% PA PAE) for the 2.5 GHz and 5-to-6 GHz bands, respectively. This report shows very promising results for integrated CMOS PAs with excellent PAE and EVM numbers. However, the output power is still ∼3-4 dB lower than the external 802.11a/b/g SiGe PAs that are available commercially [7]. Moreover, the front-end switches and filters that are required for 802.11a/b/g multiband operation in commercially available front-end modules housing external PAs are still not integrated on-chip (cf. Figure 3). A central thrust of this work is the application of the "digital dividend". That is, the application of signal processing in the digital domain prior to signal generation in the analog domain. CMOS at the nanometer node can provide this processing capability with ease.

Another subsequent paper from INTEL reported a fully integrated transmit chain for 802.11a band with on-chip PA and on-chip balun matching network in 45 nm standard digital CMOS process in 2009 [11]. This work demonstrates 1 dB saturated power of +23 dBm. The average efficiency is +5% and peak efficiency is +15%. A standalone class AB CMOS PA with on-chip BALUN matching network was also fabricated for detailed characterization data and compared with the fully-integrated TX data. Note that on-wafer probing was used for measurements so the actual packaged device measurement data is expected to be worse than reported numbers. Two sets of measurements were done: one for the full TX chain and the second set for the stand-alone PA. Using digital predistortion, an EVM of −28 dB is achieved at 19 dBm for 5 GHz band and 2.5 GHz band for standalone PA. However, the EVM and the mask compliance degrade in the full TX chain as compared to the stand-alone PA measurements. Also, the TX chain consists of three RF gain stages and achieves a total of 24 dB of voltage gain across the 5-6 GHz band. In fact, in order to get ∼15 dBm of average power for WiFi operation, this gain is not enough for all the process corners and further simulation and measurements suggest the need for an additional RF gain stage to get the output power up. Lower output power is a challenging issue for on-chip CMOS PAs and the authors concede that more experiments are needed to better understand the feasibility of 45 nm technology for on-chip PAs for WiFi 802.11a TX design. One can see that the problems associated with single-chip 802.11a/b/g/n CMOS transceiver design with integrated multi-mode, multiband CMOS PAs using the 45 nm node CMOS would be considerably more challenging to overcome than a single band 802.11a TX product. In addition, it will be even tougher to further integrate high performance CMOS switches (such as a SP3T) on-chip with the CMOS PA and the transceiver on the same die. Therefore, at this point the literature argues against integrating sub-45 nm CMOS PAs in the transceivers for multimode multiband WiFi products.

Further reasonings and discussions are provided in the following section.

2.3. Benefits of External PA versus Integrated CMOS PA. Arguably, external GaAs-based PAs will still dominate the handset $1W^+$ PA markets. In addition to the superior high-frequency GaAs device performance, this dominance is at least partly due to faster time-to-market as the turn-around fabrication time of GaAs PAs can be 1-2 months faster than that of Si-based designs! In fact, the timely cycles-of-learning in the context of design iterations is a massive advantage in product development. In addition, multi-mode, multiband PA design specifications are always subject to change and the large-signal modeling is hardly ever exactly accurate. Faster cycles-of-learning is a big advantage over Si-based PAs. Yet another advantage is that III-V suppliers, as the incumbent technology, are the proven and entrenched providers of handset PAs with low cost, high volume technology solutions. In fact, all major handset PA players operate their own fabs and/or processes [4, 5, 7] in facilities that may be fully depreciated.

For non-handset, medium power wireless PA applications, the benefits of adopting external PA versus an integrated CMOS PA for portable wireless products can be summarized as follows.

(1) Cost and Yield: analog power devices, matching circuits and passive devices do not scale downwards with the CMOS technology nodes. In fact, as CMOS continues to scale down, the supply voltage has progressively decreased from 3.3 V to 1.8 V to 1.2 V to 0.8 V. As supply voltage drops, I_{CC} must increase to deliver the same power level. This translates into increased device periphery and size, and therefore, increased die cost. However, cost analysis is always complicated and variable as the foundry wafer pricing and other costs are always negotitable. What is interesting is that the die area that the PA consumes, integrated or not, is roughly the same, making the cost of external PAs potentially much cheaper than the integrated CMOS PA. In fact, any analog circuit or sizable passives integrated within the digital chip using advanced and expensive nanometer CMOS technology may end up being more expensive in purely in terms of $\$/mm^2$ (c.f. either on-chip or external WLAN dual-band PA size $\sim 2mm^2$ [10–12]). Moreover, what may be more important is the impact on the yield. Integrating CMOS PA may cause considerable yield loss for CMOS transceivers. Yield will continue to suffer as the current trend towards combo chips (Bluetooth + WiFi; GiGa Ethernet + WiFi; DSL + WiFi, etc.) consumes more area with inevitably increasing costs.

(2) Efficiency and Performance: when external PAs are used for a wireless product, they can usually provide several percentage points of higher PAE than the integrated CMOS PA. This advantage is important for portable mobile and airborne applications. For USB applications, where the interface restricts power to 2.5W total (e.g., total $I_{cc} < 500$ mA at 5 V), dual band 2×2 MIMO or 3×3 solutions are beginning to prevail in computing applications as the trend towards Netbooks is limiting battery size and capacity. In this case, the MIMO PA design becomes a bit more challenging as it is now limited by the total *current* comsumption per transmitter (say only 166 mA for each TX for 3×3 MIMO) and not limited by the total maximum power design any more! The trend towards MIMO and concurrent operation, where multiple PAs operate simultaneously in one or both WLAN ISM bands will exacerbate the efficiency problem and create more serious thermal issues for the CMOS transceivers with on-chip PAs. In addition, the requirement for higher linear power, driven by the demand for long range and high data throughput for enterprise and entertainment applications, clearly favors the external PA solution. Robustness in this case is also a serious issue for high-power integrated CMOS PAs as VSWR mismatch can degrade the reliability or even damage the PA on-chip.

Not surprisingly, higher PAE is always welcome for lower heat dissipation and overall electrical energy consumption, especially now when so much attention is being directed towards global warming and energy usage. For example, near term expectations are that broadband equipment will contribute considerably to the electricity consumption of households in the European Community. Some have estimated total European consumption of up to 50 TWh per year for the year 2015 in this respect. Therefore, the EU has implemented a "Code of Conduct on Energy Consumption of Broadband Equipment" in Nov. 2008 to limit the maximum electricity consumption to 25 TWh per year, equivalent to 5.5 Millions tons of oil equivalent (TOE) and to total savings of about € 7.5 Billions per year. To help all parties to address the issue of energy efficiency, all service providers, network operators, equipment and component manufacturers are invited to sign this Code of Conduct operating in the European Community. It is, therefore, critically important that the PA efficiency of broadband equipment is maximized [13]. The efficiency of CMOS PAs is usually lower compared to SiGe and GaAs PAs due to lower gain and lower breakdown voltages. For example, a recent study reported that a 0.18 μm CMOS self-biased cascode PA measured with chip-on-board on FR4 PCB provides a 23 dBm output power and peak PAE of 42% at 2.4 GHz for Class 1 Bluetooth application (i.e., with constant envelope modulation) [12]. However, QFN *packaged* SiGe Bluetooth PA products currently sold in the market already provide 45% PAE for Bluetooth Class 1 application with better robustness than this CMOS prototype [14].

Another fully integrated 0.13 μm CMOS RF PA for Bluetooth Class 1 application was reported in [15] where four differential amplifiers are placed on a single chip and their outputs are combined with an on-chip LC balun. This technique allows a lower impedance transformation ratio for each individual amplifier, achieving a lower power loss. The CMOS PA achieves a measured output power of 23 dBm at a supply voltage of 1.5 V and a peak drain efficiency of 35% (and a global efficiency of 29%, which is not directly applicable to Bluetooth applications). That CMOS PA requires differential signals at the input but with single-ended power-combined output. Its peak efficiency still suffers considerably compared to commercially available single-ended I/O SiGe PA and GaAs PA products for Bluetooth applications. However, that CMOS PA does exhibit an

improvement at lower output power. A similar technique has been used for SiGe PA designs [16].

(3) Time-to-market: Integrated PAs can inadvertently increase the overall development cost of transceivers, require additional cycles-of-learning, and drive chip availability down as the yield, cost, and performance suffer. As mentioned previously in the GaAs case, the impact of this time-to-market factor should never be underestimated.

The benefits of using Si-based external PAs that leverage BiCMOS capability are beginning to be apparent. A recent paper reports an innovative architecture for a dual-band front-end module (FEM) for WiFi and MIMO radios, which consists of a dual-band SiGe PA and a SP3T switch-plexer (the SP3T switch-plexer has a SP3T switch and an integrated RX diplexer) [17]. The TX switch paths show 0.1 dB compression at >33.5 dBm with <1 dB insertion loss (IL) along with >18 dB isolation. The Rx switch/diplexer path has <2.0 dB IL for both bands. The band selectivity is >15 dB. This dual-band FEM reduces assembly complexity and post-PA loss, resulting in a high band performance of 3% EVM at 18 dBm output and < -50 dBm/MHz harmonic emissions in a 4×4 mm package. This performance is comparable to state-of-the-art integrated CMOS switches [18]. Therefore, external SiGe BiCMOS PAs can be quite attractive for medium power PA applications [19, 20]. In view of this level of performance and front-end integration it would seem to be too costly and slow to integrate the switch-plexer and dual-band PA onto the 45 nm CMOS transceiver die. Moreover, the performance degradation and thermal issues associated with such a CMOS integration effort seem to provide a poor return for the massive investment. Some other topics that are rather design specific are not discussed in this paper, such as the comparision of the contribution of Si versus GaAs substrates to the PA's intermodulation distortion products (IMD), and the coupling effects among components in a fully-integrated PA product versus that in a System-in-a-Package (SiP) product that includes the PA.

3. Conclusions

A sober analysis of the state-of-the-art transceiver and device design trends reported by the leaders in the industry and academia reveal an extremely challenging effort to integrate nm-CMOS PAs on-chip for multimode, multiband wireless products. Their ability to compete with external GaAs or Si/SiGe PAs solutions is, at this point, speculative. Moreover, higher development cost, loss in time-to-market, degraded RF performace (including lower output power and PAE), and the on-going inability to integrate filters and switches make integrated CMOS PAs a less attractive approach for future multi-mode, multiband wireless RF-SoC products.

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