Hindawi Publishing Corporation
VLSI Design
Volume 2010, Article ID 512312, 14 pages
doi:10.1155/2010/512312

Research Article

FPGA-Based Software Implementation of Series Harmonic Compensation for Single Phase Inverters

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Received 10 June 2009; Accepted 20 October 2009

Academic Editor: Gregory D. Peterson

This paper presents a single chip FPGA (Altera Cyclone II) controlled single phase inverter, programmed for the reduction of harmonics in the output voltage. Separate composite digital observers have been designed for extracting the fundamental and harmonic components of the voltage and the highly distorted current signals, particularly when the inverter supplies nonlinear loads. These observers have been embedded into the FPGA along with the controllers and I/O interfaces. The multiple observers yield very pure in-phase and quadrature voltage signals for use in the outer loop and similar signals for stabilizing the inner current loop. The Inverter could be modeled as a feed back control system with the fundamental component of the voltage as the desired output while the voltage harmonics take the role of noise creeping into the output. To obtain a very low total harmonic distortion in the voltage waveform, the well-known control strategy of using a very large feed back around the noise signal has been employed.

1. Introduction

Stand-alone inverters are commonly used in the case of power failure, to deliver power for critical loads, which demand purely sinusoidal voltage at the specified magnitude, frequency, and low total harmonic distortion (THDv). The THDv in industry should not exceed 5% as per the guidelines given in the IEEE Standard 519-1992. Fixed passive filters may not perform well, particularly when the operating frequency drifts far away from the set resonance frequency. Alternatively, active filters can be employed. Many control methods have been proposed basically for obtaining pure sinusoidal output with good voltage regulation and fast dynamic response [1–9]. Sinusoidal pulse width modulation (SPWM) schemes for stand-alone inverters have been shown to perform well with linear loads [10]. However, with nonlinear loads the SPWM scheme does not guarantee low distortion in the output voltage. The availability of low cost microprocessors has led to discrete-time methods, such as repetitive control [1, 2], sliding mode control [3], and deadbeat control [4, 5] to improve the performance. To get zero steady-state error in the output voltage and fast response virtual inductor, capacitor and a resistor were used in [6], while internal model control scheme (IMC) was employed in [7]. The control methods presented in [8, 9] employ two-feedback control loops. The inner loop is used for current control and the outer loop is used for voltage control. Many of these methods have not specifically considered the reduction in distortion due to nonlinear loads.

The emergence of FPGAs has drawn much attention due to their shorter design cycle, lower cost, and higher density. The simplicity and programmability of FPGAs make them a most favorable choice for prototyping digital systems. When comparing the dynamic performance and control capabilities in PWM-controlled Power converters FPGA-based digital techniques are better than DSPs [11].

Basically a Luenberger observer (simple observer) can be used for obtaining the filtered fundamental component from the periodic output voltage and current waveforms, which leads to the indirect estimation of the total harmonics in the output voltage due to the nonlinear loads [12]. The Inverter can be modeled as a feed back control system with

the fundamental component as the desired output, while the harmonics take the role of noise creeping into the output. The well-known control strategy of using a large feed back around the noise signal was employed, to reduce the effect of noise at the output. The net effect is a smoother output voltage showing negligible total harmonic distortion, even with nonlinear loads. In this paper, an attempt has been made to show the usefulness of controlling inverters by composite observers [13, 14] rather than by using simple observers. The typical composite observer provides the pure filtered fundamental in-phase signal along with the companion quadrature signal. Alongside, the various harmonics are also estimated as instantaneous in-phase and quadrature signal pairs [13, 14]. The composite observer has a repetitive parallel structure, which can be easily implemented in an FPGA.

2. System Overview

An inverter supplying a rectifier with an RC load is shown in Figure 1. The parameters of the inverter are listed in Table 1.

The proposed control scheme can be split into two parts:

(a) use of in-phase and quadrature fundamental output voltage and current signals for conventional D-Q control,

(b) reduction of the distortion in the output voltage waveform, by feedback of voltage harmonic signals.

2.1. Design of Discrete Composite Observer. Observability means the ability to estimate the initial state from an infinite number of input-output observations. Any periodic signal $y(kT)$ rich in harmonics and a DC bias can be modeled as if $y(kT)$ emanates from a system described by

$$\begin{aligned} x((k+1)T) &= A \cdot x(kT), \\ y(kT) &= C^t \cdot x(kT), \end{aligned} \tag{1}$$

where

$$A = \begin{bmatrix} A_0 & 0 & 0 & - & 0 & - & 0 \\ 0 & A_1 & 0 & - & 0 & - & 0 \\ 0 & 0 & A_2 & - & 0 & - & 0 \\ - & - & - & - & - & - & - \\ 0 & 0 & 0 & - & A_m & - & 0 \\ - & - & - & - & - & - & - \\ 0 & 0 & 0 & - & 0 & - & A_N \end{bmatrix}; \quad A_0 = 1, \tag{2}$$

$$[C]^t = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & - & - & 1 & 0 \end{bmatrix}.$$

The typical mth subblock is given by

$$Am = \begin{bmatrix} \alpha_m & \alpha_{m-1} \\ \alpha_{m+1} & \alpha_m \end{bmatrix}, \quad \text{where } \alpha_m = \cos(m \cdot \omega_1 T) \tag{3}$$

Table 1: Inverter system parameters for simulation.

Battery Voltage V_{dc}	24 V
Dither Frequency	10 kHz
Filter Inductance L_f; R_f	1.0 mH; 1 Ω
Filter Capacitance C_f; R_c	96 μF; 0.1 Ω
Rectifier Load: Resistance R_L & Capacitance C_L	10 Ω, 1 mF
Resistive Load R_L	10 Ω

V: Volt; kHz: kilo Hertz; Ω: Ohm; mH: milli-Henry; μF: micro-Farad; mF: milli-Farad.

with state vector $x_m(kT)$ and output variable $y_m(kT)$ defined by

$$\begin{aligned} x_m(kT) &= \begin{bmatrix} x_{m1}(kT) \\ x_{m2}(kT) \end{bmatrix}, \qquad y_m(kT) = C_m^t x_m(kT), \\ C_m^t &= \begin{bmatrix} 1 & 0 \end{bmatrix} \quad \text{for } m = 1, 2, 3, \ldots, N, \ C_0 = 1. \end{aligned} \tag{4}$$

The Discrete Composite Observer is a closed loop model of the system, with an open loop part consisting of N controlled digital oscillators as sub-blocks, one for each harmonic, arranged in the parallel format along with a DC block. The mth block of the observer can be modeled with a state vector $\hat{x}_m(kT)$ and an output variable $\hat{y}_m(kT)$ defined by:

$$\begin{aligned} \hat{x}_m(kT) &= \begin{bmatrix} \hat{x}_{m1}(kT) \\ \hat{x}_{m2}(kT) \end{bmatrix}, \qquad \hat{y}_m(kT) = \hat{x}_{m1}(kT), \\ \hat{x}_m((k+1)T) &= A_m \hat{x}_m(kT) + D_m e(kT), \\ \hat{y}_m(kT) &= C_m^t \hat{x}_m(kT); \quad m = 0, 1, 2, \ldots N; \\ D_m &= \begin{bmatrix} d_{m1} \\ d_{m2} \end{bmatrix} \quad \text{for } m = 1, 2, 3, \ldots, N, \ D_0 = d_0. \end{aligned} \tag{5}$$

The observation error $e(kT)$ is defined by

$$e(kT) = y(kT) - \hat{y}(kT) = C^t[x(kT) - \hat{x}(kT)] \ = C^t E(kT), \tag{6}$$

where

$$\hat{y}(kT) = \sum_{m=0}^{m=N} \hat{y}_m(kT), \qquad E(kT) = [x(kT) - \hat{x}(kT)]. \tag{7}$$

The sum of all the individual $(N+1)$ output variables $\hat{y}_m(kT)$ shown in (7) is the scalar output of the observer.

Under steady state, $\hat{y}(kT) \rightarrow y(kT)$ as $k \rightarrow \infty$.

Each sub-block has two fixed parameters $Dm = (dm1, dm2)$ and only one tunable parameter α_m. This facilitates easy tuning of the observer under wandering frequency conditions. Only one multiplier is required rather than two required for tuning the two-dimensional sub blocks [14].

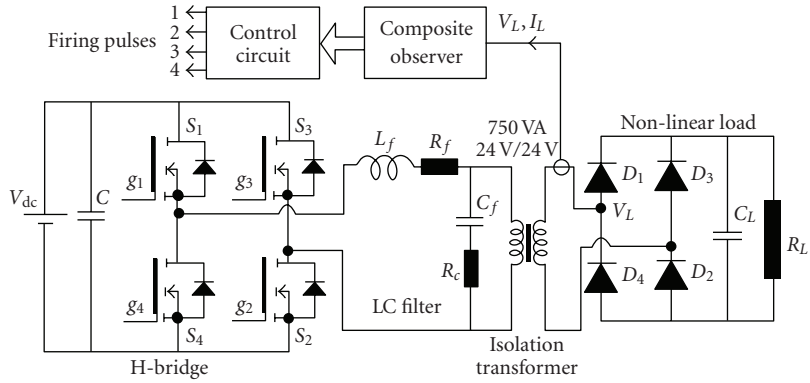


Figure 1: Single phase inverter circuit under rectifier load with RC filter.

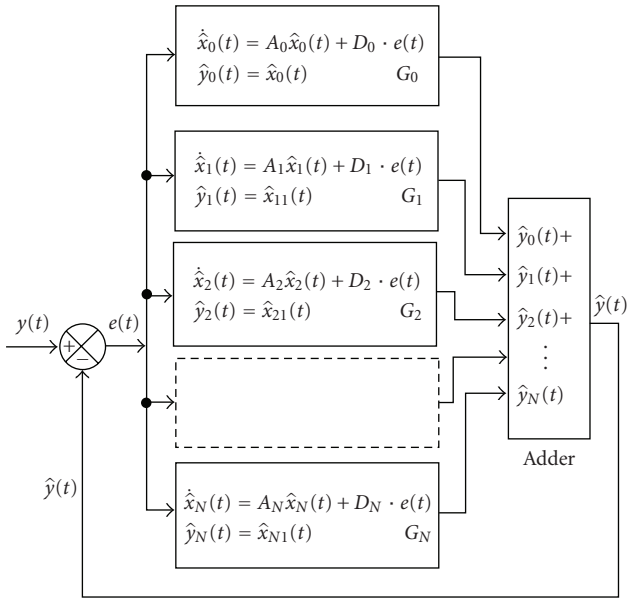


Figure 2: Structure of Discrete Composite Voltage Observer.

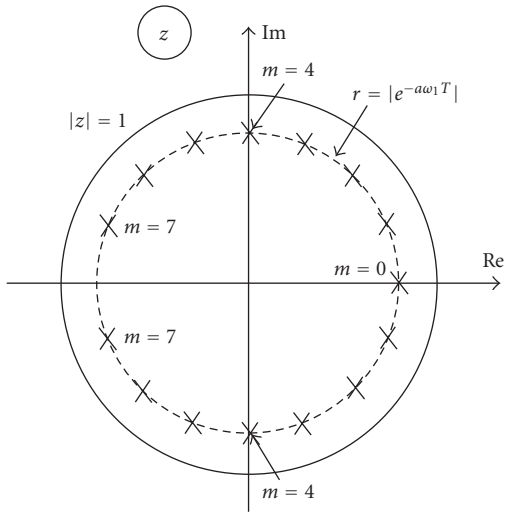


Figure 3: Poles of Discrete Observer for $(2N + 1) = 15$.

The composite observer defined so far can be concisely written as

$$\hat{x}((k+1)T) = [A]\hat{x}(kT) + [D] \cdot e(kT),$$
$$\hat{y}(kT) = C^t\hat{x}(kT), \tag{8}$$

where D the gain vector is given by

$$D = [d_0, (d_{11}, d_{12})\ (d_{21}, d_{22}) \cdots (d_{m1}, d_{m2}) \cdots (d_{N1}, d_{N2})]^t. \tag{9}$$

The $2N + 1$ observation-error-vector $[E(kT) = x(kT) - \hat{x}(kT)]$ is composed of the individual estimation errors in the DC, fundamental as well as the real and imaginary (orthogonal) harmonic components of the given signal.

Using (1), (6), and (8), we get

$$E((k+1)T) = [A - \mathrm{DC}^t]E(kT). \tag{10}$$

The characteristic equation, for the error-difference equation in (10), can be obtained in the z-domain as

$$\mathrm{Det}[zI - A + \mathrm{DC}^t] = 0, \tag{11}$$

where I is a $(2N + 1) \times (2N + 1)$ Identity matrix.

The $(2N + 1)$ roots of the characteristic equation, which are also defined as the observer poles, can be located within the unit circle in the z-plane (Figure 3). Such an "observer pole placement" makes the closed loop observer stable and the norm of the error vector E vanishes as the time tends to infinity, that is, $\|E(kT)\| \to 0$, as $k \to \infty$.

Let the $2N + 1$ closed loop poles to be equidominant and located such that $z = e^{-\delta T}$ for $m = 0$ and

$$z = e^{-\delta T}[\alpha_m \pm j\beta_m], \tag{12}$$

where $\alpha_m = \cos(m \cdot \omega_1 T)$, $\beta_m = \sin(m \cdot \omega_1 T)$ for $m = 1, 2, \ldots, N$, $\alpha_0 = 1, \beta_0 = 0$, $\delta = a \cdot \omega_1, a > 0$, which controls the observation speed, and ω_1 is the Fundamental frequency.

In the structure chosen, for a typical sub-block "m", the state variable $\hat{x}_{m1}(kT)$ will ultimately merge with the mth harmonic in the input signal. Each sub-block in the observer acts like a comb filter, accepting the signal of the

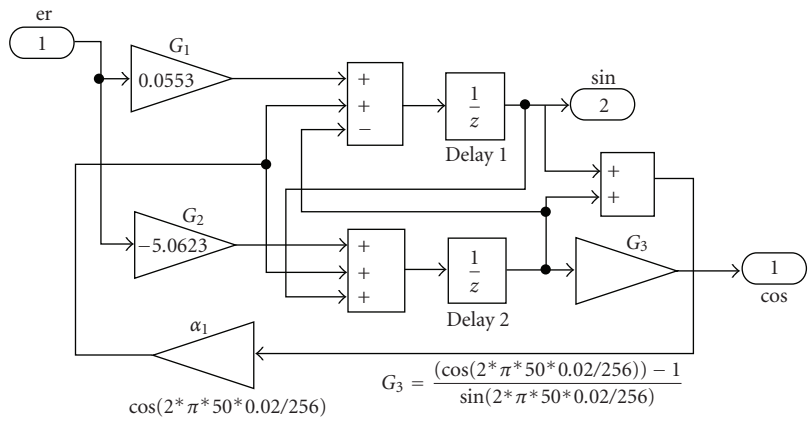


Figure 4: Structure of the Fundamental block in the Discrete Composite Voltage Observer.

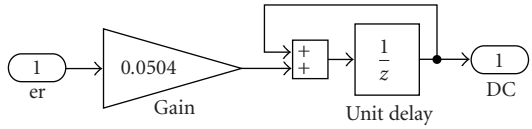


Figure 5: DC block in the Discrete Composite Voltage Observer.

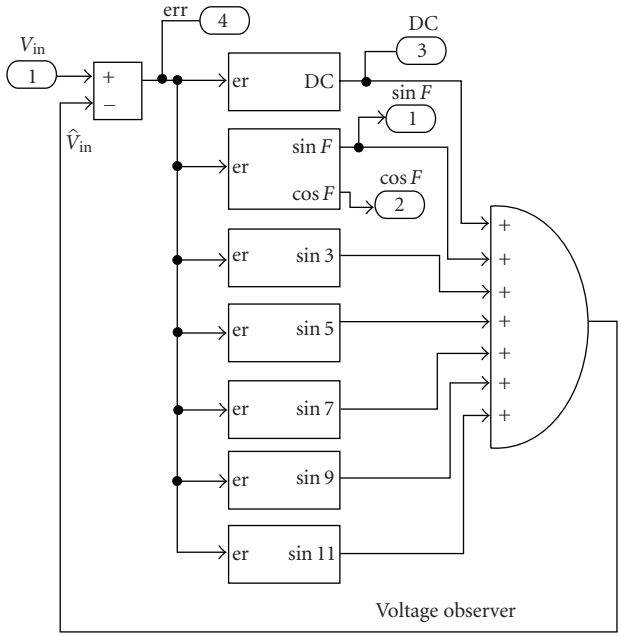


Figure 6: Structure of Discrete Composite Voltage Observer.

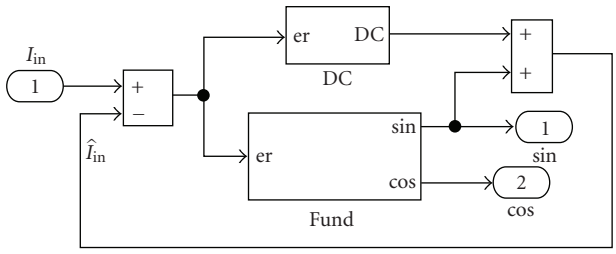


Figure 7: Structure of Current Observer.

respective tuned frequency and rejecting all other harmonic frequencies. The state variable $\hat{x}_{m2}(kT)$ will exhibit a phase-shift of 90° with respect to the signal $\hat{x}_{m1}(kT)$. Further, a magnitude scaling factor $g_m = (\alpha_m - 1)/\beta_m$ needs to be introduced for this orthogonal signal, for equalizing the amplitudes of the two signals $\hat{x}_{m1}(kT)$ and $\hat{x}_{m2}(kT)$. The observer can be tuned when the frequency of the input signal $y(kT)$ to the observer drifts. This is done by adjusting the parameter α_m using the correlation between the error signal $e(kT)$ and the fundamental quadrature signal $\hat{x}_{12}(kT)$ [14]. The fundamental block in the composite observer for $a = 1$ is shown in Figure 4. This "s" domain specification corresponds to $|z| = 0.9758$ in the digital domain (see Figure 3), for a sampling frequency of 12.8 kHz. The various harmonic blocks also have the same structure. However, the quadrature signal ("cos") need not be taken out for the harmonics, thereby reducing the number of gain elements required in the FPGA realization. The structure of the DC block is shown in Figure 5. The gains in these blocks correspond to real part of observer poles at $a = 1$. The composite observer used for voltage signal processing is shown in Figure 6.

The current observer can also be made to have the same structure as the voltage observer. However, to reduce the number of DSP elements required, only the DC block and the fundamental block were used for the current observer as shown in Figure 7.

2.2. D-Q Control Using Fundamental Components. In a 2-phase system the steady-state errors could be overcome by introducing DC reference-commands and the corresponding DC variables for representing the sinusoidal trajectories. When DC variables converge to constant values under steady-state, it is easier to make the steady-state error zero by including a conventional PI controller in the control loop.

Using a discrete composite voltage observer, having DC and odd harmonic blocks up to 11th $(0, 1, 3, \ldots, 11)$, the in-phase (sine) and the fictitious quadrature (cosine) fundamental voltage signals of the inverter can be derived. Applying the Park transformation, in a manner which is

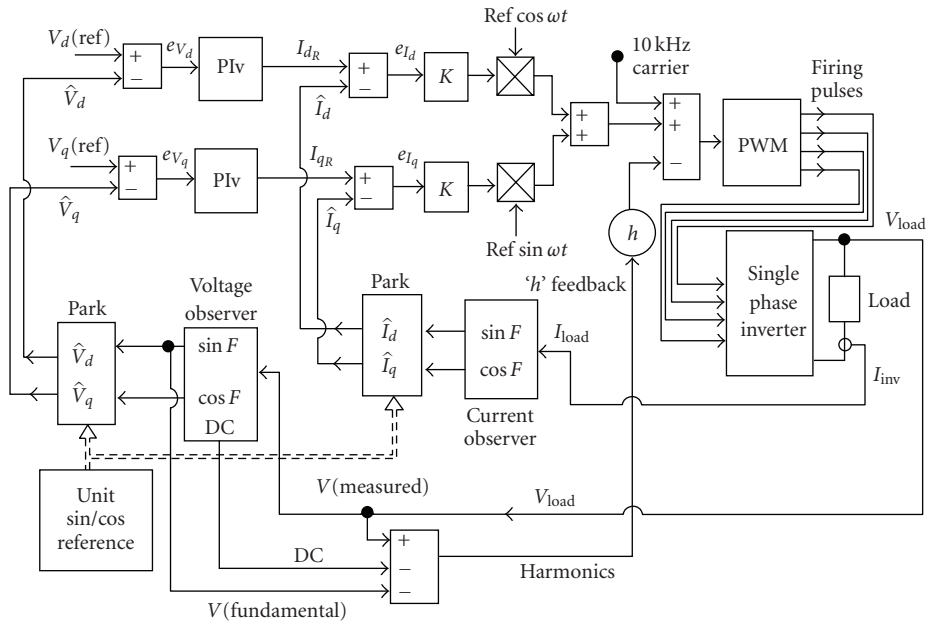


Figure 8: Schematic of the Proposed Control Strategy for the inverter.

analogous to 2-phase systems, these components can be transformed to "D-Q" coordinates. The Park transform requires unit sine and cosine reference signals which are generated internally for the stand-alone inverters:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sin(\omega_1 t) & \cos(\omega_1 t) \\ \cos(\omega_1 t) & -\sin(\omega_1 t) \end{bmatrix} \cdot \begin{bmatrix} \sin(\omega_1 t + \varphi_2) \\ \cos(\omega_1 t + \varphi_2) \end{bmatrix}. \quad (13)$$

Ideally, the load voltage is expected to contain only the fundamental components, whereas all the other harmonic components including random noise in the voltage loop must be zero. Now, the estimation speed of the observer depends on the pole-location. In the continuous domain, observer poles closer to the origin of the s-plane make the estimation sluggish, while the poles located farther from the origin of the s-plane make the observer faster. On the other hand, for a digital version of the observer, placing the poles closer to the origin in the "z" plane can speed up the estimation while placing the poles near to the unit circle makes it sluggish. In any case, very high-speed observers show a heavy distortion in the extracted fundamental and other components. Placing the observer poles closer to the unit circle in the z-domain (closer to origin of the s-plane) makes the extracted fundamental component pure and accurate, at the cost of increased time for estimation, which may even lead to instability of the voltage control system. The steady-state error-vector between the desired d-q components and the actual d-q components obtained from the composite voltage-observer is processed through PI controllers to obtain d-q current references. In the simulation and experimental studies presented in this paper, the decay factor "a" for voltage observer and current observer were set at 1.

The control scheme for reducing harmonics in the inverter is shown in Figure 8. The steady-state error-vector $[e_{vd}, e_{vq}]$ between the desired D-Q component values and the actual D-Q component values obtained from the voltage-observer is processed through PI controllers to obtain D-Q current references. Similarly, using another simple observer, the fundamental in-phase and fictitious quadrature current signals are estimated. This facilitates transformation of the current to the D-Q frame. The current error-vector $[e_{Id}, e_{Iq}]$ in the D-Q frame is processed by simple gain elements (k) even though PI or lead type compensators could have been used. The steady outputs of the two controllers in the current loop are converted into the in-phase and quadrature time signals, via the single-phase-inverse Park transform. The two time signals are added to get the sinusoidal reference signal for pulse width modulation as shown in Figure 8. Without any compensation for harmonics, the output voltage is heavily distorted for a "nonlinear load", consisting of a rectifier driving a RC load ($10\,\Omega \| 1\,\text{mF}$). The THDv is about 15.34% even though the control signal appears to be a pure sine wave. The distorted output voltage, pulsed load current, and the control voltage are shown in Figure 9. The distortion is mainly due to the voltage drop caused by the harmonic currents in the series R-L filter of the inverter.

2.3. Series Compensation by Harmonic Feedback. Let us consider the harmonics creeping into the output due to the voltage drop in the inductor as shown in Figure 10(a). The sum of all the harmonics can be assumed to be equivalent to a noise signal, superimposed on the fundamental component. In Figure 10(b), both the noise and the signal have unity gain. If a control loop could be built around the noise signal, with a high feedback gain "h" for the noise alone, as shown in

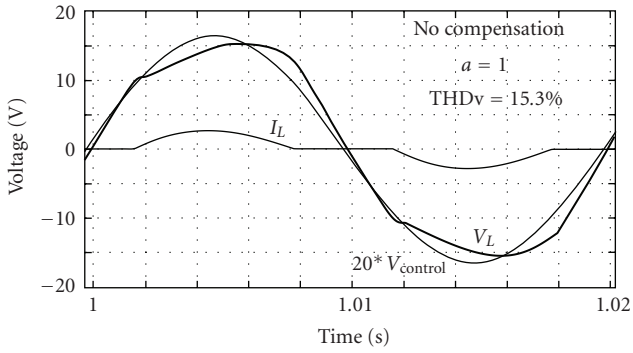


Figure 9: Distorted output voltage, current, and control signal with no harmonic feedback.

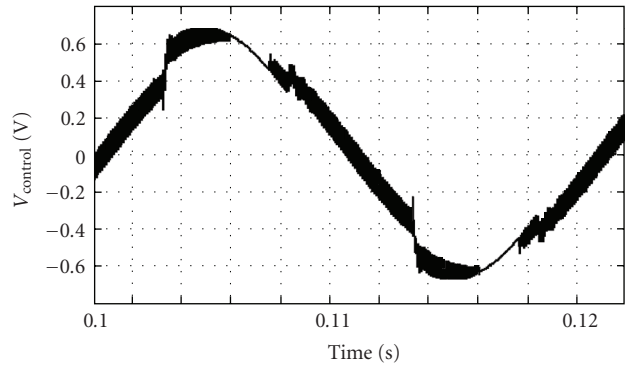


Figure 11: Control signal which yields a pure sine Output.

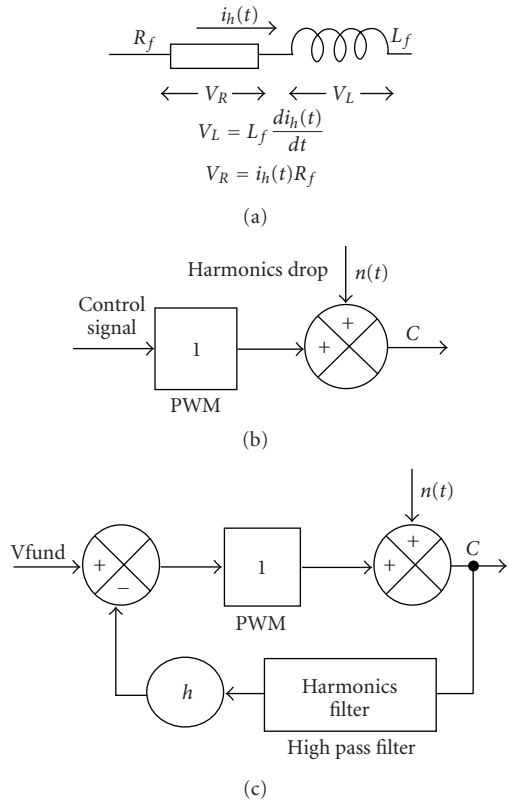


Figure 10: (a) Voltage drop across the inductor. (b) Equivalence of harmonic distortion to noise. (c) Attenuation of noise in closed loop.

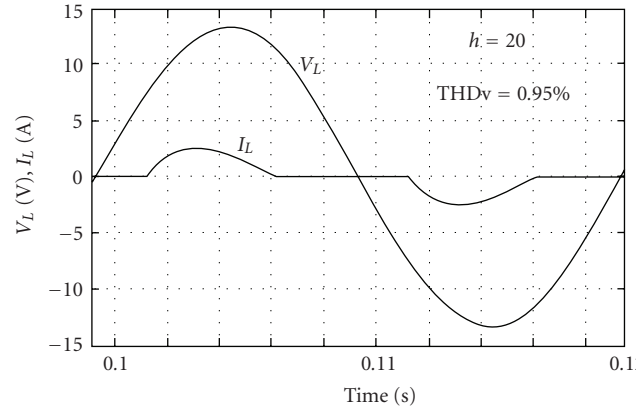


Figure 12: Load voltage signal after harmonic feed-back while supplying a current to a nonlinear load.

Figure 10(c), its effect in the output can be made negligible. This requires a highpass filter, which can be realized from the composite voltage observer, designed for extracting the various harmonics.

The high-frequency harmonic signal, which is devoid of the fundamental component and DC, can be fed back with a high gain "h" for reducing the distortion as shown in Figure 8. While the fundamental gain remains unaffected at unity, the closed loop gain (K_{nf}) for the harmonics becomes smaller:

$$K_{nf} = \frac{1}{(1+h)}. \tag{14}$$

For example, when $h = 20$, the effect of noise with this local loop reduces to $K_{nf}/1.0\sim = 5\%$.

Interestingly, due to harmonic feedback, the control signal becomes enriched with harmonics, as shown in Figure 11. In contrast, the output voltage waveform becomes a purer sine wave as shown in Figure 12.

2.4. Model of the Proposed Control System. A model for the fundamental components, as shown in Figure 13, of the inverter control system is obtained on the basis of the following assumptions. Since the loads may be nonlinear, the steady-state fundamental components of the voltage and current signals alone are taken into account for modeling. The inverter is assumed to drive near-unity power factor loads, which makes the system somewhat decoupled as far as the direct and the quadrature channels are concerned. So, we need to consider either the direct axis channel or the quadrature axis channel for analysis. The pulse width

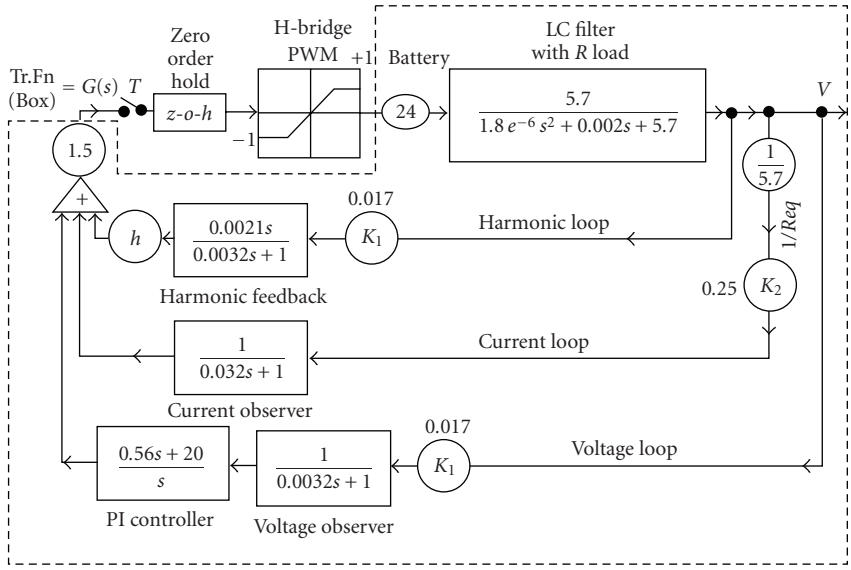


Figure 13: Block diagram for any one channel (V_d or V_q).

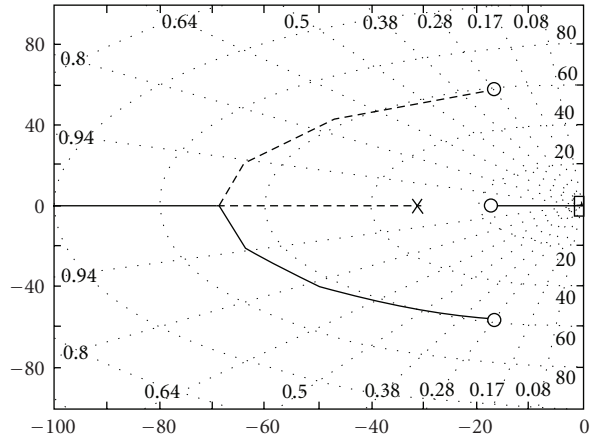


Figure 14: Root Locus for determining integral constant of the PI controller.

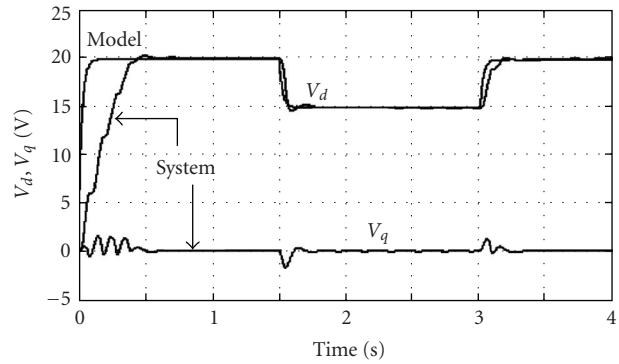


Figure 15: Validation of Model for a step disturbance in V_{dref}.

modulating (PWM) block is modeled as a unity-gain ($k \cong 1$) saturation-block, which feeds into a linear gain, of value = 24, the battery voltage. The input saturation level of PWM block is the peak of the carrier signal. The LC filter with resistive load can also be included in the model. The observer is equivalent to a lowpass filter in the d or q domains. A simple proportional controller with a fixed gain setting (say 1.5) is sufficient for the current loop because the PI controller in the voltage-loop will guarantee the accuracy of the amplitude of the output voltage, in the linear operating region. The real part of the current-observer pole was placed at -0.1ω. This is slow enough to filter out the harmonics of the current under nonlinear loads like a rectifier with RC filter. The real part of the voltage-observer pole is 10 times faster than the current-observer pole and is placed at -1ω. The slower current loop causes reduced phase margin and increased overshoot under transient conditions. The stability of the total control system depends mainly on the feedback factor "h", observer pole location, and the PI controller settings of the voltage loop. While some of the parameters listed above can be intuitively assigned, the major problem remaining is the design of the PI controller so that the control system would remain stable.

Sketching the root locus and enlarging it around the origin (Figure 14) reveal one real pole and a complex closed loop pole pair being dominant. By adjusting the zero of the PI controller, all these three poles can be made to have the same negative real part or remain equally dominant as the closed loop gain tends to infinity. For Req = 5.7 Ω, h = 20, the settings are Kp = 0.56 and Ki = 81. It is appropriate to carry out the stability analysis in the z-domain.

2.5. Validation of Model. For a step change in the reference V_d, the response of the model and system is shown in Figure 15. The system and the model initial conditions were different. However after convergence, the incremental responses of the system and the model coincide reasonably well.

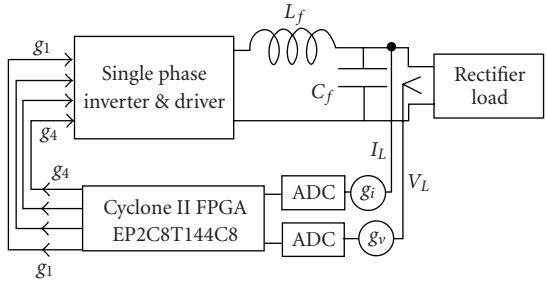


Figure 16: Overall Hardware implementation circuit of the inverter.

3. FPGA Implementation Schematic of the Controller

The overall hardware implementation circuit of the single phase inverter is shown in Figure 16. The measured output voltage and current are normalized to unity using g_v and g_i, which include voltage divider as well as the analog amplifier gains. Inside the FPGA the maximum voltage and current variables are made equal to unity. Hence the same setup could be easily extended to any voltage or current levels, by suitably adjusting the external range setting devices.

The implementation consists of two separate ADCs for feeding in the load voltage and current into the control circuit as shown in Figure 17. A serial +5V, 12-bit, MSOP-8 package analog-to-digital converter ADS7835 was interfaced with Cyclone II FPGA. Handshaking between FPGA and ADS7835 is through 3 signals named Convert, Clock, and Data. The Convert and Clock are input signals to ADC from FPGA, while the converted Data goes into the FPGA. Since the level of the digital I/O signals for the FPGA is at 3.3 V and the ADC operates at 5 V, a digital buffer (16 pin 74HC366) has been provided for the two channels. The serial data from ADS7835 has been converted into 12-bit parallel data in the integer format in the FPGA, which is shown in Figure 17. Since the integer signals are to be normalized to 18-bits floating point, that is, [3 : 15], further conversion to floating point is necessary which is illustrated in Figure 18. Bit-by-bit extraction and addition in the floating point has been carried out for achieving this. These two procedures were incorporated as subsystems.

The measured current and the voltage variables available in the floating point format are fed to separate observers, one for voltage and the other for the current as shown in Figure 19. The basic unit sinusoidal signal is generated by using a look up table and an address-generating counter, triggered by the same pulses, which drive the observers. The arrangement is shown in Figure 20. A 50 Hz unit sine wave is generated, by creating 256 data entries, obtained by sampling off-line, 256 times a full unit sine wave. The LUT which holds the data in the [3 : 15] floating format has an 8-bit address space, which can be accessed by an 8-bit address counter. The 12.8 kHz enabling pulses for the address counter are derived from a mod 313 counter, whose clock ticks at 4 MHz. The unit sine wave from the LUT is fed to an observer of the structure shown in Figure 4, so as to get the unit sine and cosine reference signals as shown in Figure 20. The extracted in-phase and quadrature fundamental signals from the voltage or current observer and the lookup table generated unit sine and cosine waves are used to derive the D-Q components of load voltage or current through the Park transform. A typical Park Transform block is shown in Figure 21. The references V_{dref} and V_{qref} are set as required in floating point format. The V_d and V_q feedback signals are derived from the voltage observer, after Park transformation as explained earlier. The errors in V_d and V_q are processed through separate PI controllers. The outputs of these PI controllers are taken to be the I_{dref} and I_{qref} signals for inner current loop. The current error signals are processed by proportional controllers and further converted into sinusoidal control signal via single-phase-inverse park transform as shown in Figure 22.

Along with this control signal, voltage harmonics are fed back with a large gain and then filtered to remove very high-frequency noise corrupting the control signal. A 10 kHz triangular carrier (dither) signal is used for the generation of sinusoidal PWM pulses required by the power MOSFETs of the inverter. The schematic is shown in Figure 23.

4. Experimental Results

Using the Altera DSP Builder, a digital version of the control scheme was designed and implemented in a Cyclone II (Altera) FPGA. The load voltage and current corresponding to a nonlinear load, with a harmonic feedback gain in the range $0 < h < 20$, were recorded, for validating the simulations. Figure 24(a) shows the heavily distorted load voltage (THDv 16.4%) for a nonlinear current since no harmonic feedback compensation was provided. Similarly even when a composite voltage observer is used along with a simple current observer, as long as no harmonic feedback compensation is provided, the voltage waveform will be distorted (THDv 15.29%) for a nonlinear load (Figure 24(b)). In Figure 25(a), the harmonic feedback gain "h" was set at 20, while supplying a rectifier load of $10\,\Omega \| 1\,\text{mF}$. It is seen that even a simple voltage observer gives a pure sine wave output, showing a THD of 1.2% When a composite voltage observer is used along with a simple current observer, the voltage waveform is still purer showing a THD of 0.98% (Figure 25(b)). Even though this result is attractive, very large harmonic feedback gains make the control system sluggish and reduce the stability margin appreciably. From Table 2, it is clear that a harmonic feedback gain of 5 is sufficient to get a THD of 4.67%.

5. Resource Utilization in FPGA

The realization of the control schemes has been done using DSP builder software in MATLAB simulink environment. DSP Builder tool provides a seamless design flow of algorithmic design and system-level integration in MATLAB and Simulink software and then ports the design to HDL for use in Altera's Quartus II design software. The DSP Builder

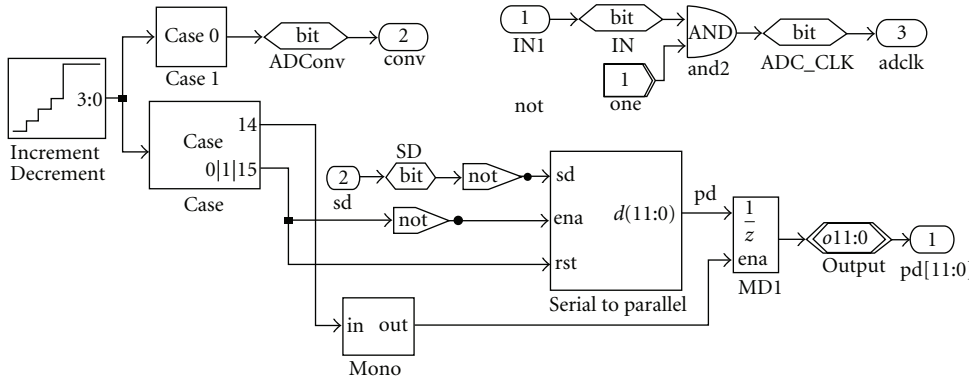


Figure 17: ADC Program for ADS 7835 in DSP Builder.

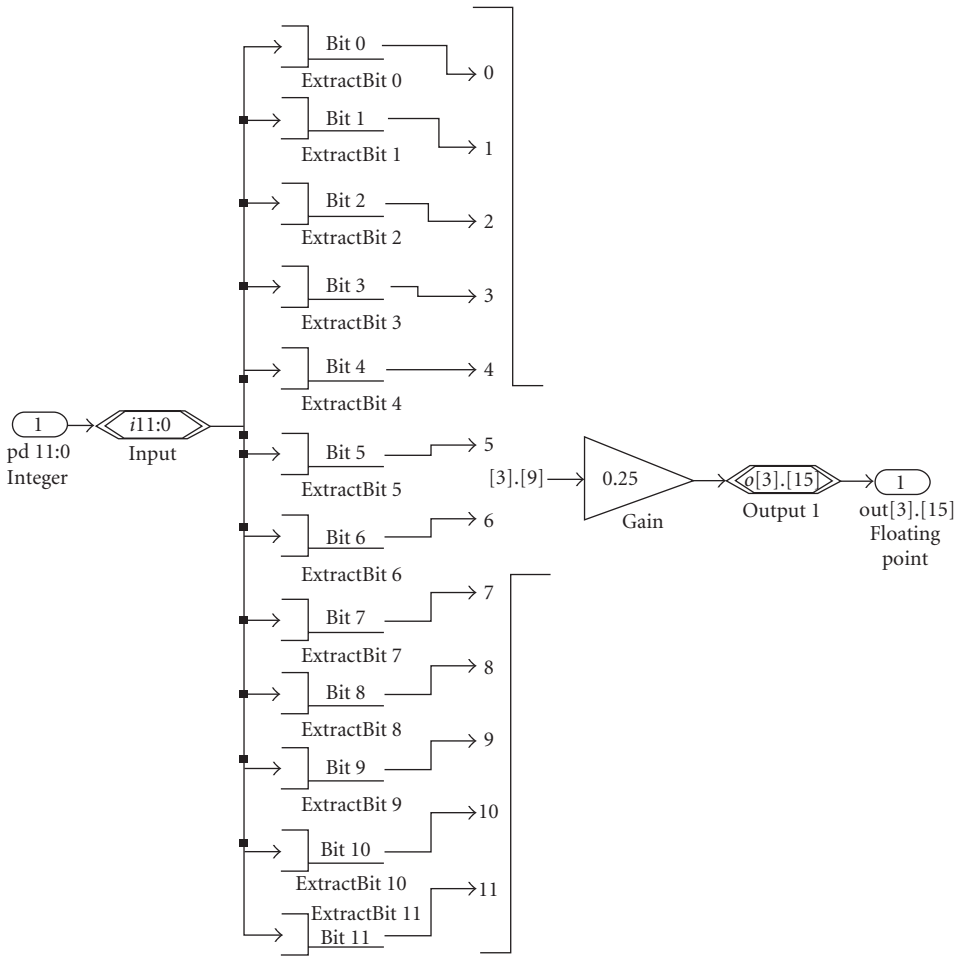


Figure 18: Integer to floating point block.

can automatically generate preverified RTL output files—including an RTL design and testbench—from the Simulink software. The DSP Builder design flow for Altera FPGA is shown in Figure 26. Quartus II software has been used for fitting the synthesised algorithm into the FPGA. The resource utilization summary for both the control schemes has been shown in Table 3. The total logic elements needed to implement the composite observer scheme using Cyclone II is only about 66%. Table 4 indicates the resources utilized by both the observers in Cyclone II.

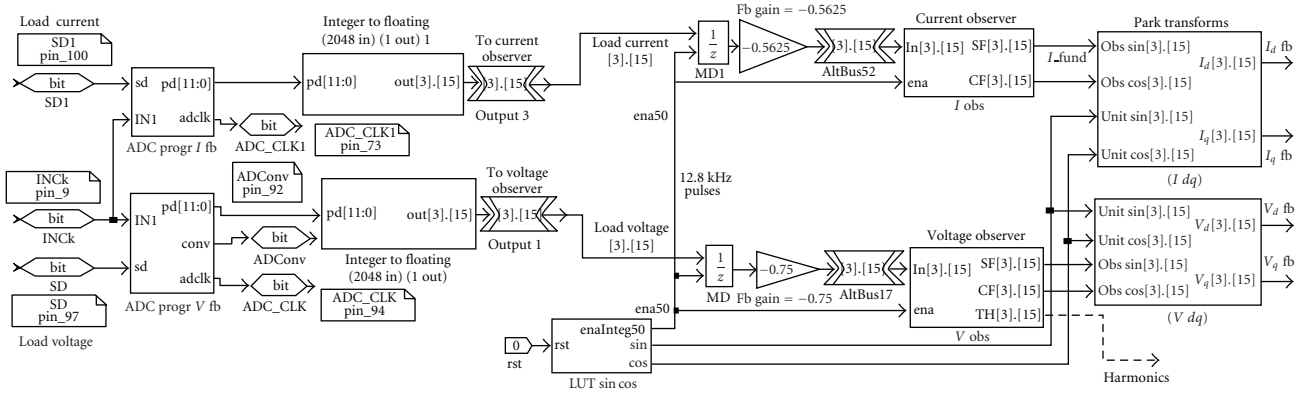


Figure 19: Generation of D-Q Voltage and Current Signals using the Output of the Inverter.

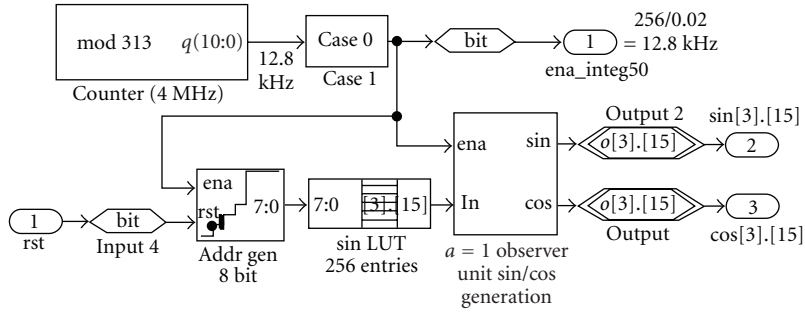


Figure 20: Internal Generation of Unit sine and cosine signals.

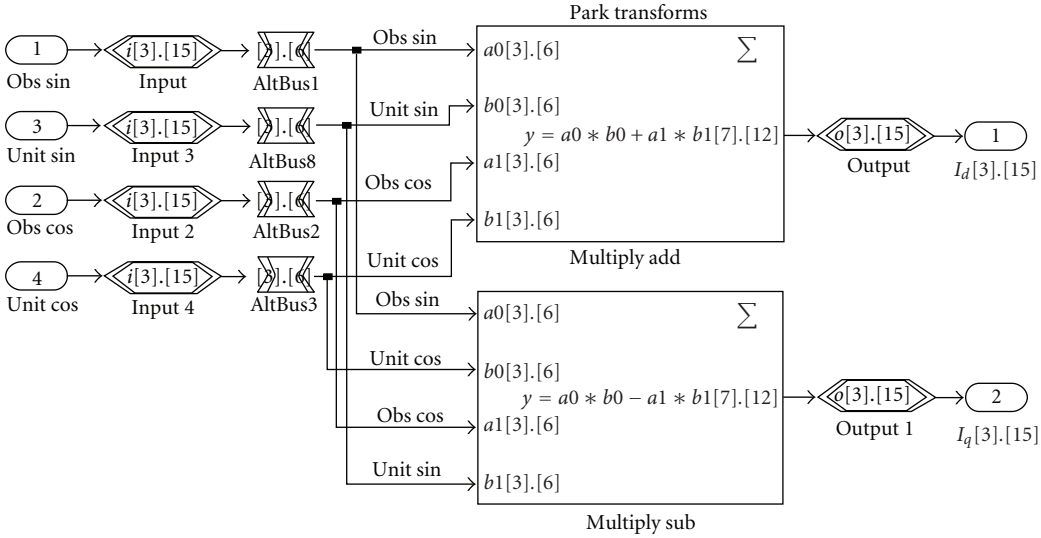


Figure 21: Computation of D-Q components (Park Transform).

Table 2: % THDv of the inverter output voltage with the two different schemes.

h	% THDv			
	Composite voltage observer and Simple current observer		Simple voltage and current observers	
	Simulation	Expt.	Simulation	Expt.
0	15.34	15.29	15.94	16.40
5	3.309	4.67	3.515	4.79
10	1.773	2.07	1.927	2.91
15	1.197	1.71	1.321	1.99
20	0.903	0.97	1.01	1.20

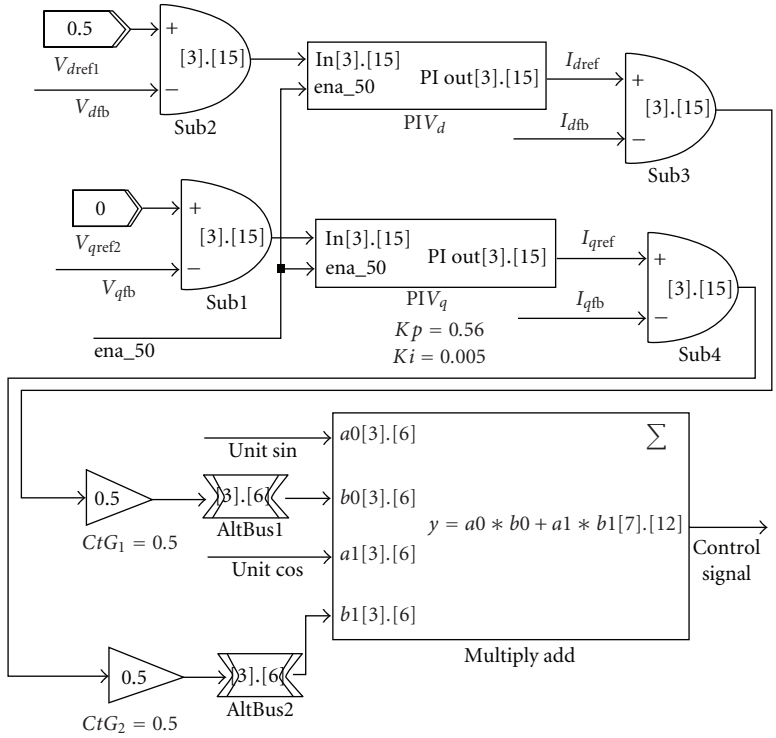


Figure 22: Fundamental Control signal generation via single-phase-inverse Park transform.

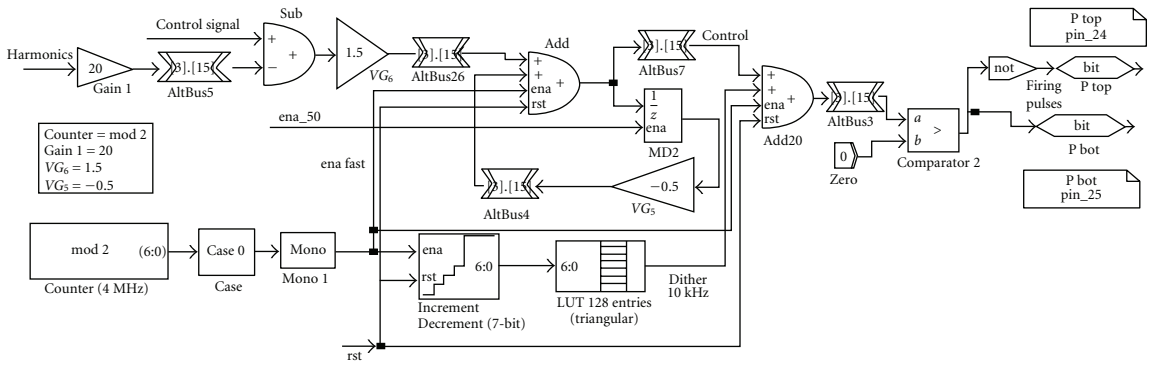


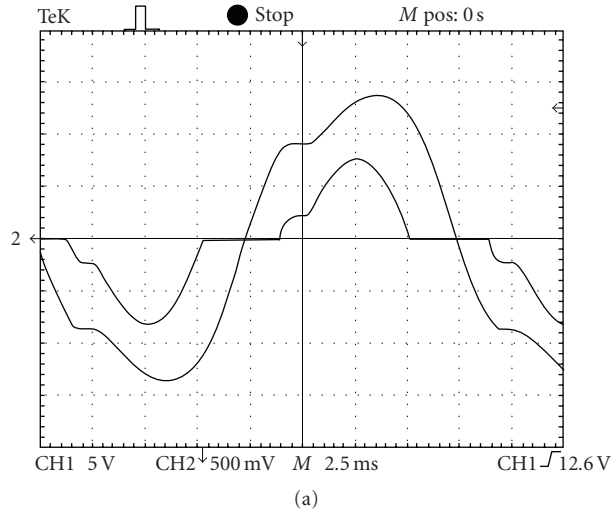
Figure 23: PWM pulse generation from the Control Signal.

Table 3: Resource utilization of the Simple Observer (SO) and Composite Observer (CO) Control scheme using Quartus II tool.

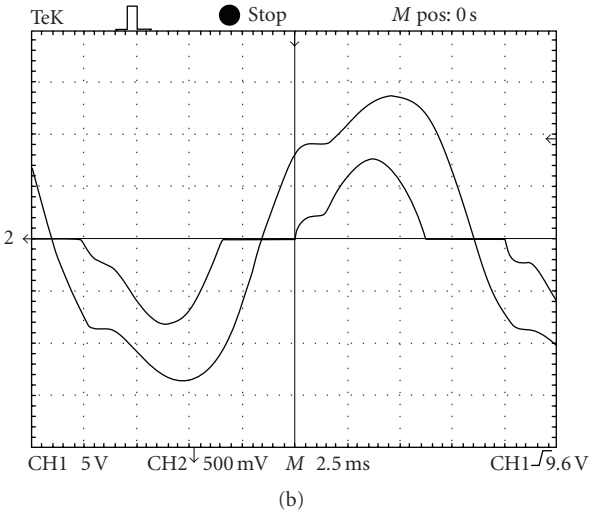
	SO	CO
Family	Cyclone II	Cyclone II
Device	EP2C8T144C8	EP2C8T144C8
Total logic elements	1,779/8,256 (21%)	5,517/8,256 (66%)
Combinational with no register	1448	4981
Register only	16	13
Combinational with a register	315	523
Logic element usage by number of LUT inputs		
4 input functions	215	662
3 input functions	1207	3967
<=2 input functions	341	875
Register only	16	13
Combinational cells for routing	13	32
Logic elements by mode		
Normal mode	574	1480
Arithmetic mode	1189	4024
Total registers	331/8,256 (4%)	536/8,256 (6%)
Total LABs	158/516(30%)	452/516 (87%)
Total pins	9/85 (10%)	9/85 (10%)
M4Ks	2/36 (5%)	2/36 (5%)
Total memory bits	5,120/165,888 (3%)	5,120/165,888 (3%)
Total RAM block bits	9,216/165,888 (5%)	9,216/165,888 (5%)
Embedded Multiplier 9-bit elements	36/36 (100%)	36/36 (100%)

Table 4: Resource utilization of the Simple Observer (SO) and Composite Observer (CO) using Quartus II tool.

	SO	CO
Family	Cyclone II	Cyclone II
Device	EP2C8T144C8	EP2C8T144C8
Total logic elements	265/8,256 (3%)	2,431/8,256 (29%)
Combinational with no register		
Combinational with a register	206	2167
Logic element usage by number of LUT inputs	59	264
4 input functions	0	6
3 input functions	240	2053
<=2 input functions	25	372
Combinational cells for routing	0	19
Logic elements by mode		
Normal mode	14	299
Arithmetic mode	251	2132
Total registers	59/8,256 (<1%)	264/8,256 (3%)
Total LABs	24/516 (4%)	207/516 (40%)
Embedded Multiplier 9-bit elements	16/36 (44%)	36/36 (100%)

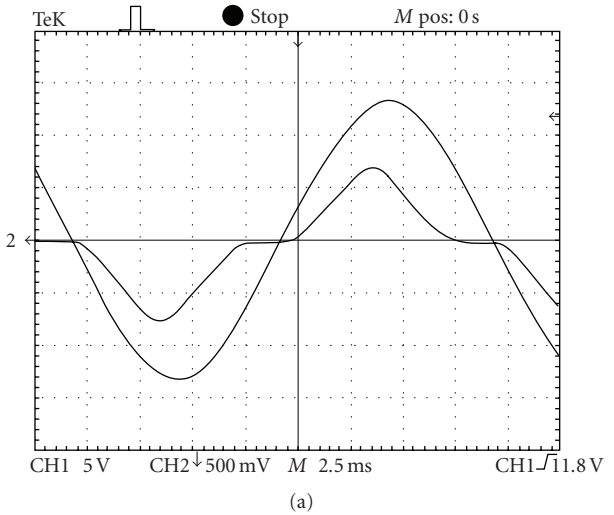


(a)

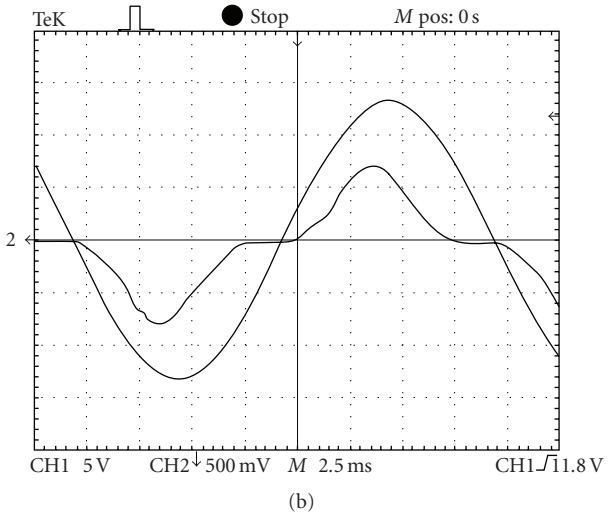


(b)

Figure 24: (a) Distorted output voltage waveform when a simple Voltage Observer and a simple Current Observer are used. (b) Distorted output voltage waveform when a Composite Voltage Observer and a simple Current Observer are used.



(a)



(b)

Figure 25: (a) Pure output voltage waveform when a Simple Voltage Observer and a simple Current Observer are used. (b) Pure output voltage waveform when a Composite Voltage Observer and a simple Current Observer are used.

6. Conclusion

The reduction of distortion in the voltage waveform in single phase Inverters, caused by the currents drawn by nonlinear loads, can be easily done by feeding back the instantaneous harmonic content of the voltage signal. This harmonic content is computed on-line by a composite observer in the voltage loop, which incidentally can also be used for obtaining the fundamental voltage signal for keeping the output voltage at the desired level. A simple Luenberger observer in the inner current loop serves the purpose of estimating the fundamental component of the load current, which is used for enhancing the stability of the overall scheme. Since the traditional trajectory control systems give rise to a steady-state error, the D-Q control procedure which is popular in 3-phase Inverters has been employed after suitable modifications for accurate voltage control of single-phase inverters. The local harmonic feedback gives rise to an enormous improvement in the quality of the waveform.

Interestingly the individual subblocks described in the work can be easily implemented in a Cyclone II FPGA, after trials in the Simulink environment. The composite observer has a parallel structure, which makes it desirable for implementation via the FPGA route. The digital multiply and add blocks were used for implementing the Park transform blocks. The various signals are almost simultaneously processed as if in an analog circuit, enabling a larger bandwidth for the control scheme. The total number of multipliers,

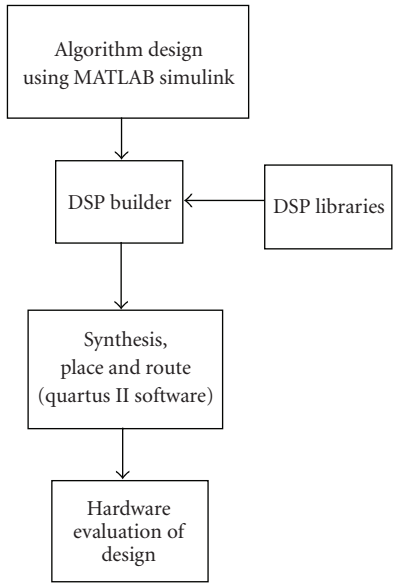


Figure 26: DSP Builder Design flow for Altera FPGAs.

adders, counters, integrators, and lookup tables was sufficient for implementing the inverter control system along with harmonic compensation procedure. Essentially, the harmonic distortion was cancelled by generating an equivalent opposing signal and adding it to the conventionally generated control signal within the FPGA. This procedure may be thought of as software-series compensation, which eliminates the need for external series transformers. It was found in the simulation and experimental studies that the composite observer shows a slightly faster response and purer output voltage waveform than a basic (simple) observer for the same feedback gain "h". Since the scheme works on the principle of "series software harmonic compensation," which is effectively carried out at the input terminal of the PWM block, a reduction in the maximum available sinusoidal peak voltage results. This is not a serious deficiency, since the output transformer turns ratio can be slightly increased, even at the design stage. Most importantly, the entire scheme could be embedded into a single cyclone FPGA Chip without any additional RAM elements. Some left over area in the FPGA can be used for protection of the Inverter under fault conditions.

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