# A Substrate Current Less Control Method for CMOS Integration of Power Bridges 

Joerg Krupar, Heiko Hauswald, and Ronny Naumann<br>DMOS GmbH, Bergstraße 4, 01069 Dresden, Germany<br>Correspondence should be addressed to Joerg Krupar, joerg.krupar@quickmos.com

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Modern electronical devices use high integration to decrease device size and cost and to increase reliability. More and more devices appear that integrate even power devices into VLSI circuits. When driving inductive loads, this is a critical step because freewheeling at a power device appears. In these applications usually special technologies with extra wells for the power devices, SOI technologies, or BiCMOS technologies are required to suppress any substrate current. However, the use of these technologies results in higher production cost for the device. We present a method to control the freewheeling actively. Using this approach we are able to integrate the power devices using a normal CMOS technology.

## 1. Introduction

Today nearly every technical product uses a controlled motor subsystem or at least an inductive actuator. Typical examples are as follows.
(i) Multimedia systems: CD-/DVD players use motors and actuators to drive the CD/DVD, to open and close the loader, or to focus the laser beam. Cameras have actuators and motors for autofocus, to open and close the lens protection or the flashlight.
(ii) Automotive applications: here motors are used to drive cooling fans and pumps but also to move seats, mirrors, or flaps. A modern car has typically between 70 and 100 electrical motors. The most of them are rather small.
(iii) Medical devices: small milling machines for the dentist, pumps, and so forth.
(iv) Toys: motors for movement.
(v) House control, heating control: open/close doors, windows, heating pumps, move flaps in the air conditioning system.

A lot of these motor/actuator systems are rather small. To decrease size and cost of these devices the integration
of the complete electronic subsystem is desired. However the integration of the power part for inductive loads is still a problem leading to significantly increased IC costs. Deactivation of a power device leads to freewheeling current. In normal CMOS technologies this freewheeling current results in substrate current. The substrate current can disturb the IC operation or even destroy the IC. To overcome this problem dedicated ICs use BiCMOS or SOI technologies or technologies with appropriated well in well devices for the power stage. Simple solutions also exist in CMOS technology. These are based on fixed timing with overlapped control signals for the power FET gates, and hence they drive significant cross current during the switching transitions [1]. The cross currents are much higher than the load current itself and result in loss of power efficiency, poor EME behaviour, and high current stress of the internal power devices. Depending on the current stress the high cross current can even result in reduced device reliability.

In the past different principles to control the body diode conduction time close to zero without introducing cross current were proposed.

The work in [2] presents a principle to control a FET like an ideal diode. In this proposal the delay errors are regulated to zero cycle-by-cycle by use of a PLL structure. The work in [3, 4] present similar cycle-by-cycle approaches for


Figure 1: Principle schematic of a half bridge driving an inductive load.


Figure 2: Principle schematic including parasitic devices of a CMOS process.
half bridges with a different current commutation detection and digital compensation of the delays. They provide faster settling to zero body diode conduction time.

However, all of these principles suffer from the same disadvantage: During the settling process the body diode conducts for a short time (Figure 3) and hence substrate current is introduced and causes uncontrolled behaviour of the IC and the timing control loop. Hence these principles are not appropriate for use with integrated power parts in standard CMOS technology.

In this paper we propose a method to control the freewheeling in the power devices actively during each edge beginning with the very first switching event. Using this method the duration of an inactive freewheeling period is reduced to less than 10 ns . This allows us to integrate the power devices in a standard CMOS technology without the need for high cross-currents in the power stage.

The method is based on the use of a fast and a slow control paths. The slow control path causes a switching transition duration of a few hundred nanoseconds. This transition duration is sufficient for motor drive applications. It may be too high for some DC-DC converter applications.

The paper is organised as follows. In Section 2 the freewheeling problem is discussed. From this discussion a substrate current free goal behaviour is derived in Section 3. In Section 4 a substrate current free power stage system for CMOS implementation is developed. Simulation results and a verification with fixed negative dead time are shown in Section 5. Section 6 draws conclusions.


Figure 3: Current commutation with deadtime.

## 2. Freewheeling in Power Circuits

Freewheeling occurs at every power stage that drives an inductive load. Figure 1 depicts a principal schematic of a half bridge driving an inductive load. The half bridge consists of two FETs including the corresponding bulk diodes. The load is modeled by $V_{1}, R_{1}$, and $L_{1}$. It can be, for example, a relay, an inductance of a DCDC converter or a terminal of a motor. The mean output voltage of the half bridge is

$$
\begin{equation*}
\overline{V_{O}}=\frac{t_{\mathrm{on}, M 1}}{T} \cdot V_{S} \tag{1}
\end{equation*}
$$

where $t_{\mathrm{on}, M_{1}}$ is the switch on duration of $M_{1}$ and $T$ is the duration of a switching period. For $\overline{\nu_{O}}>V_{1}$ freewheeling occurs at $M_{2}$ (sink mode). For $\overline{v_{O}}<V_{1}$ freewheeling occurs at $M_{1}$ (generator mode). Especially in motor applications both, the sink mode and the generator mode occur.

If no additional effort is spent, the freewheeling current is conducted by the bulk diode path. Its realisation depends on the IC processing. Figure 2 depicts a corresponding principle schematic for an n-well process. $T_{\mathrm{PP}}$ is the parasitic substrate transistor of the high side PMOS switch. $D_{\mathrm{PN}}$ is the parasitic substrate diode of the low side DMOS switch. When a freewheeling event at $M_{2}$ occurs, $D_{\text {PN }}$ injects a substrate current. For freewheeling events at $M_{1} T_{\mathrm{PP}}$ injects a substrate current. As can be seen in Figure 2 the $T_{\mathrm{PP}}$ substrate current leads to high power losses as the major part if it is driven to GND. Both substrate currents can disturb the function or even destroy the IC.

Two methods to overcome these problems are process modifications or a change in the control scheme of the power switches.

Process modifications consist either in the implantation of extra wells or in the use of an SOI process. The extra well collects the charge carriers instead of the substrate. The SOI process has no substrate current. Both modifications result in higher IC productions costs.

The change in the control scheme of the power switches (Figure 4) usually is the generation of overlapped control signals. The result of the overlapped control is a significant cross-current during each switching transfer resulting in oscillation due to parasitic inductances and poor EME behaviour. Significant cross current means that the cross current is much higher than the load current.

Hence a different solution is desired.


Figure 4: Current commutation with cross current.


Figure 5: Ideal current commutation without cross current and without deadtime.

## 3. Goal Behaviour

Figure 5 depicts the ideal switching transfer behaviour. In this picture the power devices are controlled so that the sum of the high side and low side power FET current exactly equal the load current. In this special case neither a body diode is conducting nor cross current is induced. The goal of the proposed method is to achieve a behaviour that is as close as possible to Figure 5.

The work in [4] proposes a digital control method to achieve this behaviour by measuring the body diode conduction time and compensating it out transition by transition. Unfortunately the method requires at least one switching transition with body diode conduction at the start of the system. As this single transition causes significant substrate current the method proposed in [4] is on one hand well suitable to applications with external power devices. On the other hand as a result of the substrate current during the initial switching transfer the method is not appropriated for the use with CMOS integrated power stages.

Here we use a different approach. The principle of the approach presented in this paper is to detect the conduction and freewheeling events in time during the transition and react immediately during each switching transition. The approach is presented in the next section.


Figure 6: Principle schematic of the analog part of the system.


Figure 7: Switch and current source with shared output devices.

## 4. System Description

4.1. Analog Subcircuit. Figure 6 depicts the principal schematic of the analog part of the IC. $M_{\mathrm{HS}}$ and $M_{\mathrm{LS}}$ are the integrated power FETs. The gates of them can be charged/discharged slowly by the current sources $I_{x S, \mathrm{ON}}$ and $I_{x S, O F F}$, respectively. $x$ stands for $H$ or $L$, respectively. Here slowly means a discharge time of a few hundred nanoseconds. Additionally the power devices gates can be fastly charged/discharged by the internal switches. $S_{x S, \mathrm{ON}}$ switches the corresponding driver on; $S_{\mathrm{HS}, \mathrm{PH}}$ switches the high side (HS-) driver or low side (LS-) driver off.

The current sources and switches use shared output devices to save chip area. Figure 7 depicts a scheme of one combined current source/switch to ground. The current mirror is built using $M_{I}$ and $M_{O}$. The input signal Cs selects between current mirror mode and switch mode. For $C s=H$ the circuit operates as current mirror and for $C s=L$ it operates as switch. All current sources are made in the same manner.
$M_{x S, S}$ are current sense transistors. Together with $\mathrm{Co}_{x S, \mathrm{ON}}$ they build current mode comparators to detect the end of the conduction time of the corresponding power FET (conduction loss comparator). As a result of the integration the threshold voltages of the power FETs and the sense FETs match very good. As the power FET losses need to be sunk in the IC package the internal power FETs are rather large to reduce conduction losses.


Figure 8: State machine.

Hence the effective $V_{\mathrm{GS}}$ of these devices is rather small. As a result even with a fixed threshold of the sense comparator the point of conduction loss is hit very good. Hence the fixed threshold can be used to control the commutation transfer. $C o_{x S, F R W}$ detects at which driver the freewheeling occurs. Its threshold is in the range of a few millivolts to detect the freewheeling path also at the active device (when no freewheeling occurs). Depending on the freewheeling path different sequences are processed during the switching transition. Additionally the comparators $\mathrm{Co}_{x \mathrm{~S}, \mathrm{PH}}$ are required to detect conduction loss at high load current. In the next section the different behaviour of the two kinds of conduction loss comparators will be explained more in detail.
4.2. State Machine. To handle the very low transfer times correctly the state machine has to be realised asynchronously. Figure 8 depicts the state machine. To keep the picture compact we use the following spelling.
(i) We do not distinguish between HS and LS switch. We separate a master power switch $(M)$ and a slave power
switch ( $S$ ). The master is the switch to be activated and the slave is the switch to be deactivated. If the tristate is to be activated the master switch is the switch that remains off the slave is the one that is to be switched off.
Using this simplification the number of states can be reduced by $50 \%$.
(ii) The states include only the active control signals for the drivers.
(iii) In the states the first letter separates master and slave, the second letter separates hard switch $(S)$ and current source ( $I$ ) and the rest is the switch/current source direction (on or off).
(iv) The signals at the state transfers are control signals and comparator signals. Control signals are the switch on and off signals of the master and slave, respectively ( $M$ on, $M$ off, $S$ off). Comparator signals are the freewheeling comparator output FRW, $x$, the current comparator on detection $\mathrm{ON}, x$ and the phase comparator output PH, $x$.


Figure 9: Switching transfer from high side to low side, fixed zero dead time.

The state transfer marked with "start" is the state initialisation after power up. When the IC is active the initial state is either state 8 (one driver is active) or state 10 (half bridge is in tristate). A switch on transfer always ends in state 8. A transfer to tristate mode always ends with state 10.

The transfer from one active driver to the other is as follows; Before each switching transfer the freewheeling direction is detected. Every transfer starts by swapping master and slave, state 1 .

Then the gate of the slave is discharged with constant current until its threshold is reached. If the freewheeling occurs at the slave device at the same time the master gate is charged by constant current, state 2 . When both power devices reached their thresholds (states $5,6,7$ ) the master gate is clamped on and the slave gate is clamped off, state 8 . This is the final state of the switching transfer.

The use of the different kinds of conduction loss comparators depends on the side at which the freewheeling current occurs. If the freewheeling occurs at the master device the master device remains off until the phase voltage begins to change. The beginning of the phase voltage change depends on the load current and starts earlier than the reaction of the $\mathrm{Co}_{x \varsigma, \mathrm{ON}}$ comparator. To prevent substrate current at the master device it is switched on as soon as the phase voltage begins to change, state 8. If the freewheeling occurs at the slave side the reaction of $\mathrm{Co}_{x S, \mathrm{ON}}$ is earlier than that of $C o_{x S, \mathrm{PH}}$ hence in these cases $C o_{x S, \mathrm{ON}}$ should be used for timing reasons.

When transferring to the tristate also depending on the direction of the freewheeling either the slave stays active or a transfer to active master is initiated, states 1 and 3, respectively. The corresponding device stays active until the freewheeling is finished. With the end of the freewheeling time the final state 10 is reached.

## 5. Simulation Results

The proposed analog and digital subsystems were implemented in a $0.35 \mu \mathrm{~m}$ high voltage CMOS technology with 40 V power devices. This section presents the simulation results of the proposed scheme. In the simulations two load currents have been used: a high load current of 2 A and a reduced load current of 400 mA .

For verification purposes Figure 9 depicts a simulation result of a classical approach. The simulation considers a bond wire inductance of 3 nH , uses zero dead time and a load current of 400 mA . In the figure HSON and LSON are the direct gate control signals of the HS and LS, switch respectively. During the commutation a significant crosscurrent of 12 A occurs that leads to gate voltage oscillations at the end of the commutation. To cover all process corners and temperature dependencies without substrate current the adjusted dead time would typically have a negative value resulting in an even higher cross-current.

All pictures in the sequel depict results of the implemented control approach. In all pictures the upper two

| 7 | + | + | + | + | + | + | + HSON |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| + | + | + | + | + | + | + | + LSON |
| XXS3 |  |  |  |  |  | S8 | FSM |




- $-\mathrm{VGS}_{\mathrm{HS}}$

$-\mathrm{ID}_{\mathrm{HS}}$
$\cdots \cdot \mathrm{ID}_{\mathrm{LS}}$

FIGURe 10: Switching transfer from high side to low side, freewheeling occurs at low side.

| + + | + | + | + | + | + | + |  | + | + |  |  | $+\mathrm{HSON}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\checkmark$ | + | + | + | + | + | + |  |  | + |  |  | + LSON |
| ] 5 | S5 |  |  |  |  |  |  |  |  |  | S8 | FSM |


$-V_{\mathrm{PH}}$



Figure 11: Switching transfer from high side to low side, freewheeling occurs at high side.


Figure 12: Switching transfer from high side to low side, reduced current, freewheeling occurs at low side.





- $\mathrm{VGS}_{\mathrm{HS}}$
-     -         - VGS $_{\text {LS }}$



Figure 13: Switching transfer from high side to low side, reduced current, freewheeling occurs at high side.





- $\mathrm{ID}_{\mathrm{HS}}$
$\mathrm{ID}_{\mathrm{LS}}$

Figure 14: Switching transfer from low side to high side, freewheeling occurs at high side.

$$
\begin{aligned}
& \text { - - - } \text { VGS }_{\text {LS }}
\end{aligned}
$$

$$
\begin{aligned}
& \text {--- } \text { ID }_{\text {HS }} \\
& \text {-.-. } \mathrm{ID}_{\mathrm{LS}}
\end{aligned}
$$

Figure 15: Switching transfer from low side to high side, freewheeling occurs at low side.


$-V_{\mathrm{PH}}$




$$
-\mathrm{ID}_{\mathrm{HS}}
$$

$$
\mathrm{D}_{\mathrm{LS}}
$$

Figure 16: Switching transfer from low side to high side, reduced current, freewheeling occurs at high side.

$$
\begin{aligned}
& -V_{\mathrm{PH}}
\end{aligned}
$$

$$
\begin{aligned}
& \text { - } \mathrm{ID}_{\mathrm{HS}}
\end{aligned}
$$

Figure 17: Switching transfer from low side to high side, reduced current, freewheeling occurs at low side.


FIGURE 18: Switching from low side to high impedance, freewheeling occurs at high side.


Figure 19: Switching from low side to high impedance, freewheeling occurs at low side.
digital signals depict the input control signals of the system. In the state diagram a nonnamed state occurs within a very short time interval at the beginning of the switching sequence. This state is state 1 . The analog signals depict phase voltage, gate source voltages of the power devices and the power device currents.

Figure 10 depicts the switching transfer from high side to low side with freewheeling at the low side. Within the first 500 ns the HS power gate is discharged until the phase voltage changes. As soon as the phase comparator threshold is achieved, the transfer to the final switching state is initiated. The current conducts fastly from the HS device to the LS device. The duration of the phase voltage change is sufficient to charge the low side switch gate.

Figure 11 depicts the same switching transfer but with freewheeling at the high side. Here first both power device gates are charged/discharged to a threshold voltage $V_{c, x S}$, states 2 and 5 . This voltage is above the $V$ th of the power devices. $V_{c, x s}$ is a compromise between substrate current and cross current. $V_{c, x S}$ is designed to drive approximately half of the maximum load current with the power device. A lower value leads to substrate current and a higher value leads to an increased cross current. After both $V_{c, x s}$ values have been reached, state 7 is activated for a short constant time interval. This intermediate state is used to prevent high cross currents when transferring from state 5 to the final state 8 .

At reduced load current the HS to LS transfer with freewheeling at the low side is identically to that of the high load current case, Figure 12.

Freewheeling at the high side, Figure 13 leads to identical cross currents independently from the load current. Hence for the reduced load current case in Figure 13 the cross current is higher than the load current.

The transfer from low side to high side is complementary to the switching from high side to low side, Figures 14, 15, 16 , and 17.

Figure 18 depicts the transfer from low side to high impedance with freewheeling at the high side. Here the automaton first initiates a transfer from low side to the high side to conduct the freewheeling current, states 3 and 1 . As soon as the freewheeling current vanishes the high side switch gate is discharged, state 4 , and the final state 10 is achieved.

A transfer from low side to high impedance is depicted in Figure 19. The low side switch conducts the freewheeling current until it vanishes. As soon as the freewheeling current vanishes the high side switch gate is discharged, state 4 , and the final state 10 is achieved.

## 6. Conclusion

The paper proposed a concept to implement power drivers for inductive loads into standard CMOS processes. Implementations of the analog and the digital subsystems are presented. The systems were implemented and simulated using a 0.35 um 40 V high voltage CMOS process. The proposed system actively conducts any freewheeling currents and does not suffer from high cross currents as constant
dead time approaches do. For further reduction of the cross currents at low load currents further investigations will be done.

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