Hindawi Publishing Corporation
Advances in Power Electronics
Volume 2011, Article ID 164286, 6 pages
doi:10.1155/2011/164286

Research Article

Heat Transfer of DE-Series MOSFETs

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Received 19 January 2011; Accepted 6 May 2011

Academic Editor: Jose Pomilio

MOSFET devices have developed significantly over the past few years to become the number one choice for high-power applications in power electronics and electronic communication. Commercially available devices (such as the IXYS RF manufactured) now operate into the VHF range with output RF powers of up to 300 W. They are optimized for linear operation and suitable for broadcast and communication applications. This paper presents the heat transfer out of an IXZ210N50L MOSFET which is sandwiched between two identical heatsinks. The results reveal a linear decrease in heat flowing away from the top of the MOSFET when compared to the bottom of the MOSFET for each step increase of drain current. Two graphs (representing the top and bottom heatsinks connected to the MOSFET device) contrast the temperature rise for the Bisink technique when the drain current through the IXZ210N50L MOSFET is kept constant at 5 A. The Bisink technique has the advantages of lower on-state resistances and higher output powers when compared to the traditional mounting using only one heatsink, resulting in improved reliability and performance. Results further reveal that the ambient temperature must be measured in the vicinity of the heatsink.

1. Introduction

A metal-oxide-semiconductor field-effective transistor (MOSFET) originates when a metal plate is separated from the semiconductor channel by an oxide dielectric. The semiconductor channel is then controlled by an electric field which is applied to the isolated metal gate. These semiconductor devices have been housed in a variety of packages depending on the frequency and power requirements. Typical packages include the DPAK, SO-8, CopperStrap SO-8, PowerPak, LFPAK, DirectFET, iPOWIR, TO-3, TO-220, TO-247, and the most recent DE-Series from the IXYS Corporation [1, 2]. DE-Series packages were designed to overcome the various parasitic elements that inhibit high-speed operation and addresses the need for a true low-inductance, high-speed, and high-power device.

Any electronic circuit consumes electric power because it contains components that convert electricity into other forms of energy, such as heat [3]. Heat is produced when power is dissipated at the silicon level and is generally dominated by the conduction loss caused by the drain current and on-state resistance of the device [4]. How does the on-state resistance of the DE-Series IXZ210N50L MOSFET change with different load currents? And what percentage of the total heat flows out through the top and bottom of the MOSFET device? These questions are important as they influence the amount of current which may be successfully switched through the MOSFET. Ensuring a lower on-state resistance and a better flow of heat away from the junction will ensure the reliability and performance of the MOSFET as a switching device.

The thermal design or layout of the MOSFET is based upon the resistive model of thermal conduction in a power device and associated components. This will firstly be reviewed. A brief comparison of two recognized mounting techniques will then be given to substantiate the use of the Bisink approach. A new connotation for ambient temperature is provided along with relevant equations. Results of on-state resistance change and heat flow ratios from the MOSFET device are given in graph form.

2. Thermal Conduction in a Power Device and Associated Components

The resistive model is depicted in Figure 1, showing three thermal resistances (θ_{JC}, θ_{CS}, θ_{SA}), power dissipation (P_D),

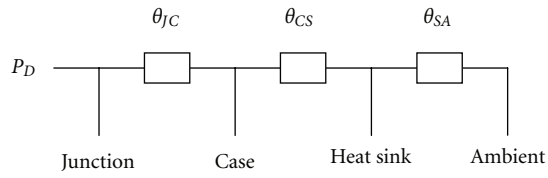

Figure 1: Resistive model of thermal conduction.

and various temperatures (Junction, Case, Heatsink, Ambient).

The mathematical expression governing the junction temperature (t_J) may be written as [5–9]

$$t_J = P_D \times (\theta_{JC} + \theta_{CS} + \theta_{SA}) + t_A \quad (^\circ\text{C}), \tag{1}$$

where P_D: power dissipated by the device in Watt; θ_{JC}: the junction-to-case thermal resistance in degrees Celsius per Watt; θ_{CS}: the case-to-heatsink thermal resistance in degrees Celsius per Watt; θ_{SA}: the heatsink-to-air thermal resistance in degrees Celsius per Watt; t_A: ambient temperature in degrees Celsius.

The total power dissipation (P_D) is usually the sum of the following losses [4]:

(i) switching transition power loss;

(ii) off-state leakage power loss;

(iii) conduction power loss;

(iv) drive input device power loss.

The first step in the thermal design or layout is to determine the total power dissipated in the device, which is generally dominated by the conduction loss (P_C) which is mathematically calculated with the following equation [4]:

$$P_C = {I_{D(\text{rms})}}^2 \times R_{DS(\text{on})} \quad (\text{W}), \tag{2}$$

where P_C: conduction power loss in Watt; $I_{D(\text{rms})}$: drain current in Ampere; $R_{DS(\text{on})}$: on-state resistance of the device in Ohm.

Power dissipation is allowed to flow out of the device in the form of heat, thereby raising the internal temperature and affecting the performance and reliability of the semiconductor device [10]. Junction temperature rise subsequently indicating an increase in power dissipation as the following equation shows [4]:

$$P_D = \frac{t_J - t_C}{\theta_{JC}} \quad (\text{W}), \tag{3}$$

where t_C: the case temperature in degrees Celsius

Certain characteristics of the devices are also modified as the junction temperature increases which include the on-state resistance ($R_{DS(\text{on})}$) governed by the following equation [10]:

$$R_{DS(\text{on})}(T_J) = R_{DS(\text{on})}(25^\circ\text{C}) \times \left(\frac{T_J}{300}\right)^{2.3} \quad (\Omega), \tag{4}$$

where T_J: the junction temperature in Kelvin.

The following factors have led to establishing a temperature limit of 200°C for the junction of solid state devices to ensure good reliability and performance [5].

(i) It is well below the temperature at which silicon becomes intrinsic.

(ii) Diffusion currents in silicon die begin to increase rapidly above 200°C.

(iii) Metal migration increases rapidly above 200°C.

(iv) It appears to be a realistic temperature consistent with thermal resistances and power dissipation needed in high-power RF devices.

Swart and Pienaar [11] provided the following equation for calculating the on-state resistance for different drain current values:

$$R_{DS(\text{on})} = \frac{t_S - t_A}{{I_{D(\text{rms})}}^2 \times \theta_{SA}} \quad (\Omega). \tag{5}$$

The heatsink temperature directly above or below the MOSFET device needs to be measured, along with the ambient temperature. The heatsink-to-air thermal resistance also needs to be known, which may be determined in the following way. The IXZ210N50L MOSFET device has a maximum allowable junction temperature of 175°C, while its junction-to-case thermal resistance is 0.32°C/W [12]. The maximum allowable drain current is 10 A with a typical on-state resistance of 1 Ω resulting in a maximum power dissipation of 100 W. The resistance of the mounting interface between the case and the heatsink may be assumed to be 0.05°C/W when using a RS heatsink compound (stock number 554–311) [13]. Maximum ambient temperature will be approximately 26.6°C. Manipulating (1) to give the heatsink-to-air thermal resistance yields the following:

$$\theta_{SA} = \frac{t_J - t_A}{P_D} - \theta_{JC} - \theta_{CS} \quad (^\circ\text{C/W}), \tag{6}$$

$$\begin{aligned} \theta_{SA} &= \frac{175 - 26.6}{100} - 0.32 - 0.05, \\ \theta_{SA} &= 1.114 \quad (^\circ\text{C/W}). \end{aligned} \tag{7}$$

The RS International Electronic Catalogue lists numerous heatsinks with their relevant thermal resistances. One of these heatsinks (stock code 271–864) has a thermal resistance of 1°C/W [13]. It is 100 mm long, 120 mm wide, and 37 mm high with 10 protruding fins. This heatsink will suffice when the MOSFET exhibits a power dissipation of 100 W and will therefore be used in this study.

3. The Bisink Technique

The Bisink technique involves sandwiching the MOSFET device between two different heatsinks of the same type, as shown in Figure 2. This requires the use of two 2 mm bolts to secure the PCB to the one heatsink, thereby ensuring a secure mounting with little stress to the MOSFETs leads. Two 6 mm bolts are used to clamp the two heatsink together, one on the top of the MOSFET and the other on the bottom of the device (being the isolated substrate). Research done by Swart and Pienaar [11] proved that using two heatsinks, instead of just one, ensures a lower on-state resistance

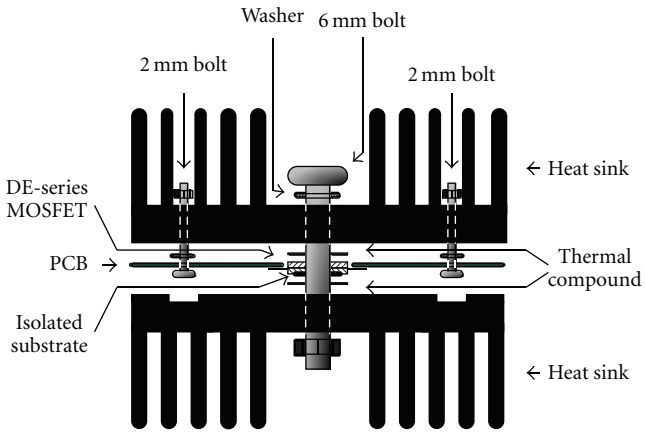

Figure 2: Bisink technique for mounting MOSFETS using two heatsinks.

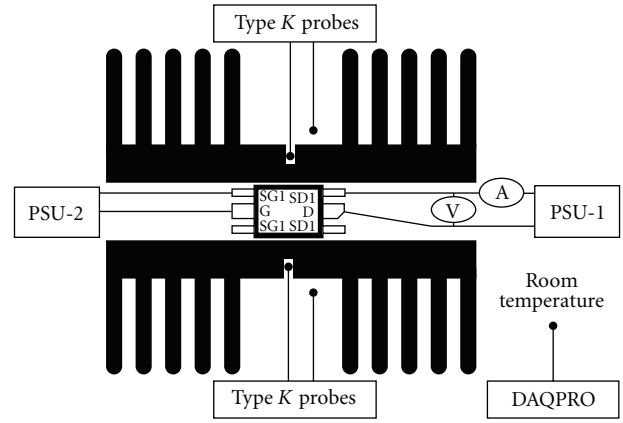

Figure 3: Practical setup of the equipment.

and a corresponding lower power dissipation within the MOSFET device. Subsequently, higher output powers are achievable with this technique.

4. Determining Power Dissipation in the Semiconductor Device

The junction temperature of MOSFET devices tend to rise when the drain current increases. This in turn increases the on-state resistance and the power dissipation within the device. It is therefore imperative to determine by how much the on-state resistance changes, as this will increase the power dissipation and affect the power delivered to the load.

The change in on-state resistance may be determined using (5), which requires knowing the heatsink temperature and ambient temperature for each discrete step in drain current increase. The change in temperature was measured with the DAQPRO 5300 Data Logger using two Type-K thermocouples. The K-thermocouple is the most commonly used base metal type with a specified operating temperature range of −250°C to 1200°C, a resolution of 0.1°C and an accuracy of approximately 0.5% [14]. The tip of one thermocouple is imbedded 2 mm into the heatsink just below the MOSFET, while the other thermocouple is positioned approximately 1 cm away from the heatsink to measure the ambient temperature in the vicinity of the heatsink, a method substantiated by a number of research articles [15–17].

It is important to remember that the thermal analysis of fin heatsinks often involves a combination of the three modes of heat transfer, being conduction, convection, and radiation. Some researchers do not recognize the significance of thermal radiation, but consider only natural convection in their analysis [18–20]. This might not be reasonable under certain circumstances [16]. Examples where thermal radiation and view factors need to be considered include heatsinks with low air velocities or heatsinks mounted on hot surfaces [21]. None of these factors exist in the current experimental setup, shown in Figure 3. Moreover, excluding thermal radiation effects in the analysis of fin arrays might also be attributable to the difficulty faced in determining the radiation view factor and emissivity [21]. The view factor accounts for the shielding effect induced in fin arrays, where the view of both adjacent fins and supporting base to the ambient (to which the radiation heat exchanges) are obstructed by the particular fin itself. The effects of thermal radiation are therefore not considered in this setup in order to simplify analysis.

The first power supply (PSU-1) was used to control the drain current through the MOSFET device while the second power supply (PSU-2) was used to keep the MOSFET on by supplying a 12 V DC gate voltage. Test procedures for component characterisation generally use steady-state DC current to heat the semiconductor device [22]. Sufficient time (approximately 20 minutes) was allowed after each drain current increase to allow the heatsink temperature to stabilize. Room temperature was kept constant at 24.6°C.

Using (5) with the measured values shown in Table 1 (t_A measured 1 cm from the heatsink and t_S measured 2 mm into the heatsink just below the MOSFET) yields the calculated on-state resistances shown in column two. The heatsink-to-air thermal resistance is 1°C/W.

Using these calculated on-state resistances with (2) results in the power dissipation (P_DA) shown in column three.

The drain current and drain source voltage (measured with the Ammeter and Voltmeter in Figure 3) is used with the following equation to calculate the second power dissipation (P_DB) shown in column seven:

$$P_DB = I_{D(\text{rms})} \times V_{DS} \quad (\text{W}). \tag{8}$$

The percentage difference between the two power dissipations (P_DA and P_DB) is less than 8% when using a changing ambient temperature measured 1 cm away from the heatsink. The on-state resistance also remains within touch of 1 Ω, which is the datasheet value for the IXZ210N50L MOSFET [12]. On the other hand, the percentage difference between P_DA and P_DB varies greatly (up to 234%) as well as the on-state resistance (up to 2.62 Ω) when a constant ambient temperature is used. This suggests that the ambient temperature should be measured in the immediate vicinity of

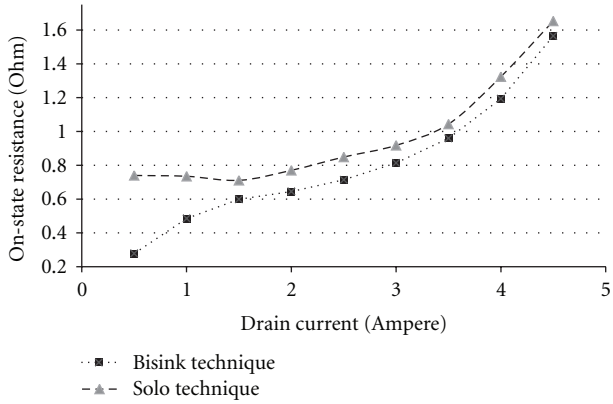

Figure 4: On-state resistance change versus drain current increase for the Bisink and Solo techniques.

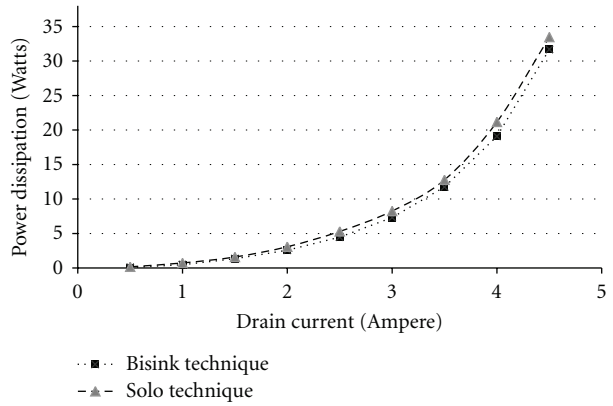

Figure 5: Power dissipation increase for specified drain currents when using two heatsinks (Bisink Technique) and one heatsink (Solo Technique).

the heatsink, being considered as a varying temperature and not a constant.

Figure 4 depicts the change in on-state resistance (values from Table 1) for various drain currents when using a single heatsink (Solo technique shown with a triangle) and the double heatsink (Bisink technique shown with a square) (adapted from Swart and Pienaar [11]).

A drain current of 5 A resulted in the heatsink temperature increasing dramatically when using the single heatsink, indicating no signs of temperature stabilization. A maximum drain current of 4.5 A was therefore chosen to ensure temperature stabilization on the single heatsink. Figure 5 presents a comparison between the two stated techniques with regard to power dissipation increase for specified drain currents, where the values in column three of Table 1 are used based on (2). Figure 6 presents the junction temperature increase for the two techniques. These measurements were recorded after temperature stabilization was achieved (roughly 20 minutes after each drain current step increase). It is clearly discernable that a lower power dissipation results when using the Bisink technique (Figure 5) which subsequently gives a lower junction temperature (Figure 6).

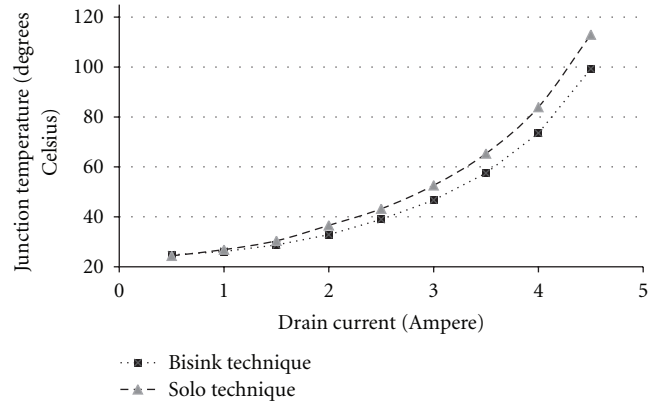

Figure 6: Comparison between the Bisink Technique and the Solo Technique with regard to junction temperature increase for specified drain current settings.

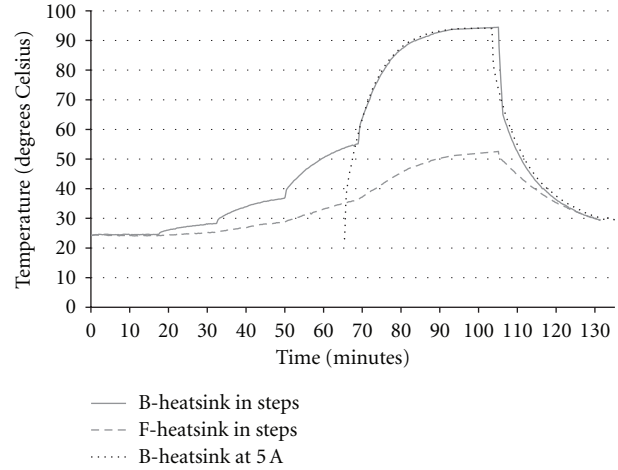

Figure 7: Bottom and top heatsink temperatures for the MOSFET using the Bisink technique.

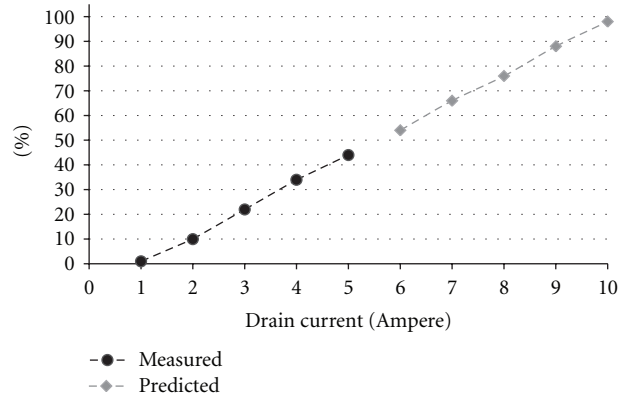

Figure 8: Measured and predicted values for the percentage difference between the temperatures on the bottom of the MOSFET as compared to the top when using the Bisink technique.

Table 1: Measured values to calculate power dissipation.

Drain current $I_{D(\text{rms})}$ (A)	On-state resistance $R_{DS(\text{on})}$ (Ω)	First power dissipation P_DA (W)	Ambient temperature t_A (°C)	Heatsink temperature t_S (°C)	Drain source voltage V_{DS} (V)	Second power dissipation P_DB (W)	Percentage difference (%)
Changing ambient temperature							
1.00	0.40	**0.40**	25.4	25.8	0.40	**0.40**	0%
2.00	0.65	**2.60**	29.3	31.9	1.37	**2.74**	−5%
3.00	0.88	**7.90**	36.5	44.4	2.79	**8.38**	6%
4.00	1.27	**20.30**	46.8	67.1	5.51	**22.03**	8%
Constant ambient temperature							
1.00	1.34	**1.34**	24.6	25.9	0.40	**0.40**	−234%
2.00	1.83	**7.30**	24.6	31.9	1.37	**2.74**	167%
3.00	2.16	**19.41**	24.6	44.0	2.79	**8.38**	132%
4.00	2.62	**41.89**	24.6	66.5	5.51	**22.03**	90%

Figure 7 illustrates the heatsink temperature change with each step in drain current. The temperature for the bottom of the MOSFET (B-heatsink in steps) is depicted with a solid grey line, while the top of the heatsink (F-heatsink in steps) is shown by means of a slotted grey line. Temperature stabilization was achieved beyond 4.5 A with the Bisink technique, and therefore the current was adjusted in 1 A steps to a maximum of 5 A. The black dotted line represents the temperature measured on the bottom of the heatsink (B-heatsink at 5 A) for a constant 5 A drain current. Temperature stabilization is visible between 90 and 105 minutes, where the heatsink temperature tappers off to around 94°C. It is further evident from Figure 7 that more heat is released from the bottom of the MOSFET (B-heatsink in steps) when compared to the top (F-heatsink in steps). This substantiates that the metal substrate is directly connected to the semiconductor die or junction, thereby facilitating a better flow of heat out from the MOSFET device [2]. Figure 7 also indicates that the MOSFET device is operating consistently, as the step approach with the drain currents leading to the 5 A curve (from 65 minutes to 130 minutes) is similar to the curve for a constant drain current of 5 A (B-Heatsink at 5 A).

Figure 8 presents a linear graph of the percentage difference between temperatures measured on the bottom heatsink (connected to the isolated substrate of the MOSFET) as compared to the top heatsink (connected to the top of the MOSFET). In other words, if 50°C is measured on the bottom heatsink for a drain current of 4 A, then the top heatsink will have a temperature difference of 35%, or a temperature 65% lower than 50°C, being 32.5°C. This linear curve increases with an increase of drain current, meaning that the higher the drain current the higher the percentage difference between the temperatures on the bottom of the MOSFET as compared to the top of it. This curve further points to a maximum percentage difference of 100% at 10 A, which is also the maximum rated drain current for this MOSFET device [12]. Using the Bisink technique with the practical setup discussed above may be another approach in determining the maximum allowable drain current for MOSFET devices. Further research on other MOSFET or semiconductor devices may collaborate this.

5. Conclusions

Figure 4 indicated the results which were obtained for the Solo technique and the Bisink technique. It indicated that the on-state resistance increases as the drain current rises, as more power is dissipated at the silicon level (see Figure 5). The values of on-state resistance remain though very close to the typical on-state resistance of 1 Ω as specified in the manufacturer data sheet. This is though achieved only when the ambient temperature is measured in the immediate vicinity of the heatsink (being 1 cm away from the heatsink in this research), being considered as a changing value instead of a constant. However, will similar results be obtained by using a larger gap (e.g., 2-3 cm) or by placing the thermocouple between certain fins of the heat sink? This question necessitates additional research.

Figure 6 reveals the junction temperature rise for the different drain currents, with a temperature of 100°C being recorded for a drain current of 4.5 A. Manufacturer specifications for the IXZ210N50L MOSFET allow for a maximum junction temperature of 175°C, which indicates that this MOSFET device can still handle higher drain currents with the use of the Bisink technique.

Figure 7 illustrated the temperature difference between the bottom heatsink (connected to the isolated substrate of the MOSFET) and the top heatsink (connected to the top of the MOSFET which shows the part number). This temperature difference increases linearly with drain current increase (see Figure 8).

It is not advisable to use the printed circuit board as a heatsink for the semiconductor device even if it may seem like a cheap and easy way to provide heat transfer. As it heats up, most printed circuit board materials expand seven times more in thickness than it does in the plane of the surface. A great deal of force is therefore exerted on the leads and solders joints of the MOSFET device, which could result in breakage or dry joints. It is therefore suggested that the

Bisink technique be used for high power applications, as the MOSFET device will not be in direct contact with the printed circuit board. This technique will further enable the MOSFET device to have a lower junction temperature, being able to deliver higher levels of RF power to the load. Ensuring a lower on-state resistance and a better flow of heat away from the junction will ensure the reliability and performance of the MOSFET as a switching device.

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