

Research Article

Flash FPGA-Based Numerical Pulse-Width Modulator

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A pulse-width modulator to drive three-phase AC motors is described. It performs a numerical modulation technique, also known as optimum or calculated modulation, but, in order to reduce hardware resources, a hybrid approach merging that calculated modulation with proportional modulation is proposed. The modulator is tested in a flash-based field programmable gate array (FPGA) implementation.

1. Introduction

The pulse-width modulation technique is a well-established method of control in motor drives and power converters. PWM has a lot of variations based upon the load type, the power level, and the semiconductor devices used in the converters [1–3].

Microcontrollers, microprocessors, programmable logic, DSPs (digital signal processors), and FPGAs have evolved to attain the ever complex control strategies required to achieve more performance at a lower cost. Modern microcontrollers with three PWMs included are not uncommon nowadays, and FPGAs with embedded 32-bit processors are a fact.

This scenario has made digital PWM (DPWM) a ubiquitous method of power management, ranging from hundreds of megawatts systems to submilliwatts on-chip voltage regulation modules (VRMs) [4].

This work presents a PWM modulator suitable for AC motor speed control and uninterruptible power sources (UPSs), but since the first application poses an additional problem, namely, the voltage resolution, it is described for such a load.

In [5] it is stated the high-frequency PWM generation and resolution trade-off. Two solutions are reported in [6, 7] that increase the effective resolution at expenses of additional subharmonic noise to the PWM spectrum.

It is proposed a different way to enhance the resolution at expenses of noise added in the upper side of the spectrum where filtering is less expensive.

The modulator has been tested using a flash-based field-programmable gate array (FPGA) [8], and block diagrams of the implementation are given.

2. Optimum Modulation

2.1. Ideal Solution. Aiming to improve the dynamic performance of the closed loop control system, an optimum three-phase pulse-width modulator is implemented in order to reduce the closed loop delay.

Other goals of the modulation technique are to reduce the amplitude of the harmonics close to the fundamental while keeping its implementation simple.

In this “optimum” modulator three independent angles were considered. The half cycle of a waveform of this type of modulation is shown in Figure 1, where E is the DC voltage applied to the motor and θ_1 , θ_2 , and θ_3 are the three angles that specify a quarter period of the waveform. The waveform is extended to a complete period adding odd and shift symmetries.

The Fourier series of the waveform gives (1) as the expression of the peak-voltage amplitude of the harmonic of order n :

$$V_n = \frac{8E}{n\pi} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) - 0.5). \quad (1)$$

The ratio between the peak voltage of the fundamental V_1 and the DC voltage E is the modulation, that is,

$$m = \frac{V_1}{E}. \quad (2)$$

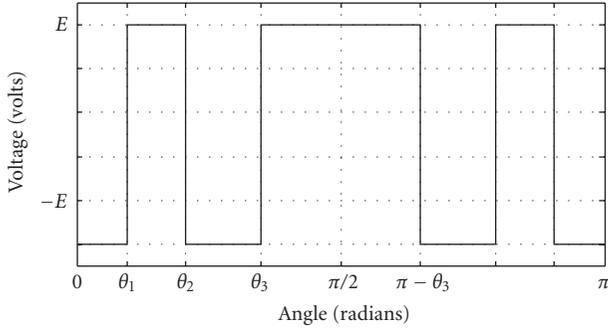


FIGURE 1: Half cycle of an optimum modulation waveform with three independent angles.

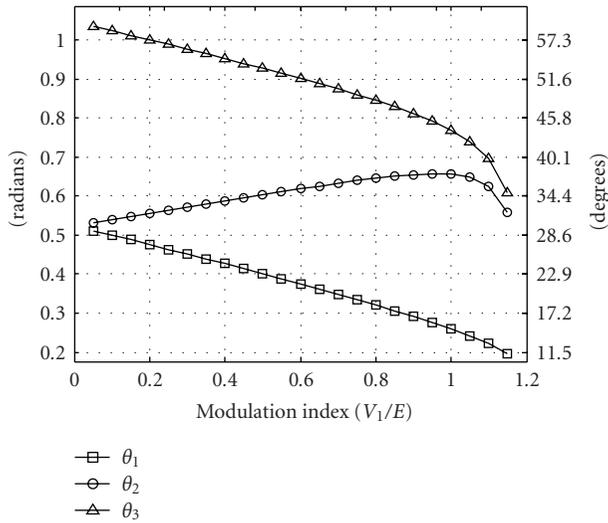


FIGURE 2: Angles for 5% steps of voltage amplitude variations.

To obtain the values of the three independent angles it is sufficient to fix the value of the peak voltage of the fundamental V_1 and to force the next two higher harmonics to become negligible. Assuming symmetrical source and balanced load the third-order harmonics form a homopolar system. Then without neutral wire, this harmonic system is forced null. Moreover, harmonics 5th and 7th are equated to zero. These restrictions are summarized in the following:

$$\begin{aligned}
 m &= \frac{8}{\pi} \left(\cos \theta_1 + \cos \theta_2 + \cos \theta_3 - \frac{1}{2} \right), \\
 0 &= \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) - \frac{1}{2}, \\
 0 &= \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) - \frac{1}{2}.
 \end{aligned} \quad (3)$$

For every index modulation value m a set of three angles can be found as long as $0 < \theta_1 < \theta_2 < \theta_3 < \pi/2$.

There are different approaches [9–13] to solve the set of (3).

2.2. Discrete Solution. To implement the PWM with a digital system such as an FPGA it is necessary to represent the angles

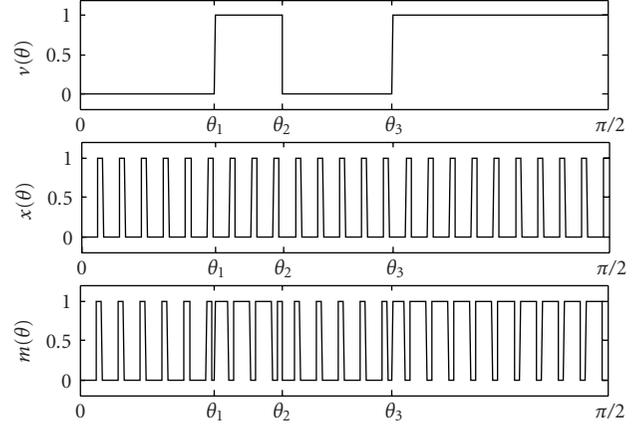


FIGURE 3: Optimum modulation waveform, $v(\theta)$, duty-variable signal $x(\theta)$, and XOR of both signals, $m(\theta)$.

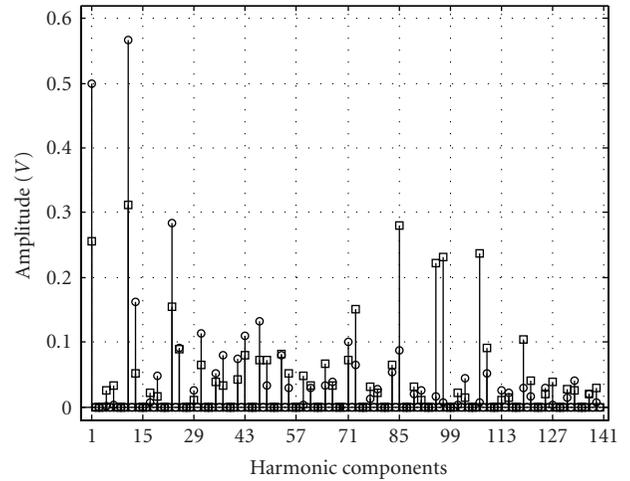


FIGURE 4: Optimum modulation spectrum: round markers, and chopped spectrum: squares markers.

of a particular solution with finite precision. Therefore the interval $[0, \pi/2]$ is partitioned in N even segments. As a consequence the approximated values of the angles are not an exact solution of (3), that is, harmonics 5th and 7th are not zero unless N is taken large enough, increasing the hardware requirements.

To choose a suitable value for N , the total harmonic distortion given by (4) (for pure inductive load) is calculated both for the true values of the angles and for the approximated values for different values of N :

$$\tau = \frac{1}{V_1} \sqrt{\sum_{i=5,7,11,\dots} V_i^2}. \quad (4)$$

Proceeding by this way when N equals 20 or more, the distortion values true and discrete differ only slightly. In this sense $N = 24$ is taken as a large enough number of segments into which $[0, \pi/2]$ is partitioned.

2.3. Amplitude Voltage Resolution. In applications of AC motor speed control a change in the machine velocity needs

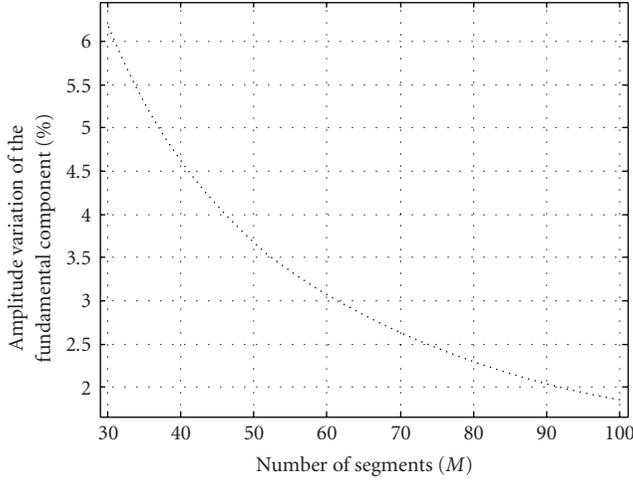


FIGURE 5: Amplitude resolution.

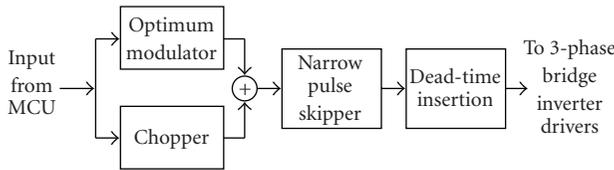


FIGURE 6: Block diagram of the system.

a proportional voltage change to keep the magnetic flux of the motor constant to prevent saturation.

It is usual to control the motor speed with a resolution of 5% or even more. Therefore to keep the flux constant, the modulator has to vary the amplitude of the fundamental in the same amount.

Figure 2 depicts the values of θ_1 , θ_2 , and θ_3 for modulation indexes ranging from 0.05 to 1.2, in 5% step increments.

It is clear that the three angles vary almost linearly except in the overmodulation range, and span $\Delta\theta_1 = 0.253$ rad, $\Delta\theta_2 = 0.125$ rad, and $\Delta\theta_3 = 0.267$ rad. Hence to vary the voltage amplitude in 5% steps it is necessary to change the angles at least in $0.125/32 = 0.004$ rad steps, that is, the interval $[0, \pi/2]$ should be partitioned in $N = 393$ steps or more to achieve a 5% of voltage amplitude resolution. This demands much more amount of hardware than the previously determined in Section 2.2. To avoid such an expensive solution a mixed modulation is proposed in the next section.

3. Optimum and Proportional Modulation

To enhance the resolution, a logical XOR operation between the original modulated signal and a high-frequency variable-duty signal was carried out. This resembles a proportional modulation in a chopper. Figure 3 illustrates this operation, where the optimum modulated signal, $v(\theta)$, is chopped with a high-frequency signal $x(\theta)$, while the outcoming, $m(\theta)$, is shown at the bottom of the figure. Only the first quarter of the waveform is shown.

Modifying the duty of $x(\theta)$ the amplitude of the fundamental component of $m(\theta)$ is modified. This is because the chopping diminishes the local average value, causing a fundamental amplitude reduction.

The coefficients of the Fourier series of the resultant signal $m(\theta)$ are expressed by

$$M_n = \frac{1}{\pi} \left[\int_{-\pi}^{\pi} [\overline{v(\theta) \oplus x(\theta)}] \cos(n\theta) d\theta + j \int_{-\pi}^{\pi} [\overline{v(\theta) \oplus x(\theta)}] \sin(n\theta) d\theta \right]. \quad (5)$$

To further simplify (5) one additional requirement on the chopper signal $x(\theta)$ is introduced forcing T_v (the period of $v(\theta)$) to be an integer multiplier of T_x (period of $x(\theta)$). This may be stated as

$$T_v = KT_x. \quad (6)$$

So (5) can be expressed as

$$M_n = \frac{2}{\pi} \left[\int_0^{\pi} [\overline{v(\theta) \oplus x(\theta)}] \cos(n\theta) d\theta + j \int_0^{\pi} [\overline{v(\theta) \oplus x(\theta)}] \sin(n\theta) d\theta \right]. \quad (7)$$

With this symmetry the value of the coefficients may be calculated considering that, in the interval $[0, \pi]$, the signal $m(\theta)$ is the logical difference between $v(\theta)$ and $x(\theta)$. This condition becomes clear from Figure 3.

Taking into consideration this operation the coefficients of $m(\theta)$ can be expressed with the following equations:

$$A_n = \frac{2}{\pi} \left[\int_0^{\pi} v(\theta) \oplus x(\theta) \sin(n\theta) d\theta \right], \quad (8)$$

$$B_n = \frac{2}{\pi} \left[\int_0^{\pi} v(\theta) \oplus x(\theta) \cos(n\theta) d\theta \right].$$

Figure 4 shows the spectral components of both signals $v(\theta)$ with round markers and $m(\theta)$ with square markers. It may be seen that the amplitude of fundamental component of $v(\theta)$ is two times the amplitude of the fundamental component of $m(\theta)$. Besides this, the operation applied before does not deteriorate the spectral characteristics of the modulated signal, specially in the low frequencies (harmonics close to the fundamental). In this way, the user could achieve the desired value of fundamental component without regenerating the previously eliminated harmonics.

In the figure the components near the 100th component became amplified, because the spectrum was periodized. Therefore, the components of $m(\theta)$ can be expressed as a periodization of the $v(\theta)$ components, with each period centered in the integer multipliers of $1/T_x$ (frequency of $x(\theta)$).

As it was mentioned before, modifying the duty cycle of $x(\theta)$ changes the amplitude of the fundamental component. For example, in Figure 3 a duty cycle equal to 25% was adopted yielding a decrement of 50% of the original amplitude.

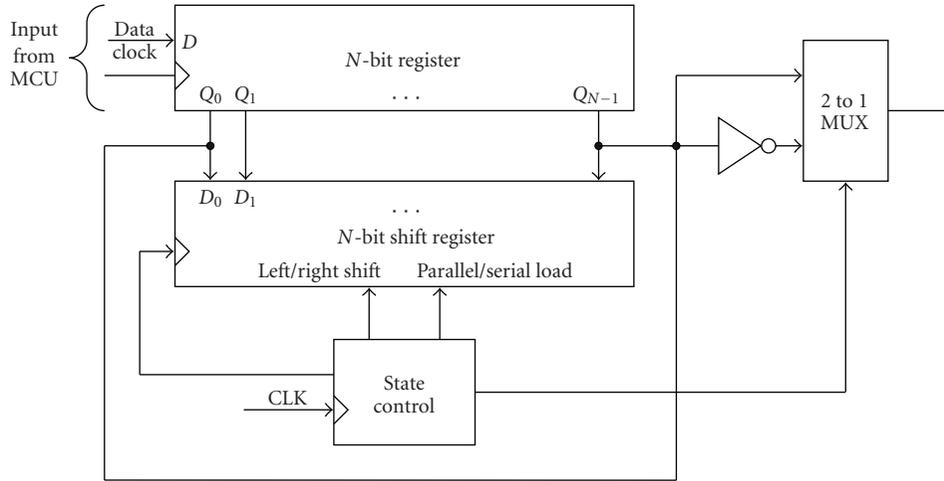


FIGURE 7: Optimum modulator block diagram.

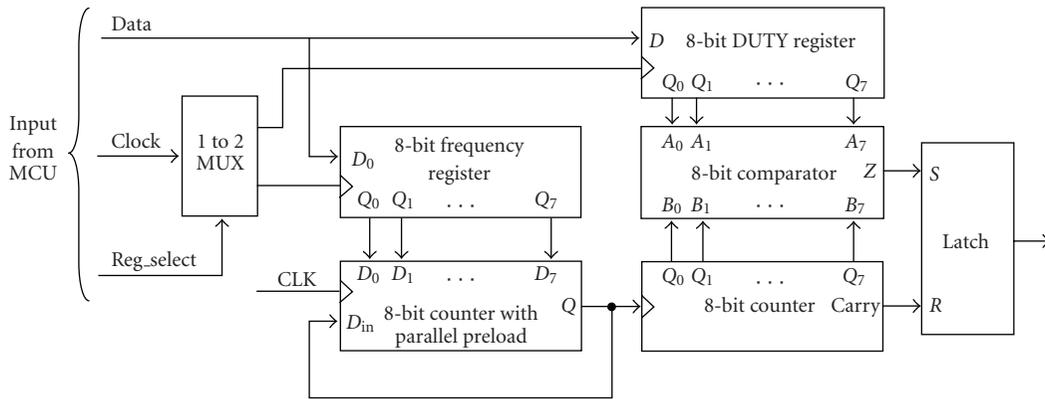


FIGURE 8: Chopper signal generator.

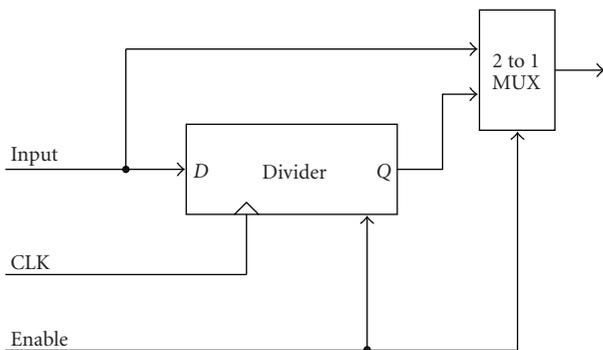


FIGURE 9: Narrow pulse skipper.

The duty cycle of $x(\theta)$ has to be less than 0.5 because, for this value, $m(\theta)$ becomes zero and further, for values beyond 0.5, $m(\theta)$ inverts its polarity.

Since the interval $[0, \pi/2]$ is partitioned into 24 slots and the XOR operation is essentially a multiplication of signals, while for a 5% in the amplitude resolution it is necessary 393

segments, $2 * (393/24) = 33$ segments are required to adjust the duty cycle.

Figure 5 shows simulation results for the degree of variation of the amplitude that can be achieved.

4. Physical Implementation

To prove the concepts of this work the system was implemented on a flash-based FPGA. The overall block diagram of the system is shown in Figure 6.

A microcontroller unit, or MCU, allows to load the proper parameters of the PWM modulator through a serial interface.

The optimum modulator is further detailed in Figure 7 and is loaded by the MCU with the desired $N = 24$ -bit modulation pattern into a register with serial input and parallel output. The 24-bit string represents a quarter or period of the full waveform and is loaded into a N -bit shift register. The state control block alternatively shifts the pattern to the left and then to the right to complete one half of the waveform. Thereafter the operation is repeated but passing the output D_{N-1} through an inverter.

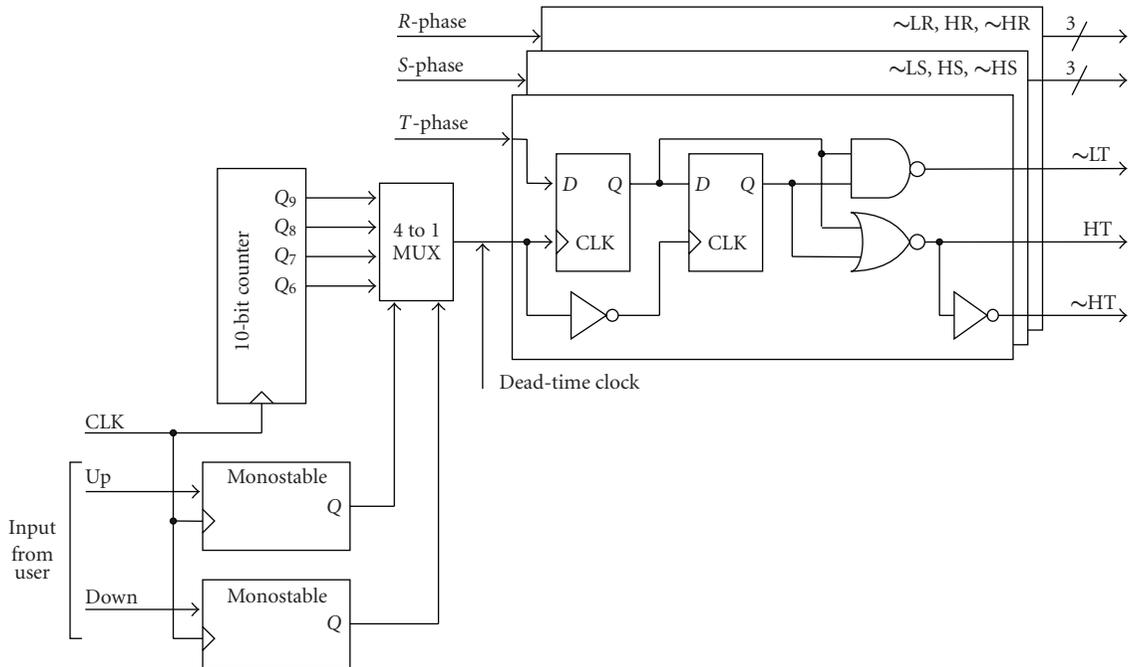


FIGURE 10: Dead-time insertion circuit.

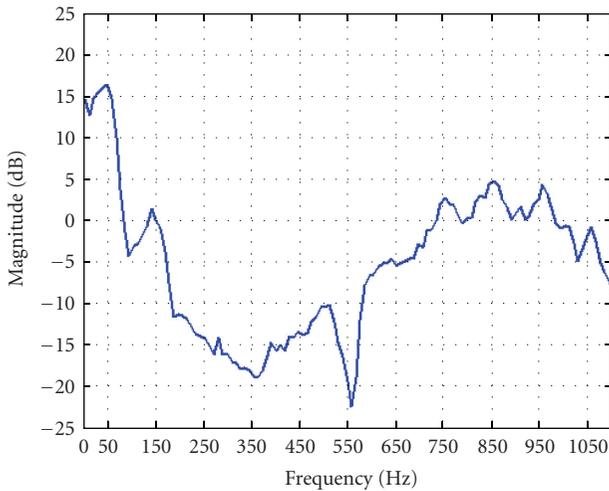


FIGURE 11: Spectrum of the optimum modulated signal.

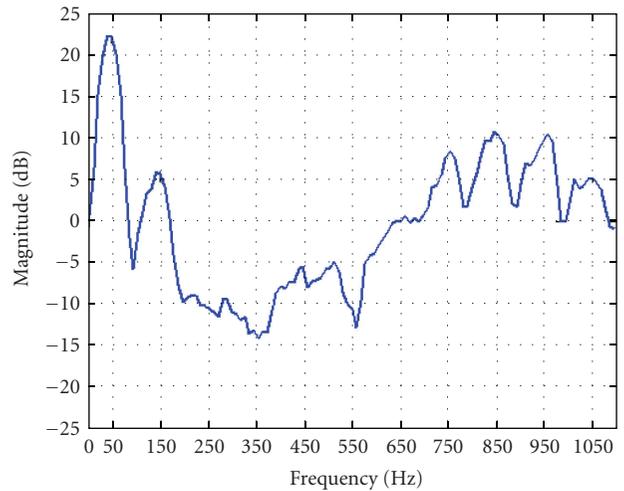


FIGURE 12: Spectrum of the chopped optimum modulated signal.

The chopper signal generator block is expanded in Figure 8. It has two 8-bit registers, one for the value of the duty and the other to produce a high-frequency signal. The chopper outputs zeros as long as the 8-bit counter value is lower than the value held in the duty registry, thereafter the chopper outputs ones.

Two other blocks are added to the system in order to produce suitable signals to the drivers of the three-phase bridge that controls the motor: a narrow pulse skipper and a dead-time generator.

The narrow pulse skipper or pulse dropper impedes that very short time pulses reach the semiconductor devices

of the bridge since its on-off characteristics made them incapable for following very fast transitions. A scheme of this circuit is shown in Figure 9. These narrow pulses are a direct consequence of the XOR operation and can be noticed in Figure 3.

The dead-time insertion circuit is appended to avoid the simultaneous conduction of both upper and lower devices of the bridge during a commutation. This section of the system is illustrated in Figure 10.

The whole system was simulated and programmed into an FPGA, and their functionalities were verified after the place and route stage.

The signals of the optimum modulator with and without the chopper operation are captured, and their spectrums are computed and shown in Figures 11 and 12.

By comparing the spectrums of both signals one may conclude that the chopped version is most modified on the upper frequency range. By changing the ratio in (6) and adding additional banned harmonics, the unwanted distortion may be moved further to higher frequencies, until the pulse dropper puts a limit to protect power devices from heating by high-frequency switching.

5. Conclusion

The implementation of an optimum digital modulator was successfully done and the main characteristics obtained are the following.

- (a) The output filtering operation might be avoided when the PWM output is applied to an AC motor because the modulation technique allows to cancel out some undesired harmonic frequencies while the remaining high frequencies are attenuated by the motor coil inductance. More than three angles can be used to eliminate more unwanted harmonics.
- (b) The implementation is done in a single chip using only a little fraction of the total cells of the FPGA.
- (c) The implementation performs a modulation process without requiring much CPU time of a microcontroller, like most of the complex commercial modulators; this is because after calculating the angles, they can be stored in the FPGA to generate the PWM output signals inside.
- (d) An inexpensive hardware solution is proposed to vary the voltage with high resolution for motor speed control applications or VRMs. This approach involves a chopper operation as described above.

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