

## Research Article

# Scalable RFCMOS Model for 90 nm Technology

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This paper presents the formation of the parasitic components that exist in the RF MOSFET structure during its high-frequency operation. The parasitic components are extracted from the transistor's S-parameter measurement, and its geometry dependence is studied with respect to its layout structure. Physical geometry equations are proposed to represent these parasitic components, and by implementing them into the RF model, a scalable RFCMOS model, that is, valid up to 49.85 GHz is demonstrated. A new verification technique is proposed to verify the quality of the developed scalable RFCMOS model. The proposed technique can shorten the verification time of the scalable RFCMOS model and ensure that the coded scalable model file is error-free and thus more reliable to use.

## 1. Introduction

The relentless scaling down of CMOS technologies has greatly improved the RF performance of MOSFET. It has been reported that for a technology node of 90 nm, high  $f_t$  of 209 GHz and  $f_{\max}$  of 248 GHz are achieved [1]. Furthermore, the scaling down of the transistor has brought about lower  $NF_{\min}$ , and it is now comparable to the reported SiGe BJT process [1, 2]. The improved RFCMOS performance coupled with its lower cost has motivated circuit designers to integrate digital, mixed-signal, and RF transceiver blocks into a single chip [3–7]. However, for these RF chips to operate at higher-frequency region, the circuit design specifications will become more stringent, and this will require accurate and scalable RFCMOS models that can be simulated accurately at high-frequency region. Furthermore, by employing scalable RF CMOS model into the process design kit (PDK), the circuit design environment is improved, and this can help circuit designers in their circuit optimization and shorten the design cycle and time to market of these RF chips.

Most of the RF models developed today are based on the macromodelling approach. In this approach, subcircuit components are added to the transistor's core model to model

the RF parasitic of MOSFET structure [8, 9], and the core model used is usually the commercially available models such as BSIM3v3 [10] and BSIM4 [11]. The subcircuit components are extracted from the measured S-parameters of the transistor, but the extracted values of these RF components can differ when different extraction technique is used. All the existing RF parameter extraction technique is based on the transistor's small-signal equivalent circuit analysis. Therefore, to characterize an RF MOSFET, all its RF parasitic elements must be included into the small-signal equivalent circuit. Although it has been demonstrated that including the subcircuit components into the core model can accurately simulate for the transistor's RF characteristics, such developed model is normal for discrete transistor sizes. In order to generate a geometry-scalable RFCMOS model, the extracted subcircuit component values must be studied for its geometry dependency and by formulating equations to capture their physical effects at high-frequency region, and a physical scalable RFCMOS model can be generated. Presently, some publications are reported for the scalable RF MOSFET modelling [12–14], but these publications [12, 14] do not show all the geometry-scalable equations of the subcircuit components. In [13], the formulated equations

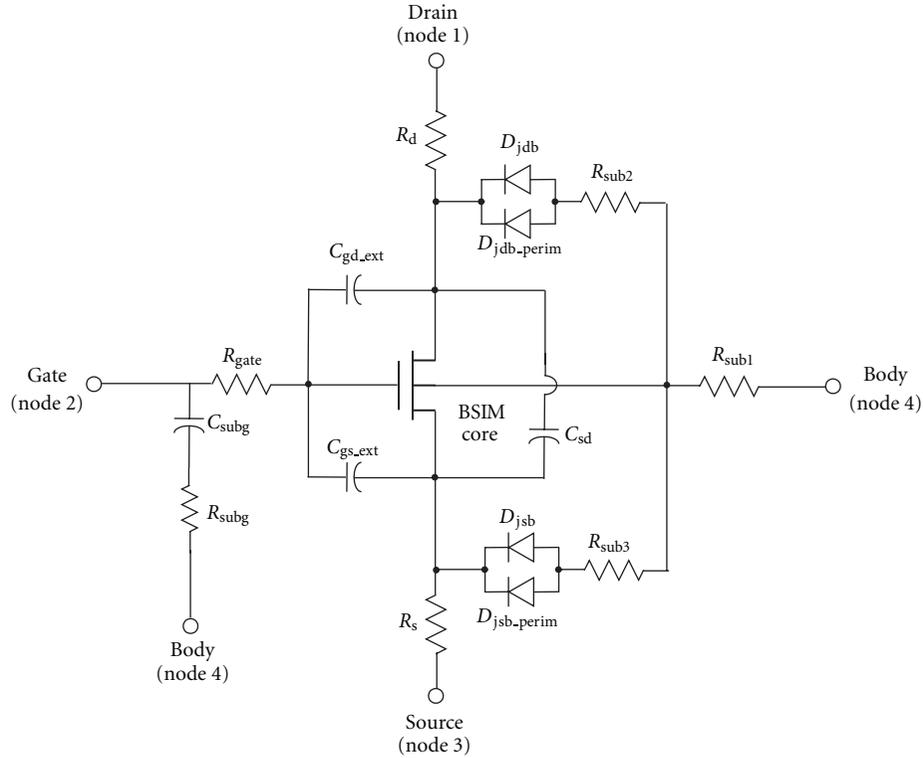


FIGURE 1: RF equivalent subcircuit model.

for the subcircuit components were empirical and have no physical meaning, and furthermore, only one device size of  $f_t$  and  $f_{max}$  plot is presented.

In this paper, the geometry dependencies of the RF subcircuit components were studied, and the formulation of these RF components was done based on their physical effects and the geometry of the layout structure. The scalable transistor's RF characteristics with respect to the layout geometry, biasing, and frequency will be demonstrated with good accuracy between the measured and simulated results. Presently, there is no standard technique proposed for quantifying the quality of a developed scalable RF model. Hence, a new technique is proposed in this paper to help modelling engineers to verify and check the developed scalable RF model for their scalability and accuracy. By utilizing this proposed technique, the model geometry scalability with respect to the transistor's unit width ( $W_f$ ) and finger number ( $N_f$ ) is monitored to ensure that the formulated geometry equations are correct. Furthermore, by plotting the proposed accuracy plots, the error population of the developed model is monitored and ensured that they are below the error's specification of the developed model. The scalable RF model was developed for 90 nm process with channel length of 70 nm for a frequency range of 50 MHz to 49.85 GHz. The devices under test (DUT) are NMOS transistors with  $N_f$  of 4, 8, 16, 24, 32, 48, and 64 and  $W_f$  of 1, 2.5, and 5  $\mu\text{m}$ . By studying the geometry dependence of the RF subcircuit components for the above DUT, the physical

geometry equations with fabrication process parameters are formulated, and from the comparison between the extracted and calculated component values, excellent agreement for all the above combinations of  $N_f$  and  $W_f$  is shown.

Section 2 shows the transistor's equivalent subcircuit model and the layout of the DUT used. The detailed explanation on the formulation of the equation for the subcircuit components is then shown, and the plots to compare between the calculated and extracted component values are presented. In Section 3, the good fitting between the measured and simulated DC and RF results for the various geometry combinations is shown, and the further verification with the proposed technique for the generated scalable RFCMOS model is presented. The conclusion follows in Section 4.

## 2. Scalable RF MOSFET Modelling

Figure 1 shows the proposed RF equivalent subcircuit model. All the subcircuit components are physical and can be used for transistor that has the source and body terminal tied together and grounded.

The resistance  $R_{gate}$  represents the effective lumped gate resistance that consists of both the electrode resistance and the distributed channel resistance [15]. The resistances  $R_s$  and  $R_d$  represent the effective source and drain resistance that consist of the metal line, via, and contact resistances.

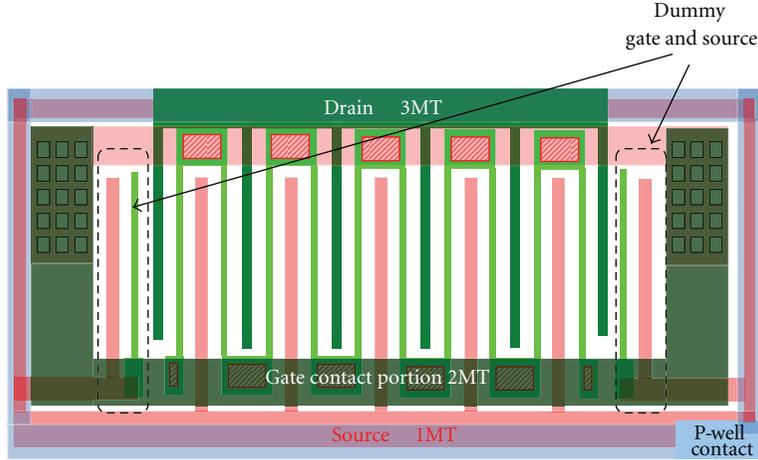


FIGURE 2: Simplified RF NMOS layout.

The capacitances  $C_{gs,ext}$  and  $C_{gd,ext}$  represent the effective gate-to-source and gate-to-drain capacitances and consist of both the overlap and fringing capacitances between the terminals.  $C_{ds}$  represents the drain-to-source fringing capacitance between the metal lines that connect to the source and drain diffusions. As the internal junction capacitances of the core model are turned off, the external diodes  $D_{jdb}$ ,  $D_{jdb,perim}$ ,  $D_{jsb}$ , and  $D_{jsb,perim}$  are added as the junction capacitances to connect the substrate resistance network.  $D_{jdb}$  stands for the area intensive diode, while the  $D_{jdb,perim}$  stands for the perimeter intensive diode, and the definition is the same for the source-to-body junction diodes. The parameters  $R_{sub1}$ ,  $R_{sub2}$ , and  $R_{sub3}$  represent the substrate network resistances. Finally,  $C_{subg}$  and  $R_{subg}$  are defined as the gate-to-substrate capacitance and resistance over the shallow trench isolation (STI) region.

Figure 2 shows the simplified layout of the RF NMOS transistor. The transistor has a multifinger configuration with double-contacted gate polystructure. Dummy gate poly is added to improve the gate structure formation. The metal 1 and metal 2 are used for the connection of the gate terminal. The source diffusions are connected using the metal 1 and shortened to the body terminal or P-well, while the drain diffusions are pulled out using the metal 3.

In order to extract physical subcircuit components in the macromodel, all the physical layers and their geometry that are used to form the structure of the transistor must be known. The extraction technique used to extract the subcircuit components values is as shown in [16].

**2.1. Gate Resistance Modelling.** Figure 3 shows the simplified polysilicon gate structure and its distributed parasitic resistances. At RF frequency region,  $R_{gate}$  is influenced by three physical effects. The three effects are the distributed gate electrode resistance  $R_{g,poly,W_f}$ , the non-quasi-static (NQS) effect in the channel  $R_{g,ch}$  [15, 17], and the polysilicon gate extension out of the active region  $R_{g,poly,W_{ext}}$  follows:

$$R_{gate} = R_{g,poly,W_f} + R_{g,ch} + R_{g,poly,W_{ext}}. \quad (1)$$

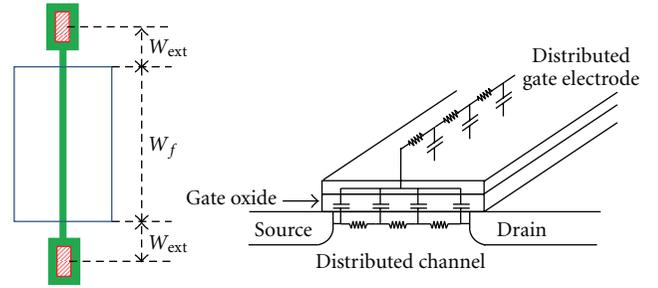


FIGURE 3: Simplified polysilicon gate structure and its distributed parasitic resistances.

In [18], the distributed effect of the gate electrode has been studied and the following equations have been derived to calculate the distributed gate electrode resistance.

$$R_{g,poly,W_f} = \frac{\rho_{poly} \cdot W_f / L_g}{3 \cdot N_f}, \quad \text{Single-contacted gate,} \quad (2)$$

$$R_{g,poly,W_f} = \frac{\rho_{poly} \cdot W_f / L_g}{12 \cdot N_f}, \quad \text{Double-contacted gate.} \quad (3)$$

In (2) and (3), the variable  $N_f$  is the number of fingers,  $\rho_{poly}$  is the gate sheet resistance, and  $L_g$  and  $W_{fs}$  are the channel length and unit width of a single finger. The factors of 1/3 and 1/12 are used in (2) and (3) to account for the distributed gate resistance effect and the different gate connection configuration at the ends of the gate structure.

The polysilicon gate extension  $W_{ext}$  as shown in Figure 1 contributes to the total gate resistance as follows:

$$R_{g,poly,W_{ext}} = \frac{\rho_{poly} \cdot (W_{ext}/2)}{N_f \cdot L_g}. \quad (4)$$

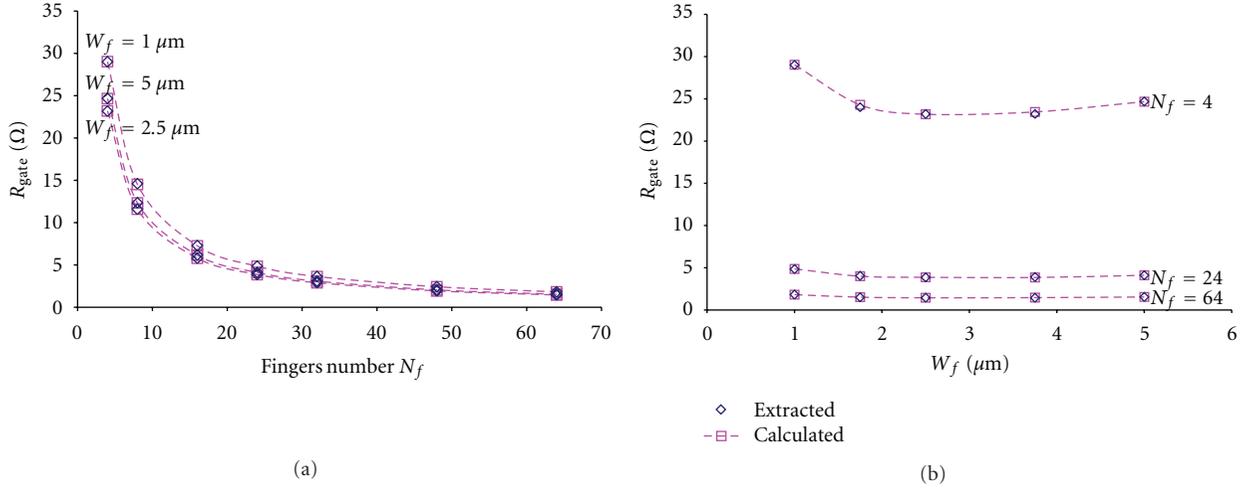


FIGURE 4: Extracted and calculated  $R_{\text{gate}}$  versus (a)  $N_f$  and (b)  $W_f$ .

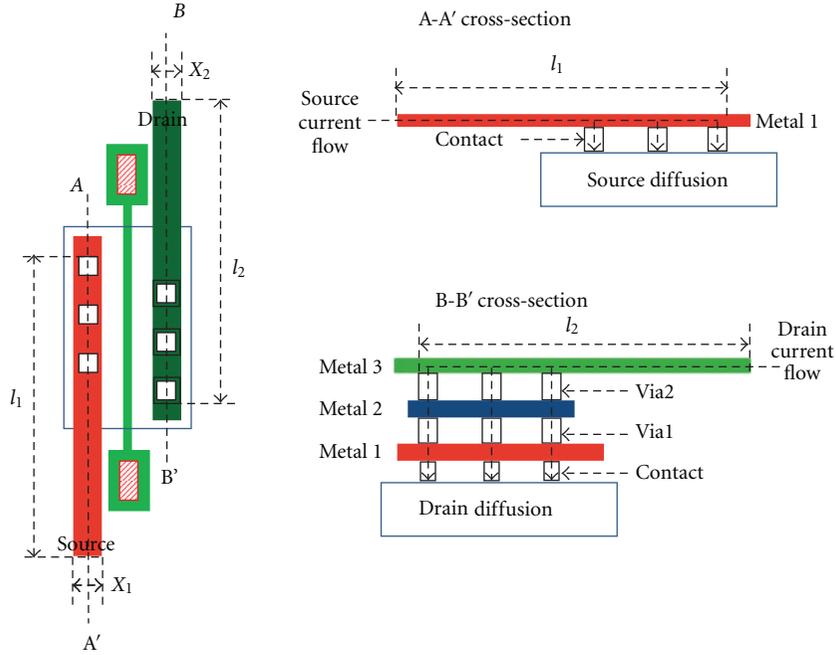


FIGURE 5: Source and drain metal structure.

At RF frequency region, the channel will become like a distributed RC network as shown in Figure 1. The distributed channel resistance will reflect to the gate through the capacitance network and increase the total gate resistance. Note that this NQS channel resistance is bias and geometry dependent. However, it is reported that a simple gate resistance can model the distributed gate resistance effect, and it is accurate up to  $f_t/2$  for a MOSFET without any significant NQS effects [19]. Hence, only a geometry-dependent NQS channel resistance is assumed to contribute to the total gate resistance as follows:

$$R_{g,\text{ch}} = \frac{x_1 \cdot (L_g)}{N_f \cdot W_f}. \quad (5)$$

Note that the variable  $x_1$  is defined as a factor of the channel sheet resistance that is reflected back to the gate structure.

Figure 4 shows the comparison between the extracted and calculated  $R_{\text{gate}}$  versus  $N_f$  and  $W_f$  plots. It is observed that  $R_{\text{gate}}$  is inversely proportional to  $N_f$ , and there exists a minimum  $R_{\text{gate}}$  at the  $W_f$  of  $2.5 \mu\text{m}$ . The  $N_f$  and  $W_f$  dependence of  $R_{\text{gate}}$  can be explained by considering (1)–(5). From (2)–(5), the three physical effects on the gate resistance are inversely proportional to  $N_f$ , and this explains the trend of  $R_{\text{gate}}$  versus  $N_f$ . As shown in (3), the resistance  $R_{g,\text{poly-}W_f}$  is directly proportional to  $W_f$ , but in (5), the resistance  $R_{g,\text{ch}}$  is inversely proportional to  $W_f$ . The  $W_f$  effect on the resistance  $R_{g,\text{poly-}W_f}$  and  $R_{g,\text{ch}}$  will compete

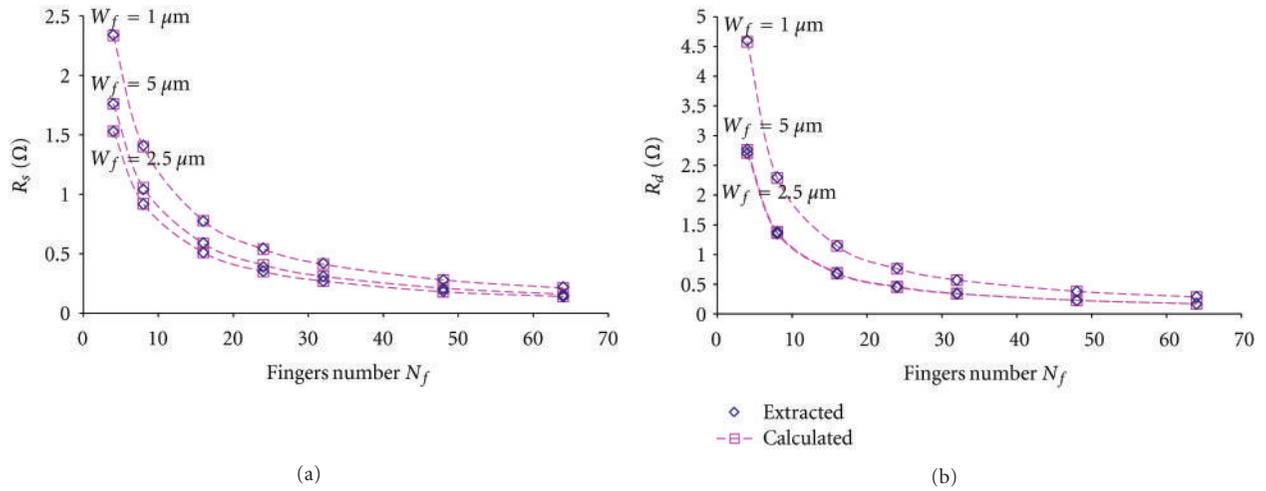


FIGURE 6: Extracted and calculated (a)  $R_s$  and (b)  $R_d$  versus  $N_f$ .

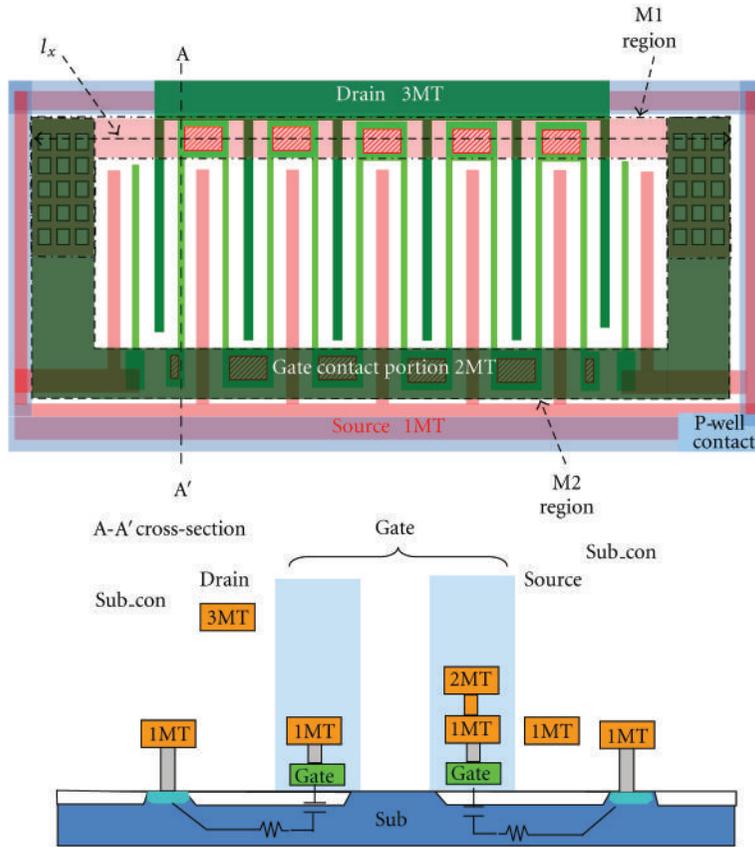


FIGURE 7: Gate-to-substrate capacitance and resistance structure.

with each other and cause  $R_{\text{gate}}$  to have a minimum point as shown in Figure 4. Therefore, based on the proposed physical geometry equation, the calculated and extracted  $R_{\text{gate}}$  resistance matches well with the change in  $N_f$  and  $W_f$  of the transistor.

2.2. Source and Drain Resistance Modelling. The resistances  $R_s$  and  $R_d$  shown in Figure 1 are defined as the effective resistances that consist of the metal line, via, and contact resistances as shown in the layout of Figure 5. It is assumed that the source and drain resistance model in the BSIM3v3

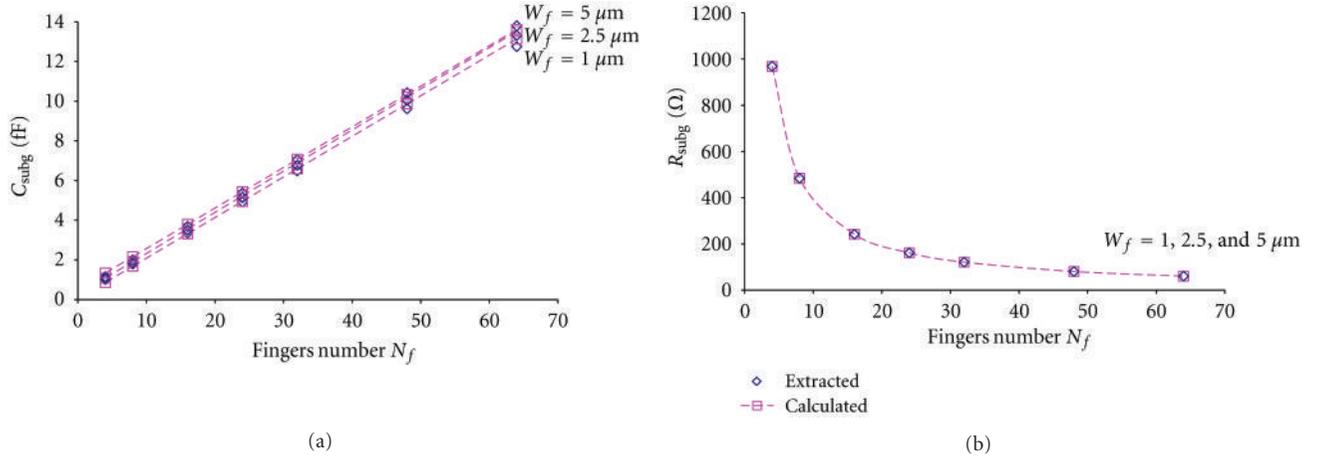


FIGURE 8: Extracted and calculated (a)  $C_{\text{subg}}$  and (b)  $R_{\text{subg}}$  versus  $N_f$ .

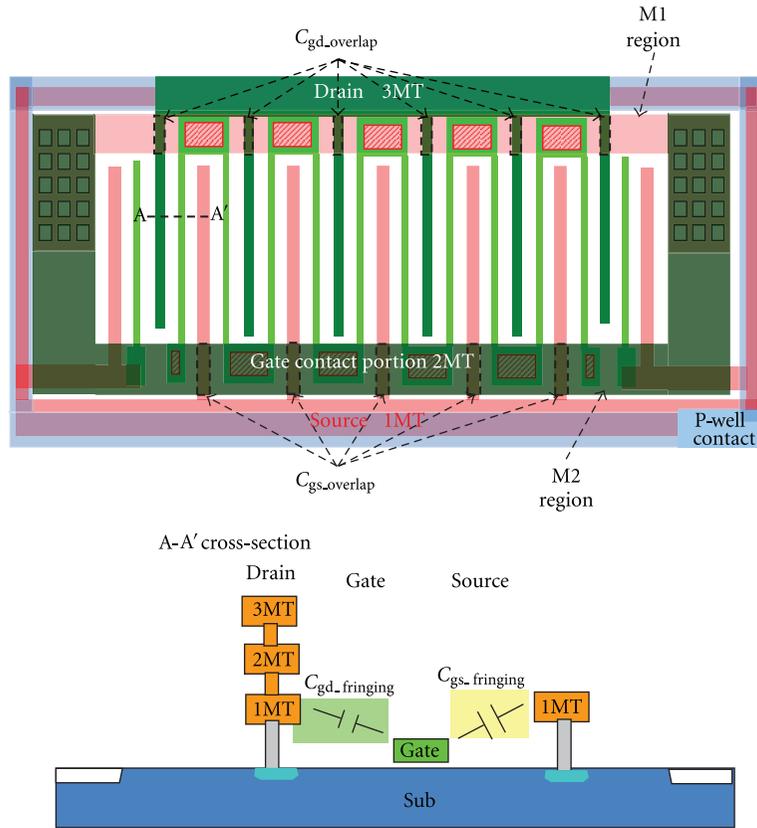


FIGURE 9: Gate-to-source and gate-to-drain capacitance structures.

model only models the active region of the parasitic resistances. Based on the above layout, the following equations can be derived to represent  $R_s$  and  $R_d$ :

$$R_s = \frac{(\rho_{m1} \cdot l_1)/x_1 + (R_{\text{con}}/n_{\text{con}})}{n_{\text{diff,source}}},$$

$$R_d = \frac{(\rho_{m3} \cdot l_2)/x_2 + (R_{\text{con}} + R_{\text{via1}} + R_{\text{via2}})/n_{\text{con}}}{n_{\text{diff,drain}}}. \quad (6)$$

The variables  $\rho_{m1}$  and  $\rho_{m3}$  represent the sheet resistance for metal 1 and metal 3, and the variables  $R_{\text{con}}$ ,  $R_{\text{via1}}$ , and  $R_{\text{via2}}$  represent the contact, via1, and via2 resistances and the

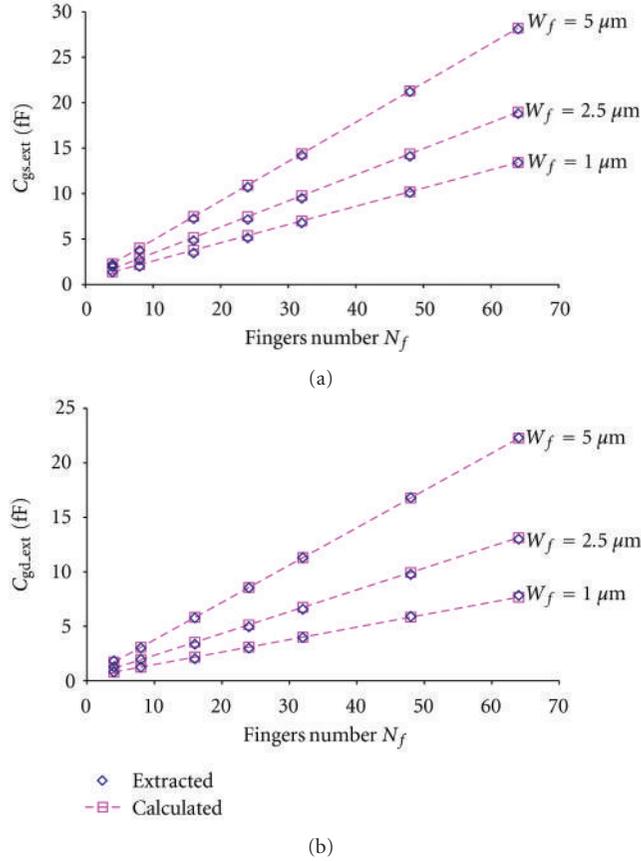


FIGURE 10: Extracted and calculated (a)  $C_{gs,ext}$  and (b)  $C_{gd,ext}$  versus  $N_f$ .

$n_{con}$ ,  $n_{diff,source}$ , and  $n_{diff,drain}$  are the numbers of contacts and source and drain diffusions in the transistor.

Figure 6 shows the comparison between the extracted and calculated  $R_s$  and  $R_d$  versus  $N_f$  plots. It is observed that both resistances are inversely proportional to  $N_f$ , and there exists a minimum point of resistance value at the  $W_f$  of  $2.5 \mu\text{m}$ . From (6), the  $n_{diff,source}$  and  $n_{diff,drain}$  are the number of source and drain diffusions, and they are proportional to  $N_f$ . Hence, the  $R_s$  and  $R_d$  resistances show the inverse proportionality with  $N_f$ . From Figure 5, the variables  $l_1$ ,  $l_2$  and  $n_{con}$  are proportional to the  $W_f$  of the transistor, and when they are applied to (6), the  $W_f$  effect on both  $l_1$  and  $l_2$  will compete with  $n_{con}$  and cause a minimum resistance level to occur at  $W_f$  of  $2.5 \mu\text{m}$ .

**2.3. Gate-to-Substrate Capacitance and Resistance Modelling.** The components  $C_{subg}$  and  $R_{subg}$  that are shown in Figure 1 are defined as the gate-to-substrate capacitance and resistance over the STI region, and they are shown in the cross-sectional structure in Figure 7. The dotted enclosed region in Figure 7 is the gate area that is on top of the STI region generating the parasitic components  $C_{subg}$  and  $R_{subg}$ , and based on the above layout geometry, the following equations are formulated:

$$C_{subg} = C_{M1,STI} \cdot a_{M1} + C_{M2,STI} \cdot a_{M2}. \quad (7)$$

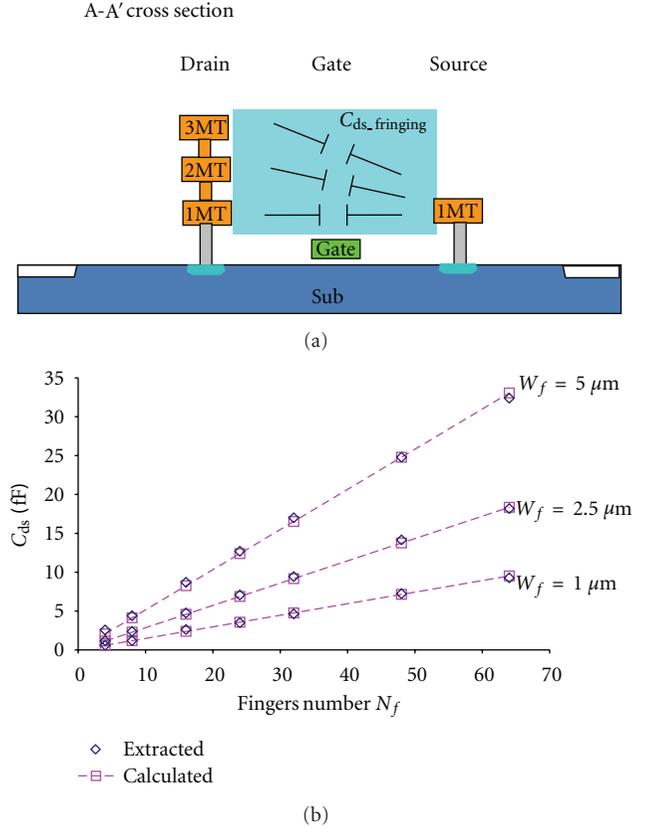


FIGURE 11: Drain-to-Source capacitance structure (a) and extracted and calculated  $C_{ds}$  versus  $N_f$  (b).

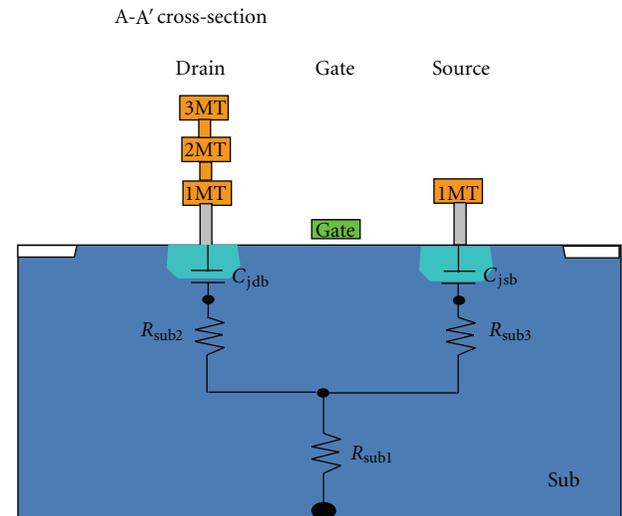


FIGURE 12: Substrate resistances network.

The variables  $C_{M1,STI}$  and  $C_{M2,STI}$  are the parasitic capacitances per unit area of metal 1 and metal 2 over the STI region, while the variables  $a_{M1}$  and  $a_{M2}$  are the area of the

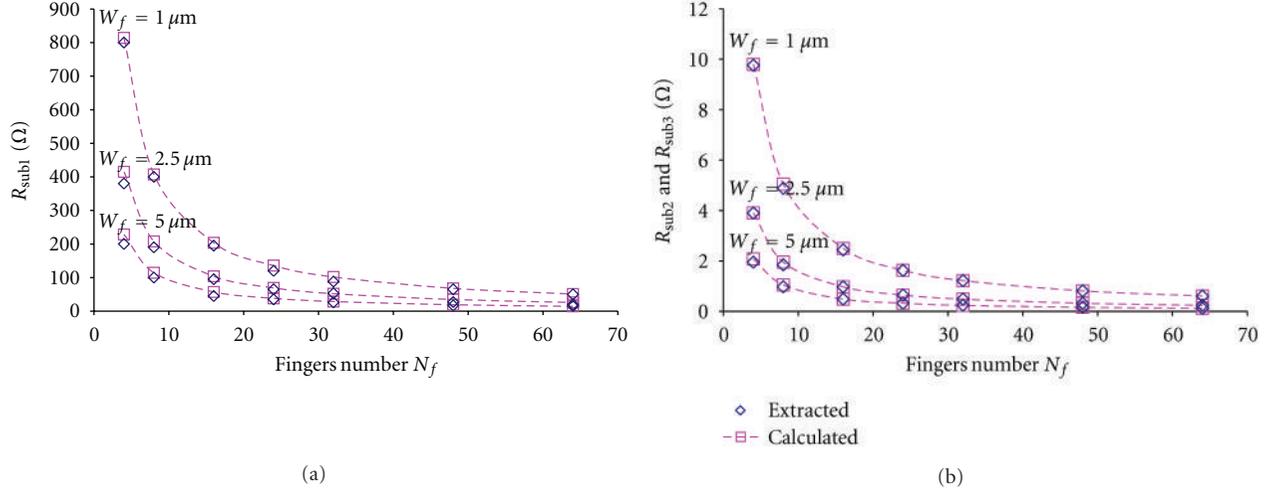


FIGURE 13: Extracted and calculated (a)  $R_{\text{sub1}}$  and (b)  $R_{\text{sub2}}$  and  $R_{\text{sub3}}$  versus  $N_f$ .

dotted enclosed region of metal 1 and metal 2 as shown in Figure 7.

$$R_{\text{subg}} = \frac{R_{\text{substrate,STI}}}{N_f}. \quad (8)$$

From (7), it is shown that  $C_{\text{subg}}$  is mainly contributed by the parasitic capacitances due to the layers of gate metal 1 and metal 2 over the STI region. The extracted variables  $C_{M1,STI}$  and  $C_{M2,STI}$  in (7) represent the capacitance per unit area ( $fF/\mu\text{m}^2$ ) of the enclosed metal 1 and metal 2 regions as shown in Figure 7. As the dielectric thickness between metal 2 and the substrate is higher than that of metal 1, it is expected that the extracted  $C_{M1,STI}$  is higher than  $C_{M2,STI}$ . Since there is some area under the enclosed metal 1 and metal 2 regions that is overlapped with the polysilicon gate, the proposed equation (7) may overestimate  $C_{\text{subg}}$  slightly, and a small capacitance may be required to be subtracted from the above equation.

$C_{\text{subg}}$  and  $R_{\text{subg}}$  are extracted using Seneca and Substrate storms [20] that simulate the layout structure as shown in Figure 7. Based on the extracted results of  $R_{\text{subg}}$ , it is found that it is only dependent on  $N_f$ , and it is formulated as shown in (8). Note that the extracted  $R_{\text{substrate,STI}}$  is defined as the substrate parasitic resistance under the STI region.

Figure 8 shows the comparison between the extracted and calculated  $C_{\text{subg}}$  and  $R_{\text{subg}}$  versus  $N_f$  plots. It is observed that  $C_{\text{subg}}$  is proportional to  $N_f$  while  $R_{\text{subg}}$  is inversely proportional to  $N_f$ . In (7),  $C_{\text{subg}}$  is dependent on  $a_{M1}$  and  $a_{M2}$ , and when  $N_f$  increases, the two areas will increase and cause  $C_{\text{subg}}$  to increase.

Based on the layout structure in Figure 7, it is observed that the length of  $l_x$  is proportional to  $N_f$ . By using the simple resistance equation that uses the sheet resistance multiply with the number of squares, it is obvious that the number of squares in the signal flow path of  $R_{\text{subg}}$  is inversely proportional to the length of  $l_x$ . Hence,  $R_{\text{subg}}$  will decrease with increasing  $N_f$ .

**2.4. Gate-to-Source and Gate-to-Drain Capacitances Modelling.** The capacitance  $C_{\text{gs,ext}}$  and  $C_{\text{gd,ext}}$  in Figure 1 represent the overlap and fringing capacitances between the gate-to-source and gate-to-drain terminals as shown in Figure 9. Based on the above layout structure, it is obvious that the amount of overlap capacitance is dependent on the number of source and drain metal lines that overlap the gate metal, while the fringing capacitances will be dependent on the separation distance between the source/drain metal lines to gate polysilicon structure and the  $W_f$  of the transistor. Since the separation distance between the source/drain metal lines and the gate polysilicon structure is fixed, therefore the fringing capacitance is only dependent on transistor's  $W_f$ . Based on the above analysis, the following equations are formulated:

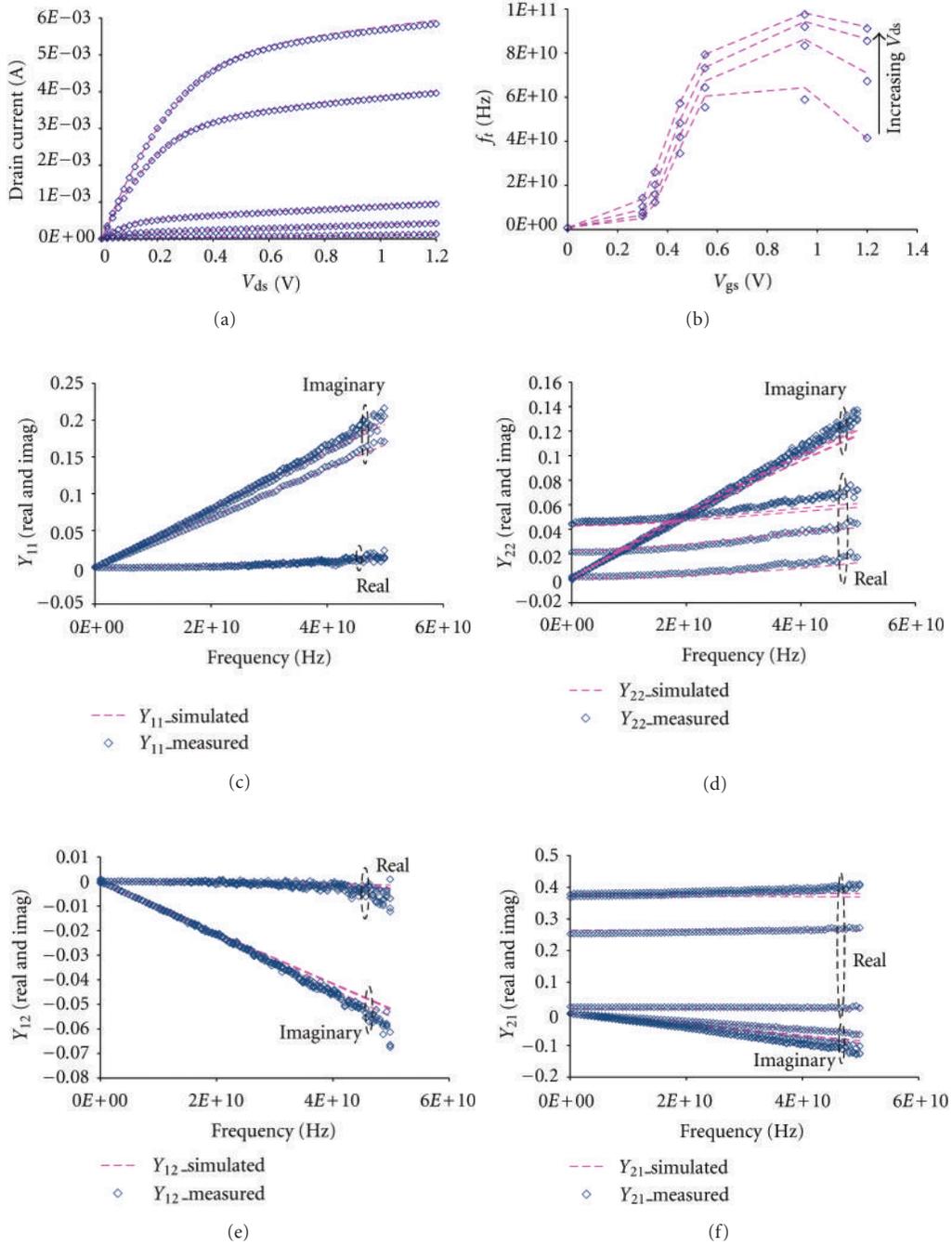
$$C_{\text{gs,ext}} = C_{M2-M1,gs,overlap} \cdot n_{\text{diff,source}} + C_{M1-Poly,gs,fringing} \cdot N_f \cdot W_f. \quad (9)$$

Note that  $C_{M2-M1,gs,overlap}$  is the overlap capacitance between the gate (metal 2) and source (metal 1) metal lines, and  $C_{M1-Poly,gs,fringing}$  is the fringing capacitance between the gate structure (polysilicon) and the source (metal 1) metal lines.

$$C_{\text{gd,ext}} = C_{M3-M1,gd,overlap} \cdot n_{\text{diff,drain}} + C_{M1-Poly,gd,fringing} \cdot N_f \cdot W_f. \quad (10)$$

Here  $C_{M3-M1,gd,overlap}$  is the overlap capacitance between the gate (metal 1) and drain (metal 3) metal lines and  $C_{M1-Poly,gd,fringing}$  is the fringing capacitance between the gate structure (polysilicon) and the drain (metal 1) metal lines. It is assumed that the fringing capacitances from the metal 2 and metal 3 lines of the drain metal structure to the polysilicon gate are small and negligible when compared to the metal 1 and to the polysilicon gate fringing capacitance.

As the dielectric separation distance between the metal 3 (drain) and metal 1 (gate) is larger than the case of metal 2 (gate) and metal 1 (source), it is expected that


 FIGURE 14: Measured and simulated results for NMOS transistor with  $N_f$  of 8,  $W_f$  of  $1\ \mu\text{m}$ , and  $L_g$  of 70 nm.

$C_{M2-M1,gs\_overlap}$  will be larger than  $C_{M3-M1,gd\_overlap}$ . Furthermore, the extracted  $C_{M1-Poly,gs\_fringing}$  must be close to the extracted  $C_{M1-Poly,gd\_fringing}$  or slightly smaller.

Figure 10 shows the comparison between the extracted and calculated  $C_{gs\_ext}$  and  $C_{gd\_ext}$  versus  $N_f$  plots. It is observed that both capacitances are proportional to  $N_f$  and  $W_f$ , and the extracted  $C_{gs\_ext}$  capacitance is slightly larger than  $C_{gd\_ext}$ . In (9) and (10), the  $N_f$  dependence in both of the capacitances is due to the variables  $n_{diff,source}$  and  $n_{diff,drain}$ ,

and since  $n_{diff,source}$  has one more diffusion than the  $n_{diff,drain}$ , the extracted  $C_{gs\_ext}$  capacitance is slightly larger than  $C_{gd\_ext}$ . The  $W_f$  dependence as shown in Figure 10 is mainly due to the fringing capacitance effect in (9) and (10).

**2.5. Drain-to-Source Capacitance Modelling.**  $C_{ds}$  is defined as the fringing capacitance between the metal lines that connect the source and drain diffusions. The location of the fringing capacitance is indicated in Figure 11(a) that uses the cross-section view of A-A' in Figure 9. Based on the

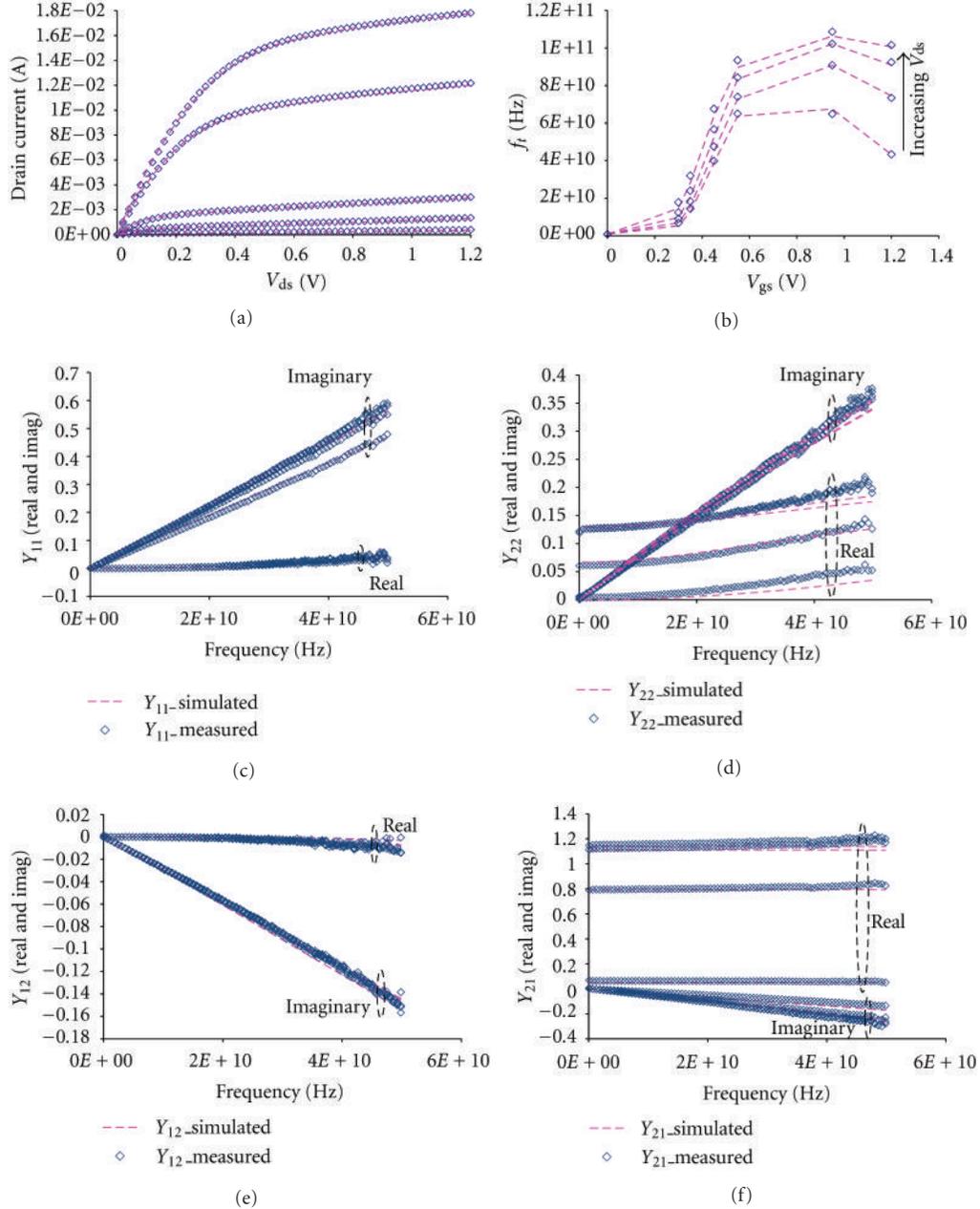


FIGURE 15: Measured and simulated results for NMOS transistor with  $N_f$  of 24,  $W_f$  of  $1\ \mu\text{m}$ , and  $L_g$  of 70 nm.

layout structure, it is predicted that the fringing capacitance is proportional to  $N_f$  and  $W_f$  of the transistor. Hence, the following equation is formulated for  $C_{ds}$ :

$$C_{ds} = C_{ds,\text{fringing}} \cdot N_f \cdot W_f. \quad (11)$$

Note that  $C_{ds,\text{fringing}}$  is the fringing capacitance per unit width between the metal lines of the source and drain metal structures.

In Figure 11(b), the comparison between the extracted and calculated  $C_{ds}$  shows that the proposed formulated equation can accurately predict the change in  $N_f$  and  $W_f$ .

**2.6. Substrate Resistances Modelling.** By using the cross-section view of A-A' in Figure 9, the substrate resistances network is added into the structure to indicate the location of the parasitic as shown in Figure 12.  $C_{j\text{sb}}$  and  $C_{j\text{db}}$  are junction capacitances that are replaced by the junction diodes as shown in Figure 1.  $R_{\text{sub}2}$  and  $R_{\text{sub}3}$  represent the substrate resistances under the channel, while  $R_{\text{sub}1}$  connects the intrinsic bulk node to the body terminal. Based on the layout structure, it is predicted that  $R_{\text{sub}2}$  and  $R_{\text{sub}3}$  are proportional to  $L_g/(N_f \cdot W_f)$ , while  $R_{\text{sub}1}$  is inversely proportional  $N_f \cdot W_f$ . Hence, the following equations are formulated for the substrate resistances:

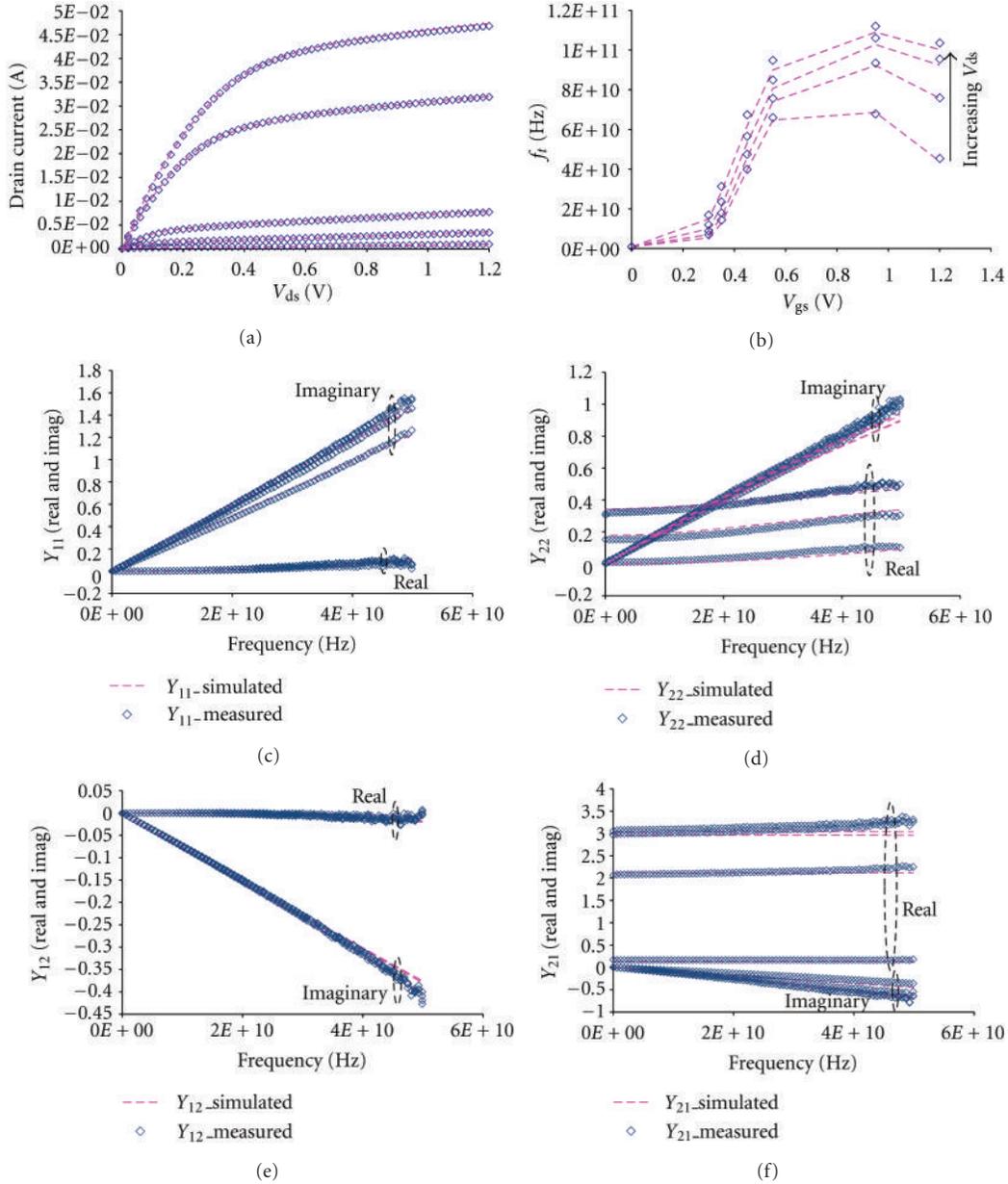


FIGURE 16: Measured and simulated results for NMOS transistor with  $N_f$  of 64,  $W_f$  of  $1 \mu\text{m}$ , and  $L_g$  of 70 nm.

$$R_{\text{sub}1} = \frac{\rho_{\text{substrate}}}{N_f \cdot (W_f + 2 \cdot XJ)}, \quad (12)$$

$$R_{\text{sub}2} = R_{\text{sub}3} = \frac{\rho_{\text{substrate, sheet}} \cdot L_g}{2 \cdot N_f \cdot (W_f + 2 \cdot XJ)}.$$

In (12), the variable  $\rho_{\text{substrate}}$  is the substrate resistivity and has the unit of  $\Omega\mu\text{m}$ , and  $\rho_{\text{substrate, sheet}}$  is the substrate sheet resistance under the active region and has the unit of  $\Omega/\text{number of square}$ . The parameter  $XJ$  represents the source and drain junction depth, and its value can be found in the BSIM3v3 model parameters.

In Figure 13, the comparison between the extracted and calculated substrate resistances shows that the proposed

formulated (12) can accurately predict the change in  $N_f$  and  $W_f$ .

### 3. Measurement Results and Discussion

**3.1. Modelling Results.** The devices under test (DUT) are thin gate NMOSs with fixed  $L_g$  of 70 nm,  $W_f$  of 1, 2.5, and  $5 \mu\text{m}$ , and  $N_f$  of 4, 8, 16, 24, 32, 48, and 64. The S-parameters were measured using the HP8510 network analyzer with GSG RF probes for a frequency range from 50 MHz to 49.85 GHz at the various bias combinations of the gate-to-source  $V_{gs}$  and drain-to-source  $V_{ds}$  potentials. After the system calibration was performed using LRRM technique, the RF transistor and its deembedding structures

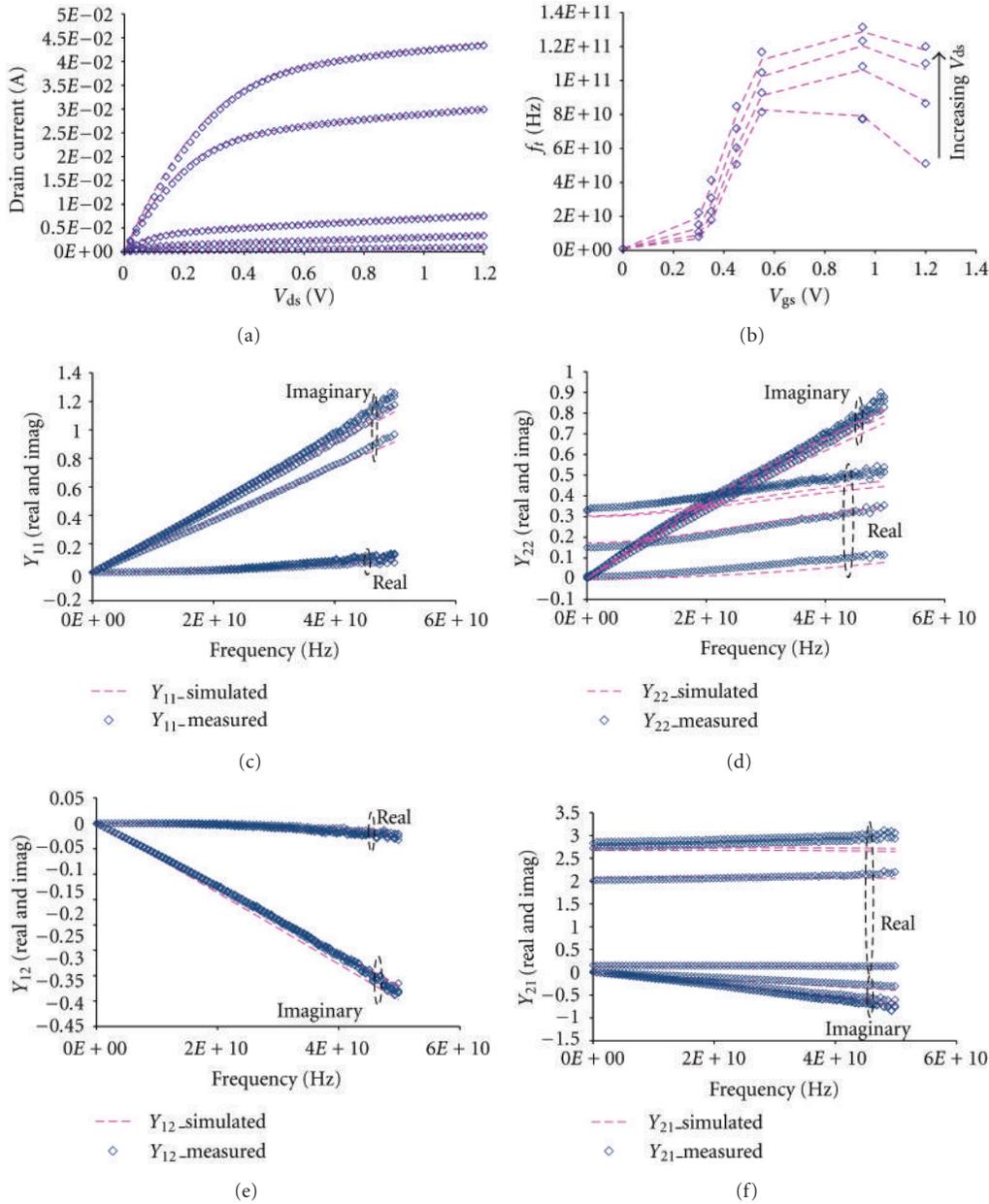


FIGURE 17: Measured and simulated results for NMOS transistor with  $N_f$  of 24,  $W_f$  of  $2.5 \mu\text{m}$ , and  $L_g$  of 70 nm.

were measured. In this measurement, the standard open and short deembedding structures were used to remove the pad and interconnects parasitic [21].

In order to demonstrate the scalability of the RF model, measured and simulated DC, Y-parameters, and  $f_t$  plots are presented in this section. Figures 14–16 show the measured and simulated results for fixed  $W_f$  of  $1 \mu\text{m}$  with varying  $N_f$  of 8, 24, and 64 at the biasing combination of  $V_{gs}$  and  $V_{ds}$  ranging from 0.3 to 1.2 V. From the comparison between the measured and simulated results, it is observed that the RF model can accurately predict the measured results as  $N_f$  varies. The  $W_f$  scalability of the RF model is demonstrated in Figures 15, 17, and 18 for fixed  $N_f$  of 24 with varying  $W_f$

of 1, 2.5, and  $5 \mu\text{m}$ . Hence, from Figures 14–18, the proposed RF model is shown to be geometry scalable for  $N_f$  and  $W_f$  for the frequency range from 50 MHz to 49.85 GHz.

**3.2. Further Verification with Proposed Technique for the Scalable Model.** In a scalable RFCMOS model, there are many different variables that determined the scalability of the RF model. It becomes very tedious to verify and monitor the model accuracy further so that the developed model, file has to be scalable for a certain range of geometry, biasing and frequency variables. Hence, a new verification technique is proposed in this paper. This proposed verification technique is crucial to both the modelling engineers and the model

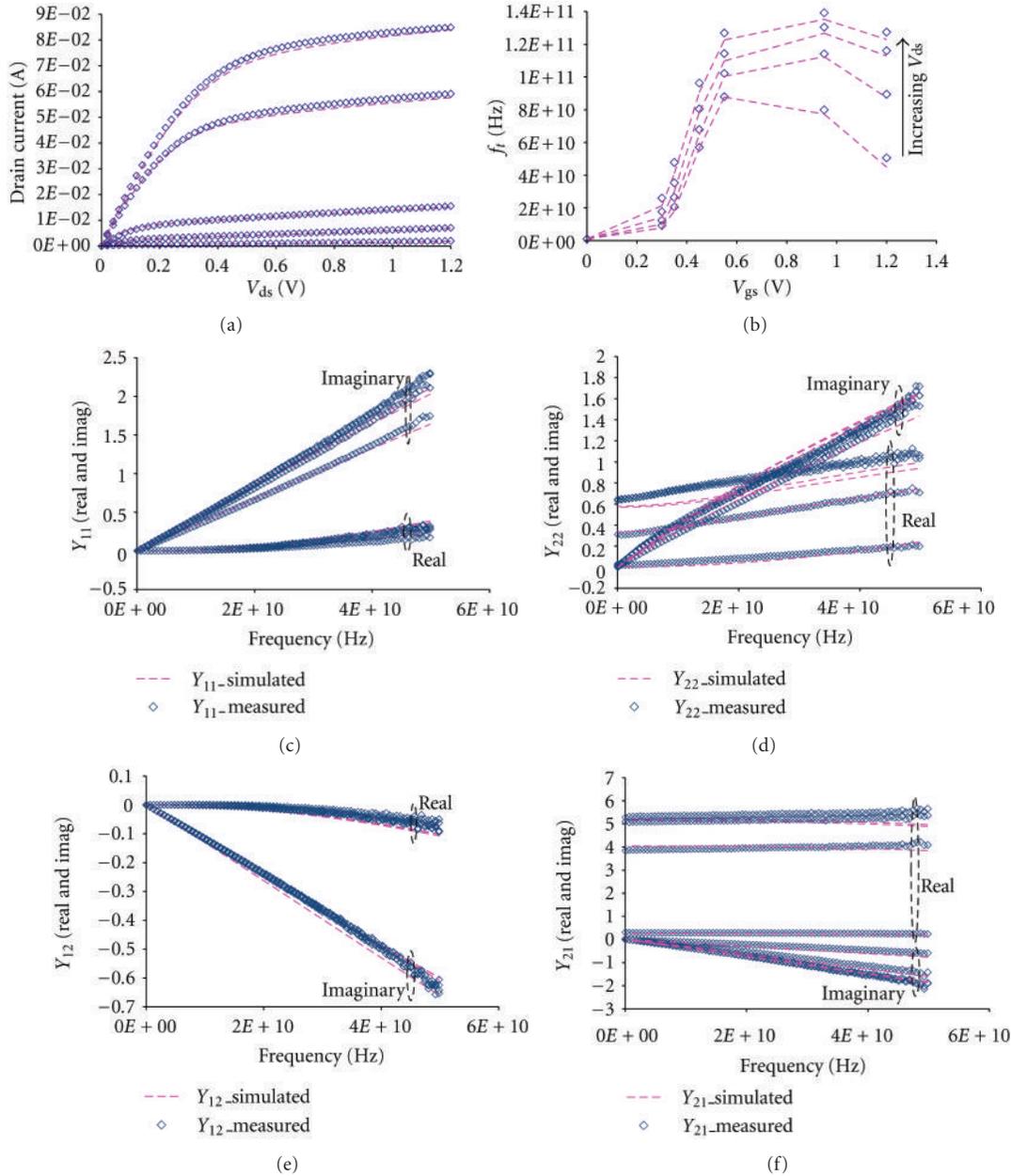


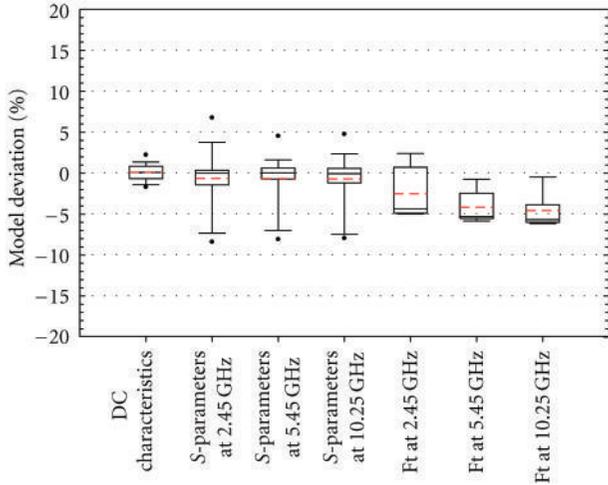
FIGURE 18: Measured and simulated results for NMOS transistor with  $N_f$  of 24,  $W_f$  of  $5 \mu\text{m}$ , and  $L_g$  of 70 nm.

file end users as it helps them to monitor the quality of the developed model and at the same time, the model file can be checked for any errors in the coded geometry equations of the parasitic subcircuit components. Furthermore, by using this proposed technique, the amount of verification time required to check the developed model file is reduced, and thus reducing the overall model development time.

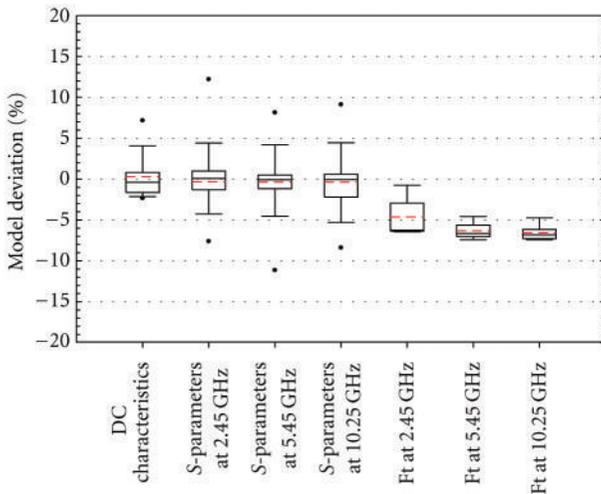
Figure 19 shows the model accuracy plots for NMOS transistors with different  $N_f$  of 4, 8, 16, 24, 32, 48, and 64 and  $W_f$  of 1, 2.5, and  $5 \mu\text{m}$  extracted at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$ . From the box plots, it is observed that 10 to 90% of the error population from the DC, S-parameters, and  $f_t$

are within  $\pm 10\%$ . In the three plots, the model accuracy for all the fabricated devices is monitored at DC, 2.45, 5.45, and 10.25 GHz. Therefore, by generating such model accuracy plots, the quality of the developed RF model in terms of its accuracy is monitored for all the fabricated device sizes and at the different frequency points. Furthermore, by plotting at the other biasing points, the model accuracy of the RF model can be checked for those important biasing regions.

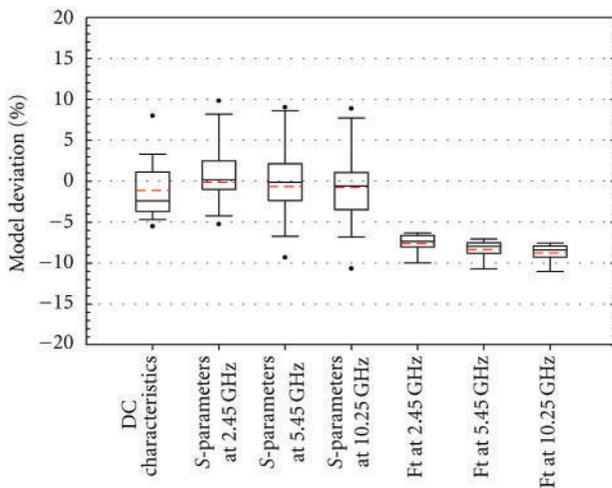
Figure 20 shows the model continuity plots for the parameters  $G_m$  and  $Y_{21}$  versus different  $N_f$  and  $W_f$  of 1, 2.5, and  $5 \mu\text{m}$  extracted at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$ . From the three plots, it is observed that the simulated  $G_m$  (blue line)



(a)

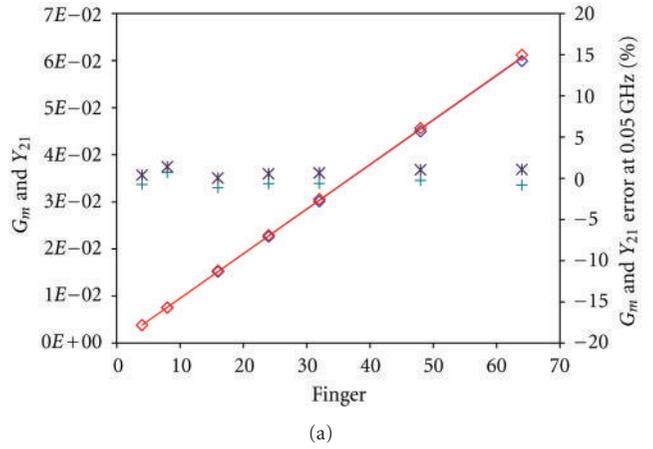


(b)

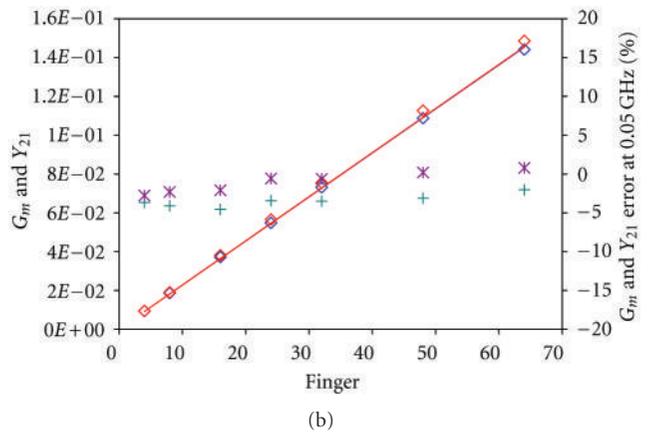


(c)

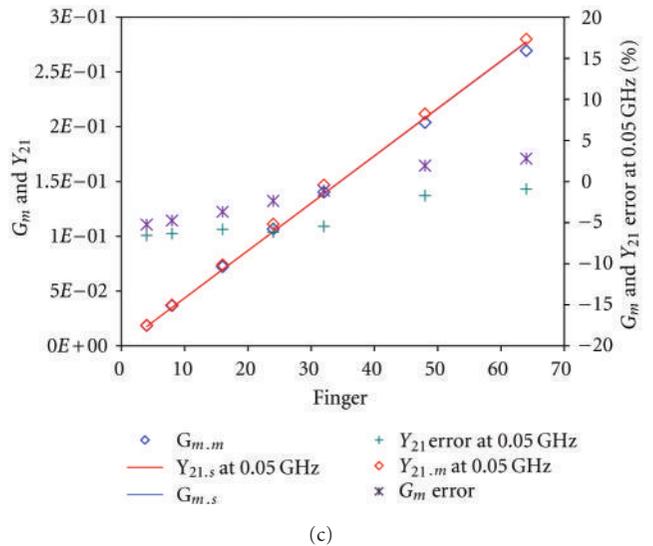
FIGURE 19: Model accuracy for NMOSFETs with different  $N_f$  and  $W_f$  of  $1 \mu\text{m}$  at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$  (a), with different  $N_f$  and  $W_f$  of  $2.5 \mu\text{m}$  at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$  (b), and with different  $N_f$  and  $W_f$  of  $5 \mu\text{m}$  at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$  (c).



(a)



(b)



(c)

FIGURE 20: Model continuity for  $G_m$  and  $Y_{21}$  for NMOSFETs with different  $N_f$  and  $W_f$  of  $1 \mu\text{m}$  at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$  (a), with different  $N_f$  and  $W_f$  of  $2.5 \mu\text{m}$  at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$  (b), and with different  $N_f$  and  $W_f$  of  $5 \mu\text{m}$  at  $V_{gs} = 0.95 \text{ V}$  and  $V_{ds} = 0.8 \text{ V}$  (c).

and  $Y_{21}$  (red line) overlap each other, and this observation implies that the RF model is continuous from DC to RF region. Furthermore, the simulated transistor's gain (red and blue lines) can accurately predict the measured data (red and blue symbols) as the  $N_f$  and  $W_f$  changes and their calculated absolute errors are within the error specification of  $\pm 10\%$ . It is also observed that the simulated  $G_m$  and  $Y_{21}$  scale linearly with  $N_f$  for all the three  $W_f$ . By plotting such model continuity plots at other biasing points, the  $N_f$ ,  $W_f$ , and biasing effect on the RF model are monitored at both the DC and low-frequency region. In the case when the coded equations of the subcircuit components in the model file are incorrect, the model accuracy and continuity plots will immediately reflect the incorrect effects of the wrong equations, and this will alert the modelling engineer to check the coded model file again.

In this proposed technique, the model accuracy and continuity plots are generated to monitor the device geometry, biasing, and frequency variables of the RF model. From these two types of plots, the quality of the developed model and the coded model file will be inspected, and the final verified model file will be error-free and reliable to use.

The proposed model accuracy and continuity plots can also be used as one of the model acceptance criteria, whereby its accuracy and continuity can be checked before accepting and using the developed RF model file.

#### 4. Conclusion

In this paper, the physical formation of the subcircuit parasitic is discussed with respect to its layout structure. The scaling effect of the device geometry is accounted for in the proposed scalable equations for each of the parasitic components. By implementing the proposed scalable equations for the parasitic components into the conventional subcircuit RF model, a scalable RFCMOS subcircuit model can be generated and shown to be valid up to 49.85 GHz. By using the proposed verification technique, the time required to verify a scalable RFCMOS model can be reduced greatly, and the verification step can also ensure that the developed model is error-free, and therefore, it is more robust and reliable to use. Although the scalable RFCMOS model can accurately predict the DC and RF characteristics of the transistor it will still require being able to predict its high-frequency noise. Hence, the scalable RFCMOS model will form the base of the RF transistor modelling so that the study of the scalable high-frequency noise modelling can be embarked on to achieve a fully scalable RFCMOS model.

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#### References

- [1] K. Kuhn, R. Basco, D. Becher et al., "A comparison of state-of-the-art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications," in *Proceedings of the Symposium on VLSI Technology: Digest of Technical Papers*, pp. 224–225, June 2004.
- [2] D. R. Greenberg, B. Jagannathan, S. Sweeney, G. Freeman, and D. Ahlgren, "Noise performance of a low base resistance 200 GHz SiGe technology," in *Proceedings of the IEEE International Devices Meeting Digest (IEDM '02)*, pp. 787–790, December 2002.
- [3] A. A. Abidi, "RF CMOS Comes of Age," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 4, pp. 549–561, 2004.
- [4] F. Op't Eynde, J. Schmit, V. Charlier et al., "A fully-integrated single-chip SOC for bluetooth," in *Proceedings of the IEEE International Solid-State Circuits Conference: Digest of Technical Papers*, pp. 196–197, February 2001.
- [5] H. Darabi, S. Khorram, E. Chien et al., "A 2.4GHz CMOS transceiver for bluetooth," in *Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 200–201, February 2001.
- [6] P. T. M. van Zeijl, J. Eikenbroek, P. Vervoort et al., "A bluetooth radio in 0.18  $\mu\text{m}$  CMOS," in *Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 86–87, February 2002.
- [7] A. Leeuwenburgh, J. ter Laak, A. Mulders et al., "A 1.9GHz fully integrated CMOS DECT transceiver," in *Proceedings of the IEEE International Solid-State Circuits Conference: Digest of Technical Papers*, pp. 450–507.
- [8] S. F. Tin, A. A. Osman, K. Mayaram, and C. Hu, "A simple subcircuit extension of the BSIM3v3 model for CMOS RF design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 612–624, 2000.
- [9] S. Lee and H. K. Yu, "A new extraction method for BSIM3v3 model parameters of RF silicon MOSFETs," in *Proceedings of the IEEE International Conference on Microelectronic Test Structures (ICMTS '99)*, pp. 95–98, March 1999.
- [10] "Official web Site of the BSIM3v3 model," <http://www-device.eecs.berkeley.edu/~bsim3/get.html>.
- [11] "Official web Site of the BSIM4 model," <http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html>.
- [12] M. Lee, R. B. Anna, J. C. Lee, S. M. Parker, and K. M. Newton, "A scalable BSIM3v3 RF model for multi-finger NMOSFETs with ring substrate contact," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 5, pp. 221–224, May 2002.
- [13] S. P. Voinescu, M. Tazlauanu, P. C. Ho, and M. T. Yang, "Direct extraction methodology for geometry-scalable RF-CMOS models," in *Proceedings of the IEEE International Conference on Microelectronic Test Structures (ICMTS '04)*, vol. 14, pp. 235–240, March 2004.
- [14] S. Yoshitomi, A. Bazigos, and M. Bucher, "EKV3 parameter extraction and characterization of 90nm RF-CMOS technology," in *Proceedings of the 14th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES '07)*, pp. 74–79, June 2007.
- [15] X. Jin, J.-J. Ou, C.-H. Chen et al., "An effective gate resistance model for CMOS RF and noise modelling," in *Proceedings of the IEEE International Electron Devices Meeting on Technical Digest*, pp. 961–964, December 1998.
- [16] A. F. Tong, K. S. Yeo, L. Jia, C. Q. Geng, J. -G. Ma, and M. A. Do, "Simple and accurate extraction methodology for

- RF MOSFET valid up to 20 GHz,” *IEE Proceedings: Circuits, Devices and Systems*, vol. 151, no. 6, pp. 587–592, 2004.
- [17] Y. Cheng and M. Matloubian, “High frequency characterization of gate resistance in RF MOSFETs,” *IEEE Electron Device Letters*, vol. 22, no. 2, pp. 98–100, 2001.
- [18] Troels Emil Kolding, “Calculation of MOSFET Gate impedance,” Tech. Rep. R98-1009, 1998.
- [19] C. Enz and Y. H. Cheng, “MOS transistor modeling for RF IC design,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 186–201, 2000.
- [20] A. Nakamura, N. Yoshikawa, T. Miyazako, T. Oishi, H. Ammo, and K. Takeshita, “Layout optimization of RF CMOS in the 90nm generation,” in *Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium*, pp. 373–376, June 2006.
- [21] Y. H. Cheng, “MOSFET modelling for RF IC design,” in *CMOS RF Modelling, Characterization and Application*, pp. 119–196, World Scientific, Singapore, 2002.



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