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Research Article

Vertical Gate RF SOI LIGBT for SPICs with Significantly Improved Latch-Up Immunity

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Based on the previous achievements in improving latch-up immunity of SOI LIGBT, process simulation on our proposed VG RF SOI NLIGBT was carried out with TCAD to provide a virtually fabricated device structure. Then, an approximate latching current model was derived according to the condition of minimum regenerative feedback couple between the parasitic dual-transistors. The model indicates that its latching current is a few orders higher than those before. Further verification through device simulation was done with TCAD, which proved that its weak snapback voltage in the off state is about 0.5–2.75 times higher than those breakdown voltages reported before, its breakdown voltage in the off state is about 19 V higher than its weak snapback voltage, and its latching current density in the on state is about 2-3 orders of magnitude higher than those reported before at room temperature due to hole current bypass through P^+ contact in P-well region. Therefore, it is characterized by significantly improved latch-up immunity.

1. Introduction

Silicon-on-insulator (SOI) lateral insulated gate bipolar transistor (LIGBT) has been widely used in smart power integrated circuits (SPICs) because of its high input impedance, low on-resistance, low forward voltage drop, high breakdown voltage, and compatibility with CMOS technologies [1–20]. SOI technology has been exhibiting more and more importance in the field of high-voltage integrated circuits (HVICs) and SPICs. Compared with bulk junction-isolated devices, SOI LIGBTs offer full dielectric isolation, reduced leakage currents, low-on state resistance, high input impedance, high packing density, fast switching speed, high noise immunity, and feasible operation at very high temperature. Therefore, SOI LIGBTs have attracted much attention in a wide variety of applications such as automotive electronics, consumer electronics, telecommunications, and industrial electronics [10–12, 14–20].

However, an inherent thyristor is involved in an SOI NLIGBT cell. The parasitic thyristor is composed of P anode, N-drift region, P-well, and N^+/P^+-cathode as shown in Figure 1. In a conventional SOI NLIGBT, hole current injected from P anode into drift region is collected by P-well and has to be transported through a pinched resistance along horizontal direction before it reaches P^+ cathode, which results in a forward voltage drop across the P-well/N^+ source junction. When the voltage drop grows sufficient to turn the vertical NPN transistor on at any point, the minimum regener]ative feedback couple condition of the parasitic dual-transistors is satisfied and the parasitic thyristor latches up in a very short time. Gate control cannot be recovered until anode current falls below its holding current and it is very harmful to the device itself and the corresponding SPICs and HVICs [1–16].

Since 1990s, a lot of studies on improving latch-up immunity of SOI LIGBTs have been done extensively [11, 14–18]. Disney and Plummer presented a P^+ sinker SOI LIGBT structure combined with a dual implanted P-well as shown in Figure 2, which yields a latch-up current density of

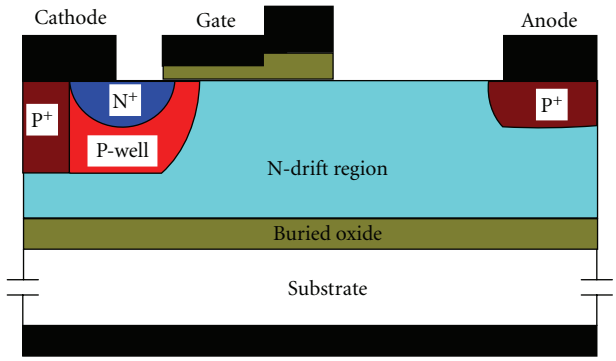


Figure 1: Cross-section of a conventional SOI NLIGBT.

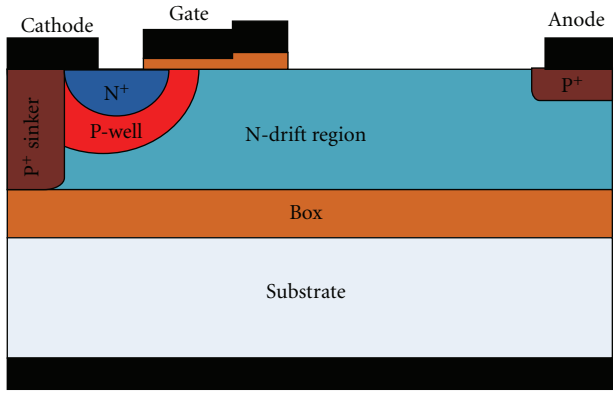


Figure 2: Cross-section of P^+ sinker SOI LIGBT.

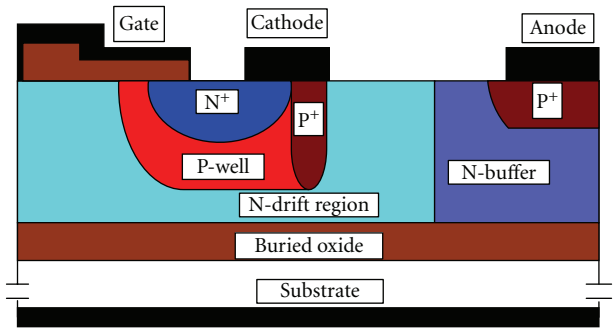


Figure 3: Cross-section of middle emitter SOI LIGBT.

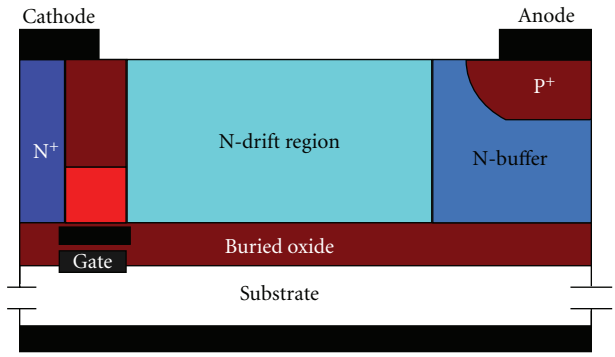


Figure 4: Cross-section of back channel SOI LIGBT.

1355 A/cm^2 with a 30 V gate-source drive voltage at the cost of adding some complexity to the fabrication process [11]. Sumida et al. proposed a middle emitter SOI LIGBT structure as illustrated in Figure 3, which showed about 3.5 times and 5.5 times improvement of dynamic latch-up current density at R.T. and at 125°C, respectively, with an increment about 0.8 V of on-state voltage drop [14].

Park et al. proposed a buried gate SOI LIGBT shown in Figure 4, the latch-up current density of which is 4140 A/cm^2 on condition that the thickness of SOI film, the doping concentration, channel length, threshold voltage, and drift region length are 1 μm, 10^{16} cm^{-3}, 1.5 μm, 2.0 V, and 15 μm, respectively, at the cost of much complexity and less agility of partial SOI processes [15]. Liang et al. put forward that a metal sinker could be used to replace the P^+ sinker shown in Figure 2 and further penetrate the buried oxide layer, which improves heat transfer and diverts holes current to substrate so that the latch-up effect could be suppressed to some extent [16]. Choi et al. proposed a dual-channel SOI LIGBT, which seems like a combination of the middle emitter structure and the conventional structure as illustrated in Figure 5 and a four times improvement of latch-up current density is obtained [17]. In [18], a new small sized lateral trench electrode insulated gate bipolar transistor (LTEIGBT) was proposed. Its latch-up current density was 1230 A/cm^2, which appears about a 10 times high as that of LIGBT and a 2.3 times high as that of LTIGBT.

2. Our Researches on Vertical Gate SOI LDMOS/LIGBT

In [21] we proposed a vertical gate (VG) SOI LDMOS structure named TGFPTD SOI LDMOS as shown in Figure 6, which consists of an N^+ source, a vertical gate and plate, a P-well tied to the N^+ source via a heavily doped P^+ contact, a lateral N-drift region, an N-buffer region, and a step-type trench drain. Thus, it is featured of low on-state voltage drop, low on-state static resistor, and high off-state breakdown voltage. Moreover, it was proved feasible to fabricate in advanced SOI CMOS technologies by 2D TCAD simulation and its channel length could be controlled down to about 130 nm [22].

In order to improve latch-up immunity of SOI LIGBT further, we proposed a vertical gate (VG) RF SOI LIGBT structure based on all the achievements above as illustrated in Figure 7. The proposed VG RF SOI LIGBT was also proved feasible to fabricate in advanced SOI CMOS technologies and its channel length could be controlled down to about 170 nm by process simulation with Silvaco TCAD [19]. From Figure 7 it could be obviously predicted that the hole current component flows through the P^+ collector region completely, which could effectively eliminate the regenerative feedback couple between the parasitic dual-transistors and increase latch-up current density of VG RF SOI LIGBT by alleviating the impact of the parasitic lateral resister under the N^+ source region in P-well. Moreover, the N-buffer region and the N^+-shorted anode can further reduce the current gain of the

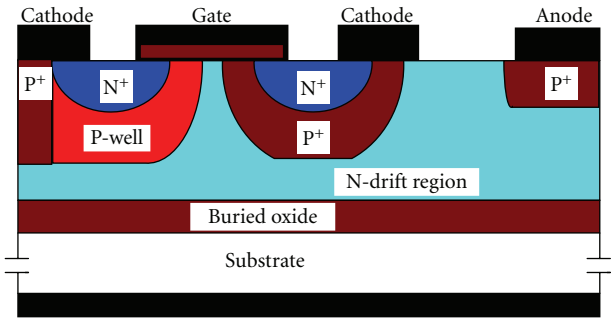


Figure 5: Cross-section of dual-channel SOI LIGBT.

lateral PNP transistor and restrict hole injection through its emitting PN junction, which might improve the latch-up current density further [20].

3. Device Structure and Basic Principle of VG SOI LIGBT

The proposed device structure of VG radio frequency (RF) SOI NLIGBT is illustrated in Figure 7. As can be seen in Figure 7 the proposed device cell consists of an SOI substrate, a top layer of silicon film on the SOI substrate, a thick field oxide layer on the silicon film, a vertical gate short channel NMOSFET with a deep trench gate and gate plate on one side of the silicon film, a low doped N-drift region in the middle of the silicon film, a heavier doped N-buffer region adjacent to the N-drift region, a P-P^+ anode and a shallow N^+ shorted anode with a drain metal electrode, and plate contacted on the other side.

The basic operation principle of the VG RF SOI LIGBT is very similar to that of an assembly of a VG MOSFET and a PNP BJT with a wide base region as the substrate is grounded. Take VG RF SOI NLIGBT for example, it lies in the off state when the gate-source bias voltage V_{gs} is less than the threshold voltage of its built-in VG nMOSFET V_{th} and the drain-source bias voltage $0 < V_{ds} < BV_{ds}$, where BV_{ds} represents the breakdown voltage. It can be turned on as $V_{gs} > V_{th}$ and $0 < V_{ds} < BV_{ds}$. At the same time, plenty of electrons injected from source electrode flow through the channel of the NMOSFET and swarm into the accumulative region beside the trench gate plate isolated by the vertical gate oxide. Then they spread out in n-drift region along both vertical and horizontal dimensions and drift toward drain electrode as can be seen in Figure 7 indicated by $-i_e$. While the voltage drop across the PN-buffer junction approaches its turn-on voltage due to $-i_e$ flowing through N-buffer region and N^+ shorted anode, a lot of holes are injected from P anode into N-buffer region and drifting toward P^+ source as well as recombining with electrons in N-buffer region and N-drift region simultaneously as can be seen in Figure 7 indicated by i_h and i_r, respectively. Injection of vast ambipolar carriers plasma into N-drift region and N-buffer region leads to a significantly reduced specific on-resistance due to conductance modulation effect so that a desired on-state drain current as well as an enough low on-state voltage drop could be

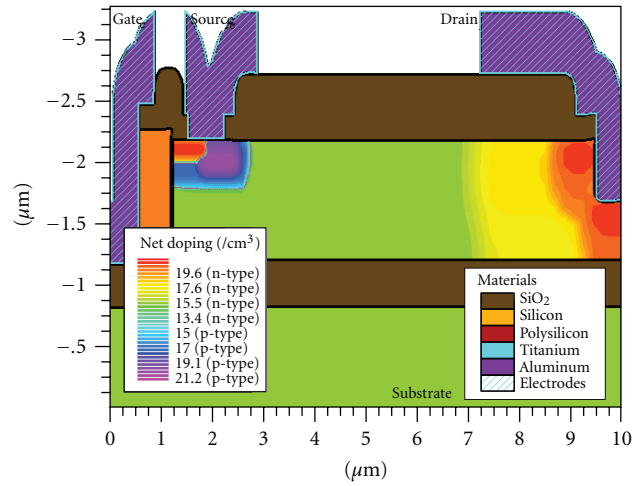


Figure 6: Cross-section of vertical gate SOI LDMOS.

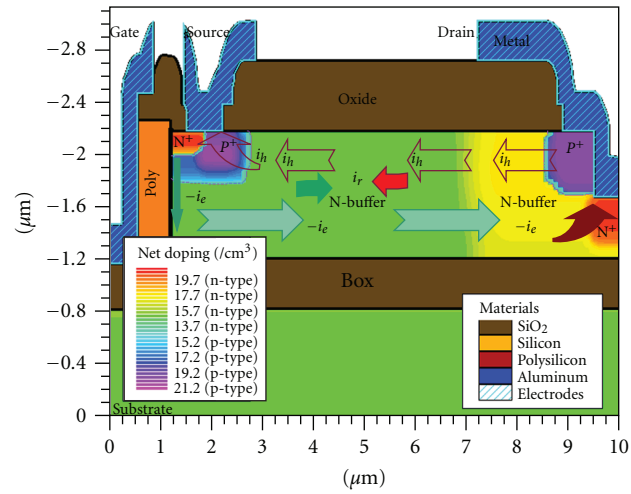


Figure 7: Cross-section of vertical gate SOI LIGBT.

obtained for the proposed VG RF SOI NLIGBT. Whether the proposed VG RF SOI NLIGBT is in the on state or breakdown state, its hole current component could mainly be bypassed through the P^+ contact region in P-well which could alleviate and even eliminate the regenerative feedback couple between the parasitic dual-transistors so that its latch-up immunity could be significantly improved further.

4. Modeling for Latch-Up Effect of VG SOI LIGBT

As can be seen in Figure 7 a parasitic thyristor structure exists in the VG SOI NLIGBT cell, which consists of N^+ source/P-well/(N-drift and N-buffer regions)/P-P^+ anode. The dual-bipolar-transistor equivalent circuit of the parasitic thyristor is illustrated in Figure 8. All parameters and symbols in Figure 8 are outlined in Table 1.

Table 1: All parameters and symbols in Figure 8.

V_{dd}	Power supply	R_{de}	Resistance of drift region for electron current
Z_L	Load impedance	R_{nb}	Resistance of n-buffer region
V_{gs}	Bias voltage between gate and source electrodes	R_{pp}	Resistance of pinched P-well region
Gnd	Ground	R_{dh}	Resistance of drift region for hole current
M_V	VG MOSFET	T_L	Lateral transistor
T_V	Vertical transistor	V_{ds}	Output

Based on the proposed device structure, a good approximation of latch-up current can be derived by solving the current required to establish a voltage drop across the pinched vertical P-well/P$^+$ contact region which is sufficient to forward-bias the P-well/N$^+$ source junction. This approximation may be expressed as

$$I_{\text{latch}} = \frac{V_{\text{on}}^{\min}}{R_{\text{pp}}} + I_{\text{ch}}, \tag{1}$$

where $V_{\text{on}}^{\min}$ is the minimum turn-on voltage of emitter junction of the parasitic vertical NPN transistor T_V by considering the distribution of impurities in these regions, which may be expressed as

$$V_{\text{on}}^{\min} = \frac{k_0 T}{q} \ln \frac{N_{\text{dm}} N_{\text{am}}}{n_i^2}, \tag{2}$$

where k_0 is the Boltzmann constant, T is the thermodynamics temperature, q is the absolute value of electron charge quantity, N_{dm} is the minimum pure impurity concentration in N$^+$ source region, N_{am} is the minimum pure impurity concentration in pinched P-well/P$^+$ contact region, and n_{i} is the intrinsic carrier concentration of silicon and may be approximately expressed as

$$n_i = 4.82 \times 10^{15} M_r^{3/4} T^{3/2} \exp\left(-\frac{E_g(T)}{2kT}\right), \tag{3}$$

where M_r is the rate between product of effective carriers' mass and square of static mass of free electron and may be approximately expressed as [23]

$$M_r = \frac{m_n^* m_p^*}{m_0^2} = 0.7990 + 6.87 \times 10^{-4}(T - 350). \tag{4}$$

E_g represents energy gap of silicon which is a function of thermodynamics temperature [23], R_{pp} represents the parasitic resistance of pinched vertical P-well/P$^+$ contact region per unit width. By considering the cross-section structure and the distribution of boron atoms in the pinched vertical P-well/P$^+$ contact region, a dual trapezoid cross-section and vertical local linear approximation of boron distribution

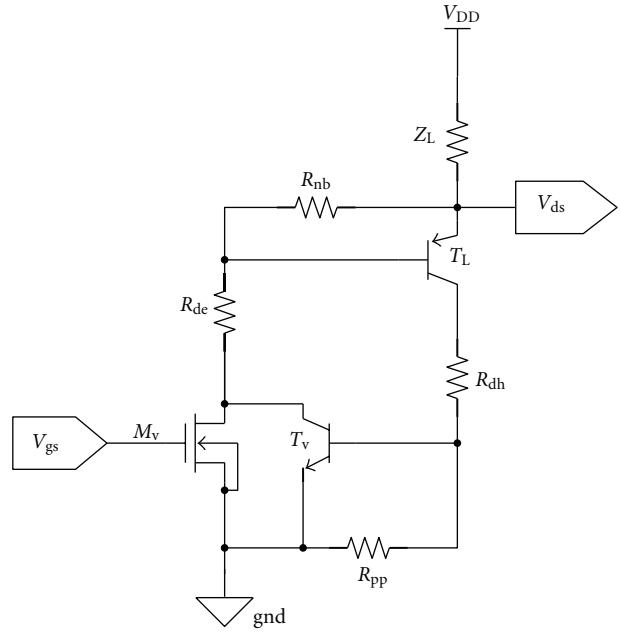


Figure 8: Equivalent circuit of the parasitic thyristor in the VG SOI nLIGBT cell.

was adopted since the thickness of N$^+$ source is only about 0.2 μm. Thus, R_{pp} may be derived out as

$$\begin{aligned} R_{\text{pp}} &\approx -\frac{1}{3 \times 5.0e20 \cdot q\mu_p} \int_0^{0.07} \frac{dx}{0.90 - 3x} \\ &\quad + \frac{12}{5.0e20 q\mu_p} \int_0^{0.12} \frac{dx}{(1 - 8x)(8.28 - 31x)} \\ &\approx \frac{1}{240\mu_p} \ln \frac{30}{23} + \frac{3}{20\mu_p} \ln 1.077, \end{aligned} \tag{5}$$

where μ_p is hole mobility in bulk silicon. It was deduced by element integral method with independent 2D coordinates for each trapezoid approximation illustrated in Figure 9. I_{ch} is saturated channel current of the built-in nMOSFET in the VG RF SOI LIGBT cell which may be approximately expressed as

$$I_{\text{ch}} = \frac{\mu_{ns} C_g W_{\text{ch}}}{2L_{\text{ch}}} \left(V_{\text{gs}} - V_{\text{th}}\right)^2, \tag{6}$$

where μ_{ns} is surface electron mobility, C_g is capacitance density of gate capacitor, W_{ch} is channel width of the built-in nMOSFET, and L_{ch} is effective channel length.

The latch-up currents at room temperature and 600 K could be obtained, respectively, by substituting (2), (3), (5), and (6) into (1) and simplifying

$$\begin{aligned} I_{\text{latch}}^0 &\approx \frac{V_{\text{on0}}^{\min}}{R_{\text{PP}}^0} \approx 93.31\,\mu_{p0} \quad (\text{A.V.S/cm}^3) \\ I_{\text{latch}}' &\approx \frac{V_{\text{on}}^{\min\prime}}{R_{\text{PP}}'} \approx 51.62\,\mu_p' \quad (\text{A.V.S/cm}^3) \end{aligned} \tag{7}$$

where V_{on0}^{min} and $V_{on}^{min\prime}$ are the minimum turn-on voltages of emitter junction of the parasitic vertical transistor T_V at room temperature and at 600 K, respectively, R_{PP}^{0} and $R_{PP}^{\prime}$ are the parasitic resistances of pinched vertical P-well/P^+ source region per unit width at room temperature and at 600 K respectively, μ_{p0} and $\mu_p^{\prime}$ are hole mobility in degenerated silicon at room temperature and at 600 K, respectively.

5. Analysis of Latch-Up Immunity

The P-type impurity concentration of low doped P-well region is about 10^{17}–10^{18} cm^{-3} whether in conventional SOI LIGBT or in the proposed new SOI LIGBT structures mentioned above. However, the P-type impurity concentration of P^+ contact region is about 10^{20}–10^{21} cm^{-3} nearly in all SOI LIGBT structures. Therefore, the parasitic resistivity of pinched vertical P-well/P^+ contact region is about 10^3 $\Omega\cdot$cm orders less than that of pinched lateral P-well region. Thus, in order to trigger the regenerative feedback of the parasitic thyristor in the proposed device, a much higher hole current is required flowing through the pinched P^+ contact region to establish a high enough voltage drop across it than in the device structures mentioned in Figures 3–5 and 7. Consequently, the proposed device structure is featured of much higher latch-up immunity.

Besides, one of the main differences among our proposed device structure and those in Figures 3–5 is that a shallow trench N^+ shorted anode is inserted in the drain region, through which a part of electron current component can be extracted directly to the drain electrode whether in the on state or during turn-off course that may significantly alleviate the over injection of hole across the P^+-N-drift or P^+-N-buffer junction and reduce the turn-off current tail. These might be improved further by inserting a P anode region between n-buffer region and P^+ anode region as illustrated in Figure 7. As a result, the parasitic thyristor may be triggered very difficultly due to almost completely decoupling between the parasitic dual-transistors in our proposed VG RF SOI LIGBT device structure.

Consequently, the values of latch-up currents at room temperature and 600 K could be calculated at about 39.20 MA/cm^2 and 15.49 MA/cm^2, respectively, by substituting the device parameters given in Figure 7 into (7), which is a few orders of magnitude higher than those reported in [11, 14–18]. That is to say, the device structure proposed in Figure 7 is characterized by very high latch-up immunity in theory.

6. Simulation Results and Discussion

The simulated cross-section view of VG RF SOI NLIGBT with TCAD ATHENA in advanced SOI CMOS VLSI technologies is illustrated in Figure 7, which demonstrates that the proposed device structure is feasible to fabricate with advanced SOI CMOS VLSI technologies. Our simulated current-voltage characteristic with $V_{gs} = 0$ V at room temperature is illustrated in Figure 10. As can be seen in Figure 10 the proposed VG RF SOI NLIGBT appears as a weak snap back phenomenon at about 75 V drain-source voltage due to BJT behavior, which is much higher in magnitude than the breakdown voltage of conventional SOI LIGBT at about 20 V and those of other improved versions at about 40–50 V with similar drift region length and other related structure parameters [11, 14–18, 24–26]. The proposed VG RF SOI NLIGBT was not broken down until drain-source voltage is beyond 94 V, which is even 19 V higher in magnitude than its snapback voltage. This might be explained by the idea that the parasitic thyristor is prevented from being triggered and broken down prematurely mainly due to bypassing of hole current directly through P^+ contact region in P-well.

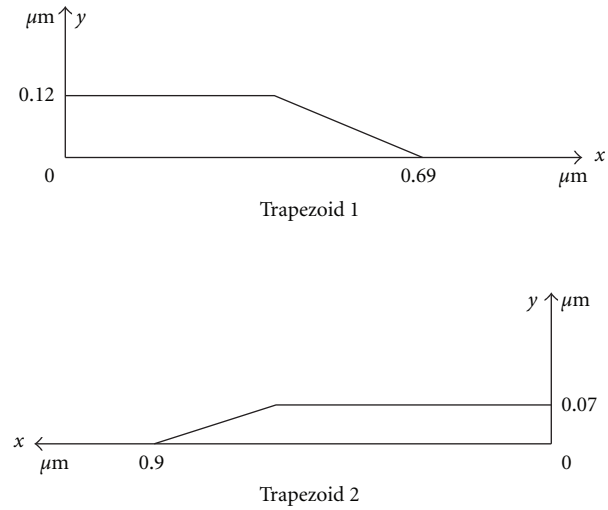
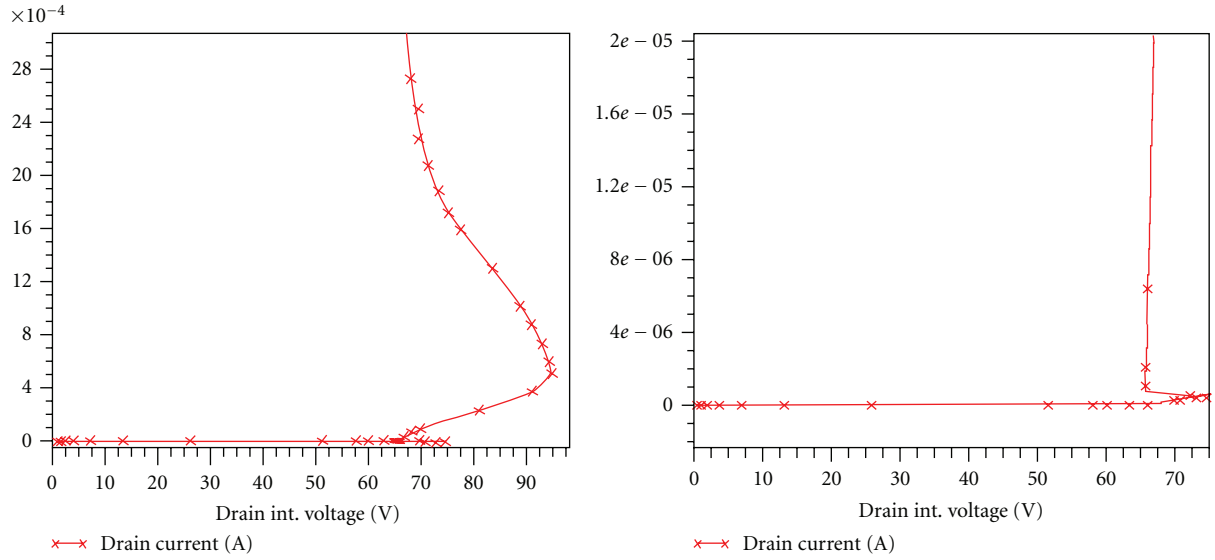


Figure 9: Independent 2D coordinates for dual trapezoid approximation of pinched P^+ source region.

Furthermore, the simulated latch-up current at room temperature could be reversely derived out at about 106.1 kA/cm^2 in linear approximation conservatively, which is still much higher in magnitude than those reported in references [11, 14–18].

Figure 11 illustrates the 2D distribution of current flow lines along the cross section of the proposed device structure in the breakdown state at room temperature. Figure 12 illustrates the 2D distribution of hole current component along the cross-section of the proposed device structure in the breakdown state at room temperature. Figure 13 illustrates the 2D distribution of electron current component along the cross-section of the proposed device structure in the breakdown state at room temperature.

There may be a few arguments deduced from Figure 11 to Figure 13. The first one is that the hole current of the proposed VG RF SOI NLIGBT is fully bypassed through P^+ well contact region even in the breakdown state at room temperature. The second one is that the impact ionization mainly happens in the depleted region adjacent to drain region. The third one is that there may be a inversion layer generated on the interface between silicon film and buried oxide at a certain bias condition which conducts a considerable hole current component so that a vertical hole current component



(a) Simulated current-voltage characteristic at $V_{gs} = 0.4$ V

(b) Amplified current-voltage characteristic in green rectangle region

FIGURE 10: Simulated current-voltage characteristic of VG RF SOI NLIGBT at $V_{gs} = 0.4$ V.

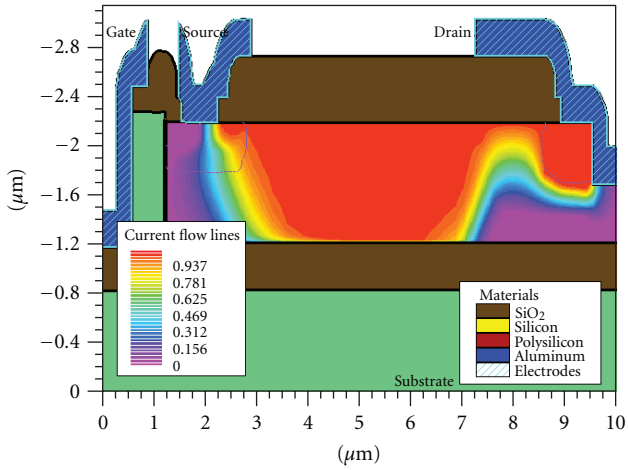


FIGURE 11: 2D distribution of current flow lines along the cross-section of the proposed device structure in the breakdown state at room temperature.

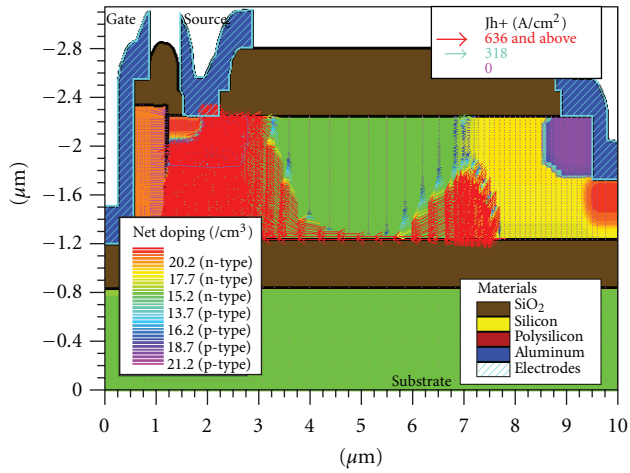


FIGURE 12: 2D distribution of hole current along the cross-section of the proposed device in the breakdown state at room temperature.

and a fly-back lateral current component flow through P-well toward P^+ contact region in the off state that was neglected in modeling for latch-up effect of VG RF SOI LIGBT mentioned above. The fourth one is that very little hole current is injected from P anode which manifests that the breakdown current mainly consists of impact ionization current components and reverse drifting current components. Consequently, the generative feedback between the parasitic vertical NPN transistor and lateral PNP transistor is not turned on even in the breakdown state at room temperature.

Figure 14 illustrates the 2D distribution of electron current component along the cross-section of the proposed device structure in the on state at room temperature. Figure 15 illustrates the 2D distribution of hole current component along the cross-section of the proposed device structure in the on state at room temperature. As can be seen in Figure 14 the trace of electron current component along the cross-section of the proposed VG RF SOI NLIGBT appears as a horizontal "S" shape in the on state at room temperature which originates from N^+ source electrode, flows through vertical N-type channel, congregates along vertical accumulation layer, expends into and travels through lateral N-drift region and N-buffer region in turn, bypasses the corner of P anode, penetrates the N^+ shorted anode, and swarms into drain electrode. This might be mainly ascribed to a few phenomena as follows.

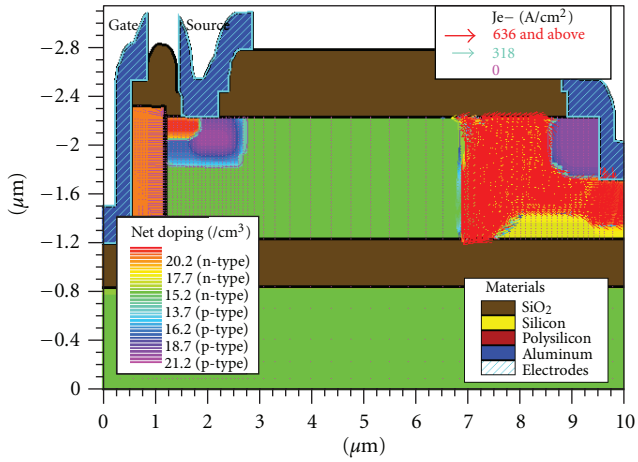


Figure 13: 2D distribution of electron current along the cross-section of the proposed device in the breakdown state at RT.

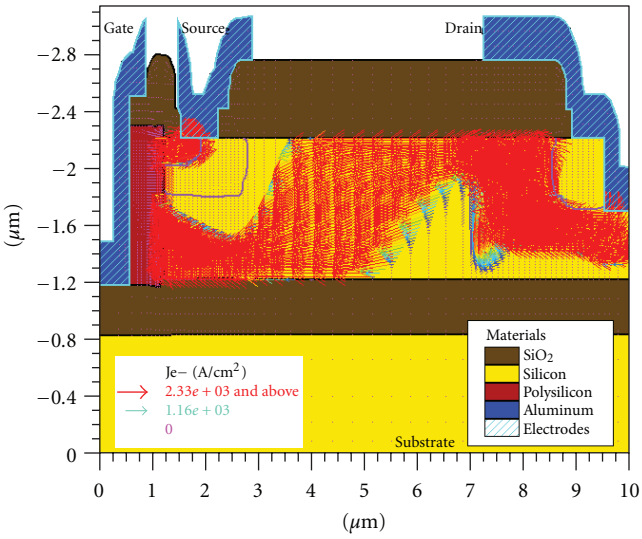


Figure 14: 2D distribution of electron current along the cross-section of the proposed device in the on state at room temperature.

(i) Electrons are injected through the vertical channel controlled by the vertical gate and accumulate beside the vertical gate plate isolated by vertical gate oxide.

(ii) A depletion layer exists in the N-drift region beside the P-well/N-drift junction due to pseudo-JFET effect.

(iii) Charge attraction force works since an electric field is built in drift region between heavily injected holes from P anode into N-buffer and N-drift region which is shown in Figure 15 and heavily injected electrons through vertical channel into N-drift and N-buffer region.

(iv) Static Coulomb force works since substrate is grounded.

(v) Impedance exists across the potential barrier of P/N-buffer junction.

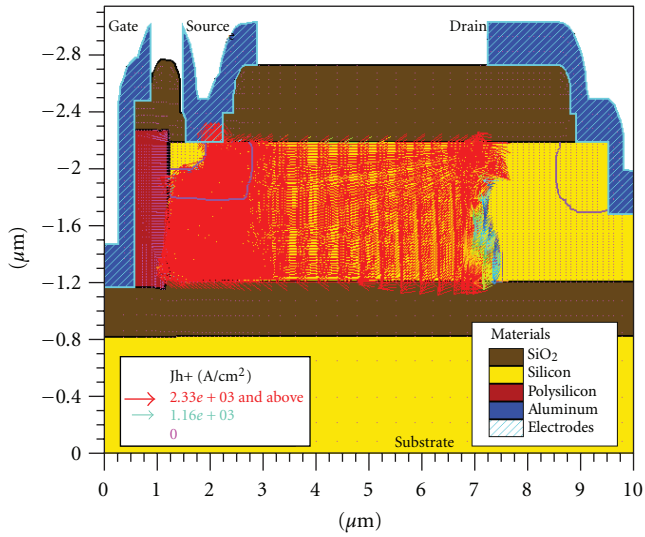


Figure 15: 2D distribution of hole current along the cross-section of the proposed device in the on state at room temperature.

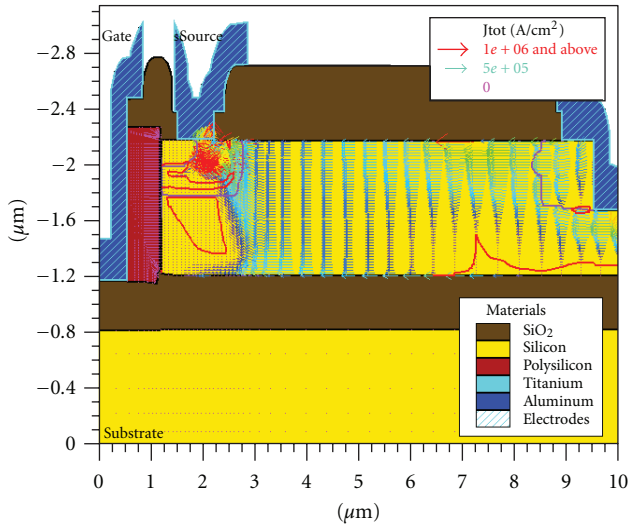


Figure 16: Simulated 2D distribution of latch-up current density of the proposed device in near critical latch-up state.

(vi) Electrons are extracted through N^+ shorted anode.

As can be seen from Figure 15 a considerable vertical hole current component exists through the part of N-drift region under P-well and an obvious fly-back lateral current component exists also in the on state, which flows through P-well toward P^+ contact region. Total on-state current density is about 4660 A/cm^2 and above at $V_{gs} = 4.0$ V.

However, even in the on state there is not any minor current observed in P-well which indicates that the parasitic vertical NPN transistor is still in the off state. In other words, the parasitic thyristor is still untriggered due to the full decouple between the parasitic dual-transistors.

Figure 16 illustrates simulated 2D distribution of latch-up current density of the proposed device structure in near critical latch-up state. As can be seen from Figure 16 the

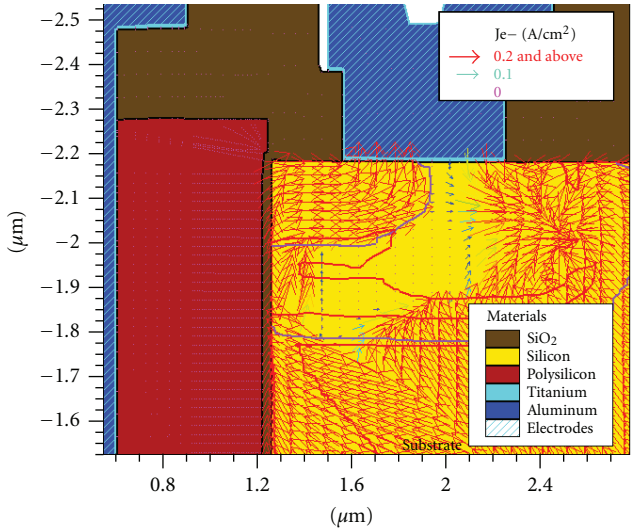


FIGURE 17: Triggering of the parasitic dual-transistors in the proposed device structure in near critical latch-up state.

latch-up current density is about in the order of 1 MA/cm^2 and above, which is approximately an order of magnitude higher than that reversely derived out according to Figure 10 and about an order lower of magnitude than that calculated from the latch-up model established above.

Based on the latch-up model, an injected electron current from N^+ source into P-well at a certain point on the interface of the N^+ source/P-well junction should exist as the proposed device lies in latch-up state. This is indicated by Figure 17 which shows that a very low electron current flows through P-well region at its fingertip in near critical latch-up state. The very low electron current indicates that the parasitic vertical NPN transistor is driven into the on state and the regenerative feedback couple between the parasitic dual-transistor is wakened up simultaneously.

7. Conclusion

Based on the researches and analyses above, it could be concluded that the latch-up current of our proposed VG RF SOI NLIGBT at room temperature might be about two orders higher in magnitude than those of previously proposed device structures since the hole current component is mostly bypassed by P^+ well contact region; the proposed VG RF SOI NLIGBT might be characterized by very high latch-up immunity whether it is in the off state or the on state and its breakdown voltage in the off state is about 2.0–4.7 times higher in magnitude than those before. Therefore, our proposed VG RF SOI NLIGBT will be more suitable for SPICs-related applications.

Furthermore, the device structure and process parameters of VG RF SOI NLIGBT may be optimized further to improve its latch-up immunity and our latch-up current model of the proposed VG RF SOI NLIGBT is a little crude due to some idealized assumptions and might be modified further according to simulation results and/or silicon verification in the future.

Moreover, it is suggested that the parasitic latch-up effect of SOI LIGBT be utilized to improve some of its main electric performances by combining with the BPL SOI substrate [27, 28], the integrated anti-ESD structure [29, 30], and the structure of thyristor so as to break through the ceilings of both on-state current and forward block voltage based on the proposed VG RF SOI NLIGBT structure.

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References

[1] B. J. Baliga, M. S. Adler, P. V. Gray, and R. P. Love, "The insulated gate rectifier (IGR): a new power switching device," in *Proceedings of the International Electron Devices Meeting. Technical Digest (IEDM Tech. Digest '82)*, pp. 264–267, 1982.

[2] J. P. Russell, A. M. Goodman, L. A. Goodman, and J. M. Neilson, "The COMFET—new high conductance MOS-gated device," *IEEE Electron Device Letters*, vol. 4, no. 3, pp. 63–65, 1983.

[3] J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, and N. D. Zommer, "The insulated gate transistor: a new three-terminal MOS-controlled bipolar power device," *IEEE Transactions on Electron Devices*, vol. 31, no. 6, pp. 821–828, 1984.

[4] M. Darwish and K. Board, "Lateral resurfed COMFET," *Electronics Letters*, vol. 20, no. 12, pp. 519–520, 1984.

[5] M. R. Simpson, P. A. Gough, F. I. Hshieh, and V. Rumennik, "Analysis of the insulated gate transistor," in *Proceedings of the International Electron Devices Meeting. Technical Digest (IEDM Tech. Digest '85)*, pp. 740–743, 1985.

[6] A. L. Robinson, T. P. Chow, M. S. Adler, B. J. Baliga, and E. J. Wildi, "N-channel lateral insulated gate transistors: part I—steady state characteristics," *IEEE Transactions on Electron Devices*, vol. 33, no. 12, pp. 1956–1963, 1986.

[7] T. P. Chow, B. J. Baliga, D. N. Pattanayak, and M. S. Adler, "Effect of substrate doping on the performance of anode-shorted n-channel lateral insulated-gate bipolar transistors," *IEEE Electron Device Letters*, vol. 9, no. 9, pp. 450–452, 1988.

[8] T. P. Chow, D. N. Pattanayak, B. J. Baliga, M. S. Adler, W. A. Hennessy, and C. E. Logan, "Interaction between monolithic, junction-isolated lateral insulated-gate bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 38, no. 2, pp. 310–314, 1991.

[9] I. Wacyk, R. Jayaraman, L. Casey, and J. Sin, "Fast LIGBT switching due to plasma confinement through pulse width control," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, pp. 97–102, 1991.

[10] Y. S. Huang, B. J. Baliga, S. Tandon, and A. Reisman, "Comparison of DI and JI lateral IGBTs," in *Proceedings of the*

International Symposium on Power Semiconductor Devices and ICs, pp. 40–43, 1992.

[11] D. R. Disney and J. D. Plummer, "SOI LIGBT devices with a dual P-well implant for improved latching characteristics," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, pp. 254–258, 1993.

[12] I. Omura, N. Yasuhara, A. Nakagawa, and Y. Suzuki, "Numerical analysis of SOI IGBT switching characteristics—switching speed enhancement by reducing the SOI thickness," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, pp. 248–253, 1993.

[13] H. Neubrand, J. Serafin, M. Fullmann, and J. Korec, "Comparison of lateral EST and IGBT devices on SOI substrate," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, pp. 264–268, 1993.

[14] H. Sumida, A. Hirabayashi, and N. Kumagai, "The modified structure of the lateral IGBT on the SOI wafer for improving the dynamic latch-up characteristics," *IEEE Transactions on Electron Devices*, vol. 42, no. 2, pp. 367–370, 1995.

[15] H. Y. Park, S. H. Kim, and Y. I. Choi, "Buried gate SOI LIGBT without latch-up susceptibility," in *Proceedings of the IEEE International SOI Conference*, pp. 57–58, October 1998.

[16] Y. C. Liang, S. Xu, C. Ren, and J. Luo, "New SOI structure for LIGBT with improved thermal and latch-up characteristics," in *Proceedings of the 3rd IEEE International Conference on Power Electronics and Drive Systems (PEDS '99)*, pp. 258–261, July 1999.

[17] W. B. Choi, W. J. Sung, Y. I. Lee, and M. Y. Sung, "Dual-channel SOI LIGBT with improved latch-up and forward voltage drop characteristics," in *Proceedings of the 59th Annual Device Research Conference (DRC '01)*, pp. 53–54, June 2001.

[18] E. G. Kang and M. Y. Sung, "A small sized lateral trench electrode IGBT for improving latch-up and breakdown characteristics," *Solid-State Electronics*, vol. 46, no. 2, pp. 295–300, 2002.

[19] H. P. Zhang, L. L. Sun, L. F. Jiang, L. J. Ma, and M. Lin, "Process simulation of trench gate and plate and trench drain SOI NLIGBT with TCAD Tools," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS '08)*, pp. 1037–1040, December 2008.

[20] H. Zhang, B. Su, L. Sun, and D. Wang, "Vertical gate RF SOI LIGBT without latch-up susceptibility," in *Proceedings of the International Semiconductor Device Research Symposium (ISDRS '09)*, pp. 1–2, December 2009.

[21] H. P. Zhang, L. F. Jiang, L. L. Sun et al., "A novel SOI LDMOS with a trench gate and field plate and trench drain for RF applications," in *Proceedings of the 7th International Symposium on Communications and Information Technologies (ISCIT '07)*, pp. 34–39, October 2007.

[22] H. P. Zhang, L. L. Sun, L. F. Jiang, L. Y. Xu, and M. Lin, "Process simulation of trench gate and plate and trench drain SOI nLDMOS with TCAD tools," in *Proceedings of the IEEE International Conference on Semiconductor Electronics (ICSE '08)*, pp. 92–95, November 2008.

[23] H. P. Zhang, *Study on silicon based MOSFET and CMOS circuits for high temperature applications*, Doctoral thesis, Microelectronics Center, Southeast University, Nanjing, China, 2001, chapter 2.

[24] S. Merchant, E. Arnold, H. Baumgart et al., "Dependence of breakdown voltage on drift length and buried oxide thickness in SOI RESURF LDMOS transistors," in *Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs*, pp. 124–128, 1993.

[25] S. Zhang, J. K. O. Sin, T. M. L. Lai, and P. K. Ko, "Numerical modeling of linear doping profiles for high-voltage thin-film SOI devices," *IEEE Transactions on Electron Devices*, vol. 46, no. 5, pp. 1036–1041, 1999.

[26] R. Tadikonda, S. Hardikar, and E. M. S. Narayanan, "Realizing high breakdown voltages (>600 V) in partial SOI technology," *Solid-State Electronics*, vol. 48, no. 9, pp. 1655–1660, 2004.

[27] S. G. Xu, H. P. Zhang, D. J. Wang et al., "Forward block characteristic of a novel SOI LDMOS with a buried P-type layer," in *Proceedings of the IEEE International Silicon on Insulator Conference (SOI '10)*, pp. 88–89, October 2010.

[28] H. P. Zhang, R. S. Qi, W. L. Zhao et al., "Forward block characteristic of a novel anti-ESD RF SOI LIGBT with a buried P-type layer," in *Proceedings of the IEEE China-Japan Microwave Conference*, 2011.

[29] H. P. Zhang, L. Zhang, D. J. Wang et al., "Positive ESD robustness of a novel anti-ESD TGFPTD SOI LDMOS," in *Proceedings of the IEEE International Conference on Computer applications and Industry Electronics*, pp. 5022–5025, 2010.

[30] H. P. Zhang, L. Zhang, D. J. Wang et al., "Negative ESD robustness of a novel anti-ESD TGFPTD SOI LDMOS," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems*, pp. 1227–1230, 2010.