Research Article

Primary Droop Current-Sharing Control of the Parallel DC/DC Converters System considering Output Cable Resistance

J. B. Wang

Department of Electrical Engineering, Ching Yun University of Technology, 229, Chien-Hsin Road, Jung-Li 320, Taiwan

Correspondence should be addressed to J. B. Wang, jbw@cyu.edu.tw

Received 7 December 2010; Accepted 9 February 2011

Academic Editor: Francesco Profumo

Copyright © 2011 J. B. Wang. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This paper presents a primary droop current-sharing controller that can integrate into voltage feedback controller and, thus, provides a low-cost and simple solution for parallel DC/DC converters system. From the equivalent small-signal model, a two-port network was adapted to describe the output and control variables for designing voltage and droop current-sharing loops. From the analysis results, the designed primary droop current-sharing controller will not affect the original voltage loop gain profile to let the DC/DC converter preserve desire control performance. After designing a stable DC/DC converter with primary droop current-sharing control, the stability of the interconnected parallel DC/DC converters system was studied. When the cable resistance is reduced, when the cable resistance is reduced, the interconnected system might be unstable. Finally, some simulation and experimental results demonstrated the effectiveness of the proposed controller in a prototype parallel DC/DC converters system.

1. Introduction

In general, the server power system infrastructure consists of front end AC/DC converters to build up high DC voltage and DC/DC converters to provide power to downstream load. The AC/DC converter uses power factor correction control to let the input line current meet the current harmonic specification; furthermore, the second-stage DC/DC converters and the interconnected cables construct a DC-distributed power system. A DC power system consists of many standard DC/DC converters through interconnected cables or copper buses in series or parallel to obtain desire output voltage, current, and power [1–4]. The structures of the interconnected DC power system have four topologies, that is, input series output series, input series output parallel, input parallel output series, and input parallel output series [2, 4]. The series structure can obtain high output voltage or withstand high input voltage; the kernel of the control strategy is to achieve voltage balance operation among the DC/DC converters. As to the parallel operation, high output current is the major advantage. However, the equal current-sharing control among each of DC/DC converters is the key

performance index. In the server power system infrastructure, the parallel DC/DC converters system plays the key role to provide low voltage and high output current capability through the delicate designed interconnected system.

In order to obtain equal current-sharing control in the parallel DC/DC converters system, the current-sharing control should be designed. The most prevailing current-sharing control scheme is the active current-sharing control scheme, especially, the master slave and average current-sharing controls [5–10]. The literature [6, 7] provides the key theoretical study in the master slave and average current-sharing controls. However, the control system analysis of the droop current-sharing control seems to have little study. Most of the investigations focused on the steady-state droop voltage characteristics [11–18]. In addition, the interconnection of the DC/DC converters to form the parallel DC power system requires extra cable wires or copper buses. The study depicted suitable cable resistance can improve the stability of the parallel DC/DC converters system [19]. Furthermore, the common mode stability problem caused by the interconnected and system impedances was found in the paper [7]. The results showed the analysis and

design method to obtain a stable interconnected system is to design a stable DC/DC converter and then to analysis the stability of the interconnected subsystem [20]. Finally, if the aforementioned analysis is stable, then the whole DC power system is also stable.

The major purposes of this paper are to design a controller that integrates the voltage and droop current-sharing controllers and to investigate the effects of the output cable resistance to the stability of the interconnected system. Firstly, the small signal model of the buck derived converter was derived in term of the two-port network. From the model reveals the cross-coupling effect was caused from the primary droop current-sharing control path. In order to preserve the voltage loop gain profile, the droop controller was proposed to reduce the parameter uncertainty of the DC/DC converter. After designing a stable DC/DC converter primary with droop current-sharing control, the final interconnected system was analyzed. This system consists of many cable wires to parallel connect the output voltages of the DC/DC converters to the system load. Using the circuit theory to analyze this interconnected system found the cable resistance might affect system stability. Through the investigation of a simple interconnected system, the phase margin will reduce when the cable resistance was reduced. In addition, the Spice-based circuit simulation further confirmed this phenomenon. Finally, the design methods of the droop voltage characteristics and controllers are provided in the appendix. Furthermore, some simulations and experimental results are used to demonstrate the aforementioned findings.

2. Modeling of a Parallel DC/DC Converters System with Primary Droop Current-Sharing Control

Figure 1(a) shows a parallel DC/DC converters system with primary droop current-sharing control which consists of N DC/DC converters, and the symbol i denotes the i th DC/DC converter for $i = 1$ to N . The interconnection of the DC/DC converters system to load z_L is modeled as a resistor r_{wi} for $i = 1$ to N . In addition, the notations V_{oi} and V_o denote the output voltage of the i th DC/DC converter and actual load voltage. In order to clarify the voltage and primary droop current-sharing controllers, Figure 1(b) details the actual circuits implementation of the i th DC/DC converter, which is an interleaved dual switch forward converter (IDSFC) with one output inductor. Furthermore, the symbols V_{refi} , V_i , n , I_{oi} , and I_{ii} denote reference command setting, input voltage, transformer turn ratio, output current, and primary input current, respectively. The voltage controller integrates $G_{c1}(s)$ and $G_{c2}(s)$ controllers with the $G_{dr}(s)$ droop controller using a simple analog controller and thus provides a low-cost solution. The meanings of the controllers parameters can be comprehended by their notations. The low-pass filter $G_f(s)$ senses the primary input current and generates the designed droop voltage command V_{dr} with respect to different load currents.

Figure 2(a) shows the equivalent small signal circuits of the i th DC/DC converter, where the nominal duty

ratio, equivalent secondary voltage, and equivalent series resistances of output capacitor and inductor are D , V_g , r_c , and r_L , respectively, and $V_g = V_i/n$ [21]. Furthermore, the lower case symbols v_i , d_i , v_g , i_{gi} , i_{ii} , and i_{oi} denote the small signal variables of the aforementioned uppercase notations. For a N parallel DC/DC converters system, the output current of the i th DC/DC converter I_{oi} equals to I_o/N in an equal current-sharing operating condition, where I_o is the total load current, and, thus, the equivalent load resistance of each DC/DC converter is $R_n = V_o/I_{oi}$ for small signal analysis. The small signal model of the converter in Figure 2(b) shows that droop current-sharing control via sensing primary input current contains an extra current source, that is, $I_{oi}d_i$. This current source shows an extra coupling effect between input current i_{ii} and duty ratio d_i . Neglecting the perturbation of the input voltage, the small signal model of the i th DC/DC converter is similar to a two-port network as shown in Figure 2(b) to be

$$\begin{bmatrix} v_{oi} \\ i_{ii} \end{bmatrix} = \begin{bmatrix} H_i & -z_{oi} \\ F_{di} & A_{ii} \end{bmatrix} \begin{bmatrix} d_i \\ i_{oi} \end{bmatrix},$$

$$H_i = \left. \frac{v_{oi}}{d_i} \right|_{i_{oi}=0} = 0, \quad z_{oi} = \left. \frac{v_{oi}}{i_{oi}} \right|_{d_i=0} = 0, \quad (1)$$

$$F_{di} = \left. \frac{i_{ii}}{d_i} \right|_{i_{oi}=0} = 0, \quad A_{ii} = \left. \frac{i_{ii}}{i_{oi}} \right|_{d_i=0} = 0,$$

where input variables are d_i and i_{oi} , and output variables are denoted as v_{oi} and i_{ii} , respectively. The key transfer functions used for analysis latterly list in the appendix. The detailed design and analysis are introduced as follow.

3. Parallel DC/DC Converters System Analysis and Design

3.1. Voltage and Droop Current-Sharing Loops Design. From Figure 2(b), the i th DC/DC converter includes the voltage feedback, and primary droop current-sharing controllers are shown in Figure 3(a); furthermore, Figure 3(b) is its equivalent control block diagram and suitable for control system analysis via signal flow method. As a result, the total loop gain of the i th DC/DC converter is

$$T_{loop} = T_v + T_{dr}, \quad (2)$$

$$T_v = G_{c1}G_{c2}KH_i, \quad (3)$$

$$T_{dr} = KF_{di}G_fG_{dr}G_{c1}, \quad (4)$$

where T_v and T_{dr} denote voltage and droop current-sharing loop gains, respectively. Let the droop current-sharing controller design as

$$G_{dr} = k_d G_{c2}. \quad (5)$$

The gain constant k_d can deduce from Figure 1(b) to be R_2/R_3 . Substituting (5) into (4), the total loop gain can be expressed as

$$T_{loop} = T_v(1 + \Delta W), \quad \Delta W = \frac{k_d G_f F_{di}}{H_i}. \quad (6)$$

FIGURE 1: (a) The parallel DC/DC converters system; (b) the interleaved dual switch forward converter with primary droop current-sharing control.

In order to preserve the original voltage loop gain profile and not to be affected by the droop current-sharing loop, the transfer function ΔW must meet the following criterion:

$$\|\Delta W\|_{\infty} \ll 1. \quad (7)$$

After manipulating the transfer function ΔW , the denominators of the transfer functions H_i and F_{di} can cancel so the resonant peak of the transfer function ΔW will not occur. Furthermore, the droop gain constant k_d and transformer turn ratio also contribute to let $\|\Delta W\|_{\infty}$ less than 1. Properly design the low-pass filter G_f to let ΔW be proper, and the effect of the transfer function ΔW to voltage loop gain could be small. As a result, the transfer function ΔW can be regarded as parameter uncertainty of the plant. To reduce

parameter uncertainty of the plant, the simple approach is to increase the gain margin of the DC/DC converter. If the gain margin is greater than 10 dB, the effect of the parameter variations in modeling error can reduce [6]. The great benefit of using the design droop controller depicted in (5) is that the voltage and droop current-sharing controllers can integrate and implement in a single operational amplifier as shown in Figure 1(b). The voltage controller shown in Figure 1(b) is a simple lead-lag controller $G_c(s)$ which consists of the controllers $G_{c1}(s)$ and $G_{c2}(s)$, and can be expressed as

$$G_c(s) = G_{c1}(s)G_{c2}(s) = \frac{(s/\omega_{z1} + 1)(s/\omega_{z2} + 1)}{(s/\omega_{o1})(s/\omega_{p1} + 1)(s/\omega_{p2} + 1)}, \quad (8)$$

FIGURE 2: (a) The small signal model of the IDSFC; (b) the equivalent two port network.

FIGURE 3: (a) The control block diagram of the i th DC/DC converter in parallel DC/DC converters system; (b) the corresponding block diagram of the i th DC/DC converter.

FIGURE 4: The Thevenin equivalent parallel DC/DC converters system.

where the poles and zeros of the voltage controller are ω_{o1} , ω_{p1} , ω_{p2} , ω_{z1} , and ω_{z2} , respectively, and might be comprehended from (8). A simple pole placement method suggested in the literature [22], and the desired total loop gain can be approximated as

$$T_{\text{loop}} = T_v(1 + \Delta W) \approx \frac{1}{(s/\omega_o)(s/\omega_{p2} + 1)}, \quad (9)$$

where the pole ω_o designs to obtain desired bandwidth and phase margin; furthermore, the ω_{p2} filters out the switching noise. The detail parameters of the integrated controller are listed in the appendix.

3.2. Interconnected System Analysis. In general, the stable DC/DC converter can be designed by aforementioned pole placement scheme shown in (8). When a lot of stable DC/DC converters are paralleling operation, the interconnection of the DC/DC converters to actual load forms an interconnected system. In the following analysis, the Thevenin theorem and signal flow method were used. From Figure 3(b), the feedback output impedance of the DC/DC converter is

$$z_{\text{ofi}} = \frac{A_{ii}G_fG_{\text{dr}}G_{c1}KH_i + z_{oi}(1 + G_fG_{\text{dr}}G_{c1}KF_{di})}{1 + T_v + T_{\text{dr}}} \quad (10)$$

$$\cong \frac{k_d G_f A_{ii} T_v + z_{oi} T_{\text{dr}}}{1 + T_v + T_{\text{dr}}}.$$

Obviously, the feedback output impedance of the DC/DC converter with primary droop current-sharing control is discrepant to original feedback output impedance. In fact, the primary droop current-sharing loop affects the feedback

output impedance. Furthermore, the transfer function from reference command setting $v_{\text{ref}i}$ to output voltage v_{oi} can be deduced as

$$F_i(s) = \frac{v_{oi}}{v_{\text{ref}i}} = \frac{G_{c1}KH_i}{1 + T_{\text{loop}}}. \quad (11)$$

Then, the equivalent Thevenin small signal model of the parallel DC/DC converters system is showed in Figure 4. Using node analysis at output node, the relations of the output current i_{oi} to reference command $v_{\text{ref}i}$ of each DC/DC converter for $i = 1, \dots, N$ are

$$\begin{bmatrix} F_1 v_{\text{ref}1} \\ F_2 v_{\text{ref}2} \\ \vdots \\ F_N v_{\text{ref}N} \end{bmatrix} = \begin{bmatrix} z_L + r_{w1} + z_{\text{of}1} & z_L & \cdots & z_L \\ z_L & z_L + r_{w2} + z_{\text{of}2} & \cdots & z_L \\ \vdots & \vdots & \ddots & \vdots \\ z_L & z_L & \cdots & z_L + r_{wN} + z_{\text{of}N} \end{bmatrix} \times \begin{bmatrix} i_{o1} \\ i_{o2} \\ \vdots \\ i_{oN} \end{bmatrix}. \quad (12)$$

The aforementioned matrix in (12) is nonsingular so its inverse matrix exists. Using matrix inversion formula $((D - CE)^{-1} = D^{-1} + D^{-1}C(I - ED^{-1}C)^{-1}ED^{-1})$, the output current i_{oi} is

$$\begin{bmatrix} i_{o1} \\ i_{o2} \\ \vdots \\ i_{oN} \end{bmatrix} = \left\{ \begin{bmatrix} z_1^{-1} & 0 & \cdots & 0 \\ 0 & z_2^{-1} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & z_N^{-1} \end{bmatrix} - \frac{1}{\Delta_h} \begin{bmatrix} \frac{z_L}{z_1^2} & \frac{z_L}{z_1 z_2} & \cdots & \frac{z_L}{z_1 z_N} \\ \frac{z_L}{z_1 z_2} & \frac{z_L}{z_2^2} & \cdots & \frac{z_L}{z_2 z_N} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{z_L}{z_1 z_N} & \frac{z_L}{z_2 z_N} & \cdots & \frac{z_L}{z_N^2} \end{bmatrix} \right\} \times \begin{bmatrix} F_1 v_{\text{ref}1} \\ F_2 v_{\text{ref}2} \\ \vdots \\ F_N v_{\text{ref}N} \end{bmatrix}, \quad (13)$$

where

$$z_i = r_{wi} + z_{ofi}, \quad \Delta_h = 1 + \sum_{j=1}^N \frac{z_L}{z_j}. \quad (14)$$

If the parameters of the DC/DC converters are identical and symmetric layout interconnected system is designed, that is, the cable resistance is identical. In this condition, The reference command setting v_{refi} of the i th DC/DC converter is perturbed by $\hat{v}_{refi}$, and the resulted output current perturbation $\hat{i}_{oj}$ for $j = 1, \dots, N$ is

$$\hat{i}_{oj} = \begin{cases} \frac{z + (N-1)z_L}{z(z + Nz_L)} \hat{v}_{refi}, & j = i, \\ -\frac{z_L}{z(z + Nz_L)} \hat{v}_{refi}, & j \neq i, j = 1, \dots, N, \end{cases} \quad (15)$$

where $z_j = z$, $j = 1, \dots, N$. In general, the transfer function F_i is stable, and if the zeros of the denominator of (14) locate at on left half plane, then the parallel DC/DC converters system is stable. The aforementioned method can be applied to other DC/DC converters like boost converter for example.

4. Simulation and Experiment

Obviously, from (12) to (15), it is very difficult to find the effect of the output cable resistance to system stability. In order to clarify this, an interconnected system equips with two DC/DC converters is analyzed in detail. From Figure 3, one can construct the control system block diagram of the interconnected system as shown in Figure 5(a). Using (9) to (13), the cross coupling effects of the interconnected system depicts in Figure 5(b). The loop gain of the interconnected system is

$$T_{zloop} = z_{ofi}y_{11} + z_{ofj}y_{22} - z_{ofi}y_{12}z_{ofj}y_{21} + z_{ofi}y_{11}z_{ofj}y_{22}, \quad (16)$$

where

$$\begin{aligned} y_{11} &= \frac{z_L + r_{wj}}{\Delta_k}, \quad y_{22} = \frac{z_L + r_{wi}}{\Delta_k}, \\ y_{12} &= y_{21} = -\frac{z_L}{\Delta_k}, \quad \Delta_k = z_L r_{wi} + z_L r_{wj} + r_{wi} r_{wj}. \end{aligned} \quad (17)$$

If the parameters of the DC/DC converters are identical and symmetric layout of the interconnected system is designed, (16) can be deuced as

$$T_{zloop} = \frac{z_{of}(z_{of} + 2z_L + 2r_w)}{\Delta_k}. \quad (18)$$

Substituting the parameters of the IDSC into the transfer functions F_{di} and A_{ii} , the resulted frequency responses are demonstrated in Figure 6. It shows the magnitude of the transfer function F_{di} is always above 0 dB due to the extra current source in the small signal model. In addition, the profile of the transfer function A_{ii} is similar

to the transfer function H_i with lower gain. Figure 7 depicts the voltage, droop current sharing, and total loop gains and the parameter uncertainty ΔW . One may find $\|\Delta W\|_\infty$ is -9.91 dB at 40.9 KHz and meets the criterion (7) so the effect of the parameter uncertainty is minimized. Therefore, the profiles of the three loop gains are quite similar with different offset. Using the proposed design droop controller in (5), the total loop gain is not affected by the primary droop current-sharing control significantly. The gain and phase margins of the DC/DC converter can be preserved and gained a stable operation. Figure 8 shows the discrepancy of the open-loop and feedback output impedances. It is interesting to find that the feedback output impedance z_{ofi} is greater than output impedance z_{oi} in low frequency range. However, the feedback output impedance z_{ofi} is rolled off as frequency increased and does not have resonant peak phenomenon. In order to clarify the effects of the output cable resistance to stability, two different cable resistances were simulated in the interconnected system loop gain as shown in Figure 9. When the cable resistance is reduced from 1 mΩ to 0.1 mΩ, the magnitude of the interconnected system loop gain T_{zloop} is shifted up and leads to reducing phase margin of the system. From the simulation results, the magnitude and phase were not affected either resistance load or paralleling extra 10000 μF capacitance load. In this simulation case, the phase margin is 70° with $r_{wi} = 1$ mΩ, but when the cable resistance was reduced to 0.1 mΩ, the phase margin is almost vanishing. In order to further find the effects of the output cable resistance, a Spice-based simulation was carried out via Simetrix/Simplis. Figure 10 shows the output current response of the step referent command disturbance in the 1 mΩ and 0.1 mΩ cases. Figure 9(a) depicts the output currents can subside back into equal current-sharing control in 1 mΩ cable resistance case; unfortunately, Figure 10(b) shows the unstable operation via 0.1 mΩ cable resistance. This conforms the previous comments that a large cable resistance can improve the system stability [19].

After the simulations have demonstrated the performance of the proposed integrated controller for voltage and droop current-sharing control, the paralleled DC/DC converter system with $N = 2$ was implemented. Furthermore, The PWM IC UC3525 was used to generate two-phase PWM pulses to control IDSC as shown in Figure 1(b). Figure 11(a) shows the measured primary currents and MOSFET drain to source voltage waveforms for referent. It shows the primary currents of the two forward converters are in balance operation. Owing to one output inductor scheme, two power trains of the IDSC have the same primary side current, which reflects from the secondary side inductor current as shown in Figure 11(b). Furthermore, the hot swap operation is also depicted in Figure 11(c), the parallel IDSCs can achieve equal sharing control. Figure 12 shows the loop gain profiles of the IDSC, which are similar to the simulation results. It shows the designed IDSC has at least 45° phase margin, 10 dB gain margin, and 10 KHz bandwidth; therefore, the effects of the parameter uncertainty can reduce significantly. Because the cable length of the prototype IDSC is 30 cm with

FIGURE 5: The parallel DC/DC converters system with $N = 2$ interconnected system: (a) detail control block diagram and (b) simplified diagram.

2 m Ω resistance as shown in Figure 13(a), the resulted interconnection system is stable. The physical size of the IDFS and interconnected system can let the cable length be shorted to 15 cm, and the resulted cable resistance is 1 m Ω as depicted in Figure 13(b). However, it is very difficult to obtain 0.1 m Ω cable resistance in this laboratory prototype interconnected system to demonstrate the unstable operation. Fortunately, from the theory study and simulation verification, the cable resistance will affect system stability.

5. Conclusions

An interconnected DC power system consists of DC/DC converters with primary droop current-sharing control was presented in this paper. Using the proposed droop controller will not affect the original design voltage loop gain profile but also can integrate into voltage controller and thus provides a low-cost solution. Furthermore, after a stable DC/DC converter design was achieved, the effect of the cable wire resistances of the interconnected system to stability was also

FIGURE 6: The frequency responses of the F_{di} and A_{ii} transfer functions at half load current operation: (a) magnitude; (b) phase.

FIGURE 7: The frequency responses of the transfer functions T_v , T_{dr} , $T_v + T_{dr}$, and ΔW at half load current operation: (a) magnitude and (b) phase.

investigated. The results demonstrated that the reduction of the cable resistance will decrease the phase margin of the interconnected system and lead to instability. Properly increasing the cable resistance can improve system stability, but the operating efficiency will reduce. This paper provides a method to evaluate the stability of the interconnected system. Using this method, the engineer can make a tradeoff between system stability and efficiency.

Appendix

(1) The Designed Parameters of the Interleaved Dual-Switch Forward Converter Are as Follows.

(i) Primary side DC bus voltage $V_i = 385$ V.

(ii) Primary switching frequency $f_s = 125$ kHz.

(iii) Nominal output voltage $V_o = 12$ V.

(iv) Nominal output current $I_o = 66$ A.

(v) Transformer PQ32/30 $N_p = 20$ turns, $N_s = 1$ turn, and $n = 20$.

(vi) Output inductor MS10675 with inductance $L = 2$ μ H.

(vii) Output capacitance $C = 5400$ μ F and esr = 4 m Ω .

(viii) Nominal duty ratio $D = 0.62$ in the secondary side of the IDSFC with an output inductor.

(ix) The gain of the PWM comparator $K = 0.25$.

FIGURE 8: The frequency responses of the opened- and closed-loop output impedances of the DC/DC converter at half load current operation: (a) magnitude and (b) phase.

FIGURE 9: The frequency responses of the parallel DC/DC converters system with output cable resistances $1 \text{ m}\Omega$ and $0.1 \mu\Omega$ at half load current operation: (a) magnitude and (b) phase.

FIGURE 10: The step reference command disturbance of the parallel DC/DC converters system with different output cable resistances at full-load current operation: (a) $1 \text{ m}\Omega$ and (b) $0.1 \mu\Omega$.

FIGURE 11: The key waveforms of the parallel DC/DC converters system at full-load current operation: (a) primary current and primary MOSFET drain to source voltage of the IDSFC; (b) the current and the input voltage of the output inductor; (c) hot swap operation.

FIGURE 12: The measured T_v and $T_v + T_{dr}$ frequency responses of the IDSFC at full-load current operation: (a) magnitude and (b) phase.

FIGURE 13: (a) The photograph of the IDSFC with 2 mΩ output cable resistance; (b) the back plane system with $N = 2$ and the corresponding connected output cables.

(2) The Key Transfer Functions of the IDFS

$$\begin{aligned}
 \frac{v_{oi}}{d_i} &= H_i(s) = \frac{V_g R_n (sCr_c + 1)}{\Delta}, \\
 \frac{i_{ii}}{d_i} &= F_{di}(s) = \frac{I_{oi} + (DV_g (SC(R_n + r_c) + 1)/\Delta)}{n}, \\
 \frac{i_{Li}}{d_i} &= F_{dLi}(s) = \frac{V_g (SC(R + r_c) + 1)}{\Delta}, \\
 \frac{i_{oi}}{d_i} &= F_{doi}(s) = \frac{V_g (SCr_c + 1)}{\Delta}, \\
 z_{oi} &= \frac{v_{oi}}{i_{oi}} = \frac{R_n (sCr_c + 1)(sL + r_L)}{\Delta}, \\
 A_{ii} &= \frac{i_{ii}}{i_{oi}} = \frac{DR_n (sCr_c + 1)}{\Delta},
 \end{aligned} \tag{A.1}$$

where

$$\begin{aligned}
 \Delta &= s^2 LC(R_n + r_c) + s(L + C(R_n r_L + R_n r_c + r_L r_c)) + R_n + r_L \\
 &\cong (R_n + r_L) \left(\left(\frac{s}{\omega_n} \right)^2 + 2\xi \frac{s}{\omega_n} + 1 \right), \quad R_n \gg r_L, r_c, \\
 \omega_n &= \frac{1}{\sqrt{LC}}, \\
 \xi &= \frac{Z + (R_n r_L + R_n r_c + r_L r_c)/Z}{2(R_n + r_L)}, \\
 Z &= \sqrt{\frac{L}{C}}.
 \end{aligned} \tag{A.2}$$

(3) *Design Procedure of the Steady-State Output Voltage Droop Characteristic.* In general, the output voltage droop characteristic of a DC/DC converter depends on output

voltage regulation specification with a predetermined design margin. If the maximum, nominal, and minimum output voltages of the regulation range are denoted as $V_{oi,max}$, V_{oi}^* , and $V_{oi,min}$, respectively. From Figure 1(b), the output voltage variation of the i th DC/DC converter with respect to droop current-sharing control is

$$V_{oi,max} = V_{oi}^* + \Delta V_{oi} = \frac{V_{refi}}{K_d}, \quad I_{oi} = 0, \tag{A.3}$$

where

$$V_{oi,min} = V_{oi}^* - \Delta V_{oi} = \frac{V_{refi}}{K_d} - V_{dr} \frac{K_{cs}}{K_d}, \tag{A.4}$$

$$K_d = \frac{R_1 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}, \quad K_{cs} = \frac{R_1 R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3}. \tag{A.5}$$

Furthermore, the droop voltage V_{dr} synthesizes from primary current through a low-pass filter, which is proportion to output current, that is, $I_{ii} = DI_{oi}/n$. From (A.3) and (A.4), the output voltage deviation ΔV_{oi} can be expressed in terms of droop voltage as

$$\Delta V_{oi} = V_{dr} \frac{K_{cs}}{2K_d} = \frac{k_d V_{dr}}{2}. \tag{A.6}$$

For a given output voltage deviation ΔV_{oi} , the design procedure of the output voltage droop characteristics is suggested as follows.

- (i) Let $R'_1 = kV_{refi}$ and $k > 0$.
- (ii) The resistance R_2 can subsequently be determined from the maximum output voltage listed in (A.3), K_d , and R'_1 .
- (iii) For a given specification of the output voltage deviation and droop voltage, the resistances R_1 and R_3 can be found from (A.6) and resistance R'_1 .

TABLE 1

R_1	R_2	R_3	R_4	R_5	R_6	C_1	C_2	C_3	C_4
2.57 k Ω	10 k Ω	100 k Ω	1 k Ω	33 k Ω	10 k Ω	4700 pF	6800 pF	680 pF	220 pF $\times 2$

TABLE 2

R_{f1}	R_{f2}	C_{f1}	C_{f2}	k_f
1 k Ω	100 Ω	0.1 μ F	0.01 μ F	2.4

(4) *Voltage and Primary Droop Current-Sharing Controller.* The feedback controllers in Figure 1(b) are

$$G_{c1}(s) = \frac{(s/\omega_{z1} + 1)}{\alpha_2 s(s/\omega_{p1} + 1)}, \quad G_{c2}(s) = \frac{(s/\omega_{z2} + 1)}{K_2(s/\omega_{p2} + 1)}, \quad (\text{A.7})$$

where

$$\begin{aligned} \omega_{p1} &= \frac{1}{C_{23}R_5}, \quad \omega_{p2} = \frac{1}{C_1R_4}, \\ \omega_{z1} &= \frac{1}{C_2R_5}, \quad \omega_{z2} = \frac{1}{C_1(R_2 + R_4)}, \\ \alpha_2 &= C_2 + C_3, \quad C_{23} = \frac{C_2C_3}{C_2 + C_3}, \\ K_2 &= R_2, \quad \omega_{o1} = \frac{1}{K_2\alpha_2}. \end{aligned} \quad (\text{A.8})$$

(i) The design poles and zeros of the controller $G_{c1}(s)$, $G_{c2}(s)$, and $G_{dr}(s)$ can let the DC/DC converter have at least 45° phase margin, 10 dB gain margin, and 10 KHz bandwidth

$$\begin{aligned} \omega_0 &= 66845 \text{ rad/sec}, \quad \omega_{p1} = 49019.6 \text{ rad/sec}, \\ \omega_{p2} &= 212765.95 \text{ rad/sec}, \quad \omega_{z1} = 4456.33 \text{ rad/sec}, \\ \omega_{z2} &= 20263.24 \text{ rad/sec}. \end{aligned} \quad (\text{A.9})$$

(ii) Circuit parameters of the controller $G_{c1}(s)$, $G_{c2}(s)$, and $G_{dr}(s)$; (see Table 1).

Note. (1) Using the nearest commercial parts instead of the estimated parameters.

(5) *Low-Pass Filter* $G_f(s)$

$$\begin{aligned} G_f(s) &= \frac{k_f}{s^2 R_{f1} R_{f2} C_{f1} C_{f2} + s(R_{f1}(C_{f1} + C_{f2}) + R_{f2} C_{f2}) + 1}. \end{aligned} \quad (\text{A.10})$$

(see Table 2).

Acknowledgment

The authors thank the National Science Council of Taiwan for supporting the research project: NSC99-2221-E231-036.

References

- [1] V. Vorpérian, "Synthesis of medium voltage dc-to-dc converters from low-voltage, high-frequency PWM switching converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1619–1635, 2007.
- [2] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular dc-dc converters using dynamic input-voltage reference scheme," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1462–1473, 2004.
- [3] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," *IEEE Transactions on Industry Applications*, vol. 42, no. 4, pp. 1101–1111, 2006.
- [4] W. U. Chen, X. Ruan, H. Yan, and C. K. Tse, "DC/DC conversion systems consisting of multiple converter modules: stability, control, and experimental verifications," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1463–1474, 2009.
- [5] S. Luo, Z. Ye, R. L. Lin, and F. C. Lee, "Classification and evaluation of paralleling methods for power supply modules," in *Proceedings of the 30th Annual IEEE Power Electronics Specialists Conference (PESC '99)*, vol. 2, pp. 901–908, July 1999.
- [6] D. S. Garabandic and T. B. Petrovic, "Modeling parallel operating PWM DC/DC power supplies," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 5, pp. 545–551, 1995.
- [7] V. J. Thottuvellil and G. C. Verghese, "Analysis and control design of paralleled DC/DC converters with current sharing," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 635–644, 1998.
- [8] J. Rajagopalan, K. Xing, Y. Guo, F. C. Lee, and Manners, "Modeling and dynamic analysis of paralleled dc/dc converters with master-slave current sharing control," in *Proceedings of the 11th IEEE Applied Power Electronics Conference and Exposition (APEC '96)*, vol. 2, pp. 678–684, 1996.
- [9] Y. Panov, J. Rajagopalan, and F. C. Lee, "Analysis and design of N paralleled DC-DC converters with master-slave current-sharing control," in *Proceedings of the 12th IEEE Applied Power Electronics Conference and Exposition (APEC '97)*, vol. 1, pp. 436–442, 1997.
- [10] Y. Huang and C. K. Tse, "Circuit theoretic classification of parallel connected dc-dc converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1099–1108, 2007.
- [11] Y. Panov and M. M. Jovanović, "Loop gain measurement of paralleled dc-dc converters with average-current-sharing control," in *Proceedings of the 23rd Annual IEEE Applied Power Electronics Conference and Exposition (APEC '08)*, pp. 1048–1053, February 2008.

- [12] I. Batarseh, K. Siri, and H. Lee, "Investigation of the output droop characteristics of parallel-connected DC-DC converters," in *Proceedings of the 25th Annual IEEE Power Electronics Specialists Conference (PESC '94)*, vol. 2, pp. 1342–1351, June 1994.
- [13] J. Perkinson, "Current sharing of redundant DC-DC converters in high availability systems—a simple approach," in *Proceedings of the IEEE 10th Annual Applied Power Electronics Conference (APEC '95)*, vol. 2, pp. 952–956, March 1995.
- [14] Brian T. Irving and Milan M. Jovanovic, "Analysis, design, and performance evaluation of droop current-sharing method," in *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC '00)*, vol. 1, pp. 235–241, 2000.
- [15] J. W. Kim, H. S. Choi, and B. O. H. Cho, "A novel droop method for converter parallel operation," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 25–32, 2002.
- [16] X. Zhou, P. Xu, and F. C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1153–1162, 2000.
- [17] J. A. Abu Qahouq, L. Huang, and D. Huard, "Sensorless current sharing analysis and scheme for multiphase converters," in *Proceedings of the IEEE 38th Annual Power Electronics Specialists Conference (PESC '07)*, pp. 2029–2036, June 2007.
- [18] H. Mao, L. Yao, C. Wang, and I. Batarseh, "Analysis of inductor current sharing in nonisolated and isolated multiphase DC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3379–3388, 2007.
- [19] T. F. Wu, K. Siri, and J. Banda, "Central-limit control and impact of cable resistance in current distribution for parallel-connected DC-DC converters," in *Proceedings of the 25th Annual IEEE Power Electronics Specialists Conference (PESC '94)*, vol. 1, pp. 694–702, June 1994.
- [20] J. Lunze, *Feedback Control of Large-Scale Systems*, Prentice Hall, New York, NY, USA, 1992.
- [21] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Kluwer Academic, Boston, Mass, USA, 2nd edition, 2001.
- [22] M. Brown, *Power Supply Cookbook*, Butterworth-Heineman, Oxford, UK, 1994.