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Research Article

Fully Programmable Gaussian Function Generator Using Floating Gate MOS Transistor

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Floating gate MOS (FGMOS) based fully programmable Gaussian function generator is presented. The circuit combines the tunable property of FGMOS transistor, exponential characteristics of MOS transistor in weak inversion, and its square law characteristic in strong inversion region to implement the function. Two-quadrant current mode squarer is the core subcircuit of Gaussian function generator that helps to implement full Gaussian function for positive as well as negative input current. FGMOS implementation of the circuit reduces the current mismatching error and increases the tunability of the circuit. The performance of circuit is verified at 1.8 V in TSMC 0.18 μm CMOS, BSIM3, and Level 49 technology by using Cadence Spectre simulator.

1. Introduction

Gaussian function is one of the most widely used functions in many domains such as neural network, neural algorithm, and on-chip diffusion profile. Diffusion is one of the important steps in the chip fabrication. The diffusion profile of impurity atoms is dependent on the initial and boundary conditions. When a constant amount of dopant is deposited on the surface, the doping profile is approximated by Gaussian function [1]. Another application of Gaussian function is observed in multidimensional problems like pattern matching and data classifications [2]. These cases are calculated using probability density functions and these functions can be modeled by normal distributions [3].

Madrinas et al. proposed a CMOS analog integrated circuit to implement Gaussian function [4]. They have successfully designed a five-transistor circuit in which current mirror is in weak inversion region and voltage variable resistors are replaced by two MOS transistors. But the conventional circuit has limitations of mismatching of MOS transistors and it can implement only half of the Gaussian function. The circuit proposed in [5] overcomes the limitations of the circuit proposed in [4] by using FGMOS transistors.

Recently the work published in [6] implements the Gaussian functions using fourth-order approximation. The accuracy and complexity of this circuit depends upon order of approximation of the Gaussian function. So, there is always a tradeoff between circuit complexity and its accuracy.

This paper presents very simple FGMOS based fully programmable Gaussian function generator that uses a single two-quadrant current mode squarer/divider to generate fully programmable Gaussian function.

FGMOS has many attractive features for example it reduces the complexity of circuits and can simplify the signal processing chain of a design. It can shift the signal levels and incorporate tunable mechanisms. It can even work normally below the operational limits of supply voltage levels for a particular technology and thus consume less power than the minimum power required for a MOS circuit of same technology without affecting the performance of the device [7].

The paper is organized as follows. Basics of FGMOS transistor is given in Section 2. A fully programmable Gaussian function generator is introduced and analyzed in Section 3. Next section details the simulation results. Finally on the basis of simulation results, conclusions are drawn in the last section.

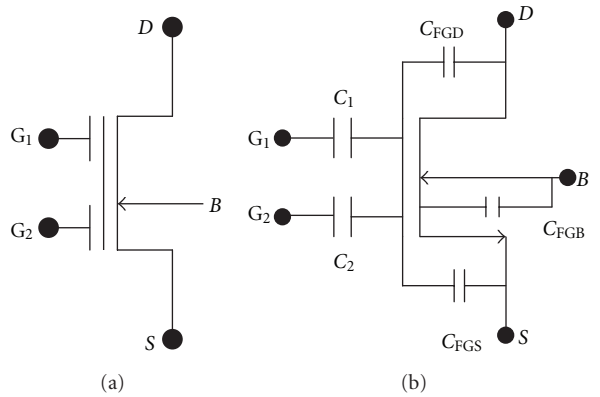

Figure 1: (a) Symbol of two-input floating gate and (b) its equivalent circuit [7].

2. Basics of FGMOS Transistor

FGMOS is a multiple-input floating gate transistor whose threshold voltage can be controlled and tuned by the values of capacitors and bias voltage applied.

The symbolic representation of two-input FGMOS transistor and its equivalent circuit are shown in Figure 1. The input signal (V_1) and bias voltage (V_b) are applied at gates G_1 and G_2 of FGMOS transistor, respectively.

The voltage on floating gate V_{FG} is given as [7–10]

$$V_{FG} = \frac{(Q_{FG} + C_{FGD}V_D + C_{FGS}V_{ss} + C_{FGB}V_B + C_1V_1 + C_2V_b)}{C_T}, \quad (1)$$

where C_1 and C_2 are the capacitances associated with G_1 and G_2, $C_T = C_1 + C_2 + C_{FGS} + C_{FGD} + C_{FGB}$, is the total floating gate (FG) capacitance. C_{FGD}, C_{FGS}, and C_{FGB} are the overlap capacitances of floating gate with drain, source, and bulk respectively, V_D is the drain voltage, V_{ss} is the source voltage, V_B is the bulk voltage, and Q_{FG} is the residual charge.

Since the floating gate of FGMOS does not have any connection to ground, so to avoid dc convergence error during simulation the model suggested by Yin et al. [11] has been used. The model is based on connecting resistors in parallel with the input capacitors as shown in Figure 2, where, $R_i = 1/kC_i = 1000\,\text{G}\Omega$.

The drain current (I_D) of the FGMOS transistor operating in ohmic region (source grounded) is given by [7]

$$I_D = \beta\left[\left\{\left(\frac{C_1}{C_T}V_1 + \frac{C_2}{C_T}V_2 + \frac{C_{FGD}}{C_T}V_D\right) - V_T\right\} - \frac{V_D}{2}\right]V_D, \quad (2)$$

where β is the transconductance parameter, C_1 and C_2 are the capacitances associated with G_1 and G_2, respectively, C_T is the total floatinggate (FG) capacitance, and V_T stands for the threshold voltage. Above equation can be simplified as

$$I_D = \beta\left(\frac{C_1}{C_T}\right)\left[(V_1 - V_{T,\text{eff}})V_D - \frac{C_T}{2C_1}V_D^2\right], \quad (3)$$

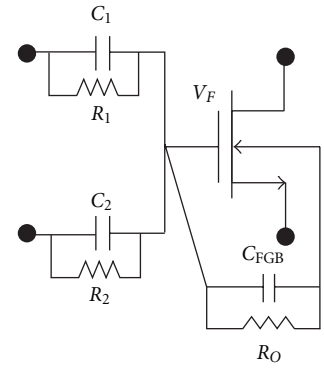

Figure 2: Simulation model for FGMOS [11].

where effective threshold voltage ($V_{T,\text{eff}}$) is given by

$$V_{T,\text{eff}} = V_T + \frac{C_2}{C_1}(V_T - V_b). \quad (4)$$

From (3), it is obvious that the reduction in $V_{T,\text{eff}}$ can be done by selecting $V_b > V_T$ and $C_2 > C_1$.

Hence, $V_{T,\text{eff}}$ is controllable and it is depending on the values of C_1 and C_2. The proposed Gaussian circuit utilizes this property of FGMOS transistor.

3. Proposed Gaussian Function Generator

If x is the input variable and y is the output, then the Gaussian function is defined by

$$y = Ae^{-x^2/2\sigma^2}, \quad (5)$$

where A, σ are the adjustable constants which define the amplitude and width of Gaussian function. In the proposed work the Gaussian function is constructed by first squaring the input variable x that is current by using the square law characteristic of MOS, secondly exponential characteristic of MOS in weak inversion is used to complete the transfer function as given in (5).

Current mode squarer/divider used for full Gaussian function generation is shown in Figure 3 [12]. The operation of the circuit will be based on square law characteristics if all the MOS transistors are biased in strong inversion region. The transistors M1 through M3 form the squarer part of the circuit. The drain currents I_{D1} and I_{D2} of M1 and M2 can be, respectively, given as [12]

$$I_{D1} = \frac{(4I_B - I_{\text{in}})^2}{16I_B} \quad \text{for } |I_{\text{in}}| \le 4I_b, \quad (6)$$

$$I_{D2} = \frac{(4I_B - I_{\text{in}})^2}{16I_B} \quad \text{for } |I_{\text{in}}| \le 4I_b. \quad (7)$$

The total current I_{out} is given by

$$I_{\text{out}} = \frac{I_{\text{in}}^2}{8I_B} + 2I_B. \quad (8)$$

From above equation, it can be seen that the output current consists of the squared input current I_{in} and dc current

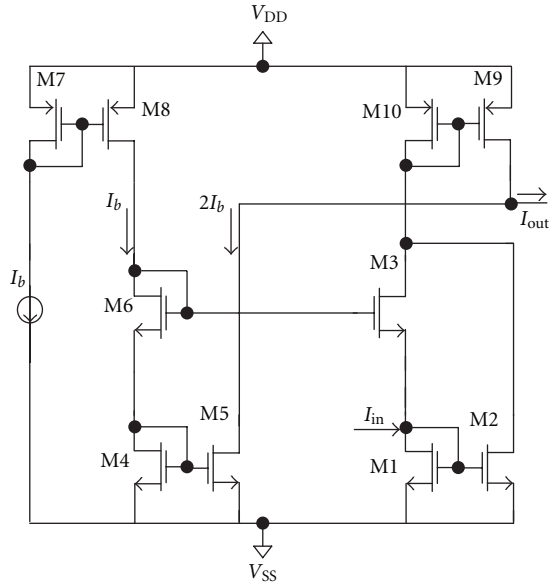

Figure 3: Two-quadrant current mode squarer/divider [12].

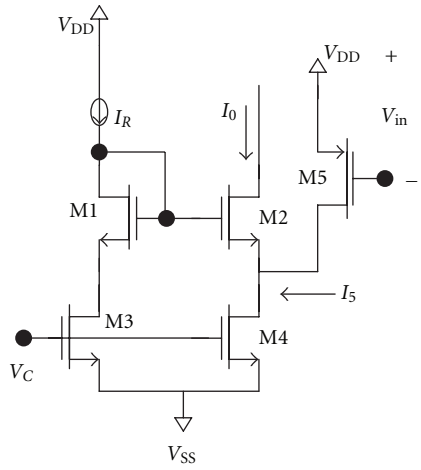

Figure 4: Conventional Gaussian circuit [4].

$2I_B$ Thus if the dc current $2I_B$ is compensated, a perfect squarer/divider circuit is obtained which can be used to realize many current mode analog processing circuits.

The operating principle of conventional Gaussian circuit, proposed by Madrinas et al. is described in [4]. The MOSFETs M3 and M4 of the conventional circuit, shown in Figure 4, are working in linear region and behave as variable resistors.

In the proposed circuit, shown in Figure 5, the MOS transistors M3 and M4 working in linear region are replaced by FGMOS transistors to increase tuning ability of the circuit and reduce mismatching error between transistor pair M3-M4. PMOS transistor M5 of the conventional (Figure 4) circuit is replaced by current squarer/divider to implement fully programmable Gaussian function.

Figure 5 is the circuit implementation of FGMOS based Gaussian circuit.

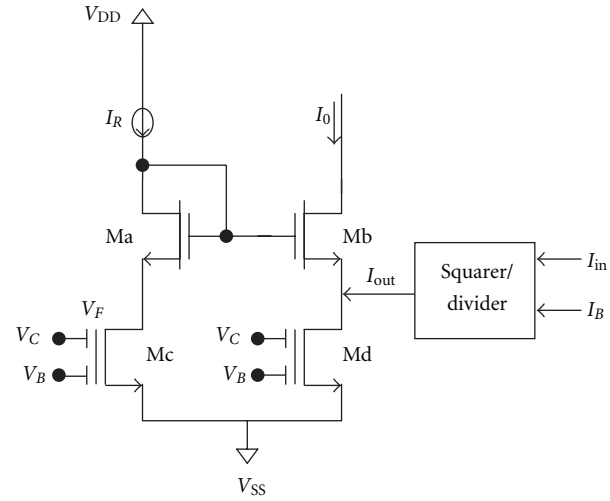

Figure 5: The proposed FGMOS based Gaussian circuit.

In the circuit V_C and V_B are the gate and bias voltages, respectively. The FGMOS transistors Mc and Md are working in their linear region. On neglecting C_{FGD}, the drain current can be expressed by (if source is grounded)

$$I_D = \beta \cdot V_D\left[V_F - V_T - \frac{V_D}{2}\right], \tag{9}$$

where

$$V_F = \frac{C_1}{C_T}V_C + \frac{C_2}{C_T}V_B. \tag{10}$$

The control voltage V_F controls the output conductances of Mc and Md, whose value is approximately given by

$$g_{dsc,d} \cong \beta_{c,d}(V_F - V_{Tc,d}). \tag{11}$$

The condition for the linear operation is

$$(V_F - V_T) \gg V_{Dc,d}. \tag{12}$$

The effect of V_F on output current and the Gaussian function is given by [4]

$$I_0 = I_R e^{-I_{out}/v_T g_{dsd}}, \tag{13}$$

where I_R is dc bias current of current mirror, v_T is volt-thermal equivalent, and I_{out} is the output current of squarer/divider. On comparing (13) and (5) it can be seen that the width of Gaussian function can be controlled by varying the floating gate voltage V_F. Since, V_F depends upon both V_C and V_B, the width becomes more programmable. The performance of the Gaussian circuit depends upon the symmetry of the current mirror used. If there is mismatch between MOS Ma-Mb, their source voltages will be different and output current I_O will not be equal to reference current I_R, that is,

$$\Delta V_S = \frac{I_R}{g_{dsc}} - \frac{I_O}{g_{dsd}}. \tag{14}$$

The difference source voltage can be zero if $g_{dsc} = g_{dsd}$. In the proposed circuit the tuning capability of FGMOS transistor helps to make gds3 and gds4 to be equal. Full implementation of the proposed circuit is shown in Figure 6.

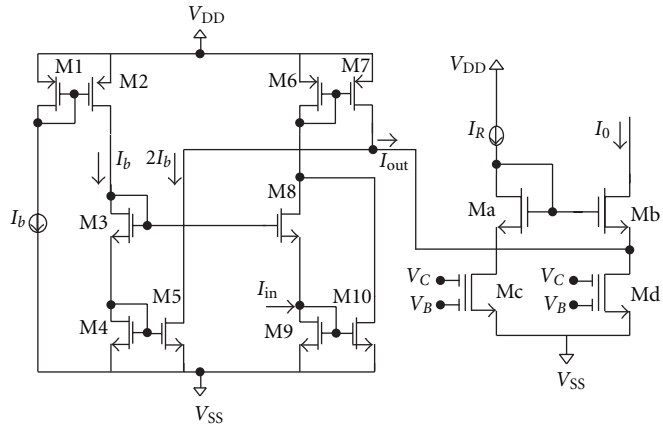

Figure 6: Proposed FGMOS based Gaussian circuit (complete).

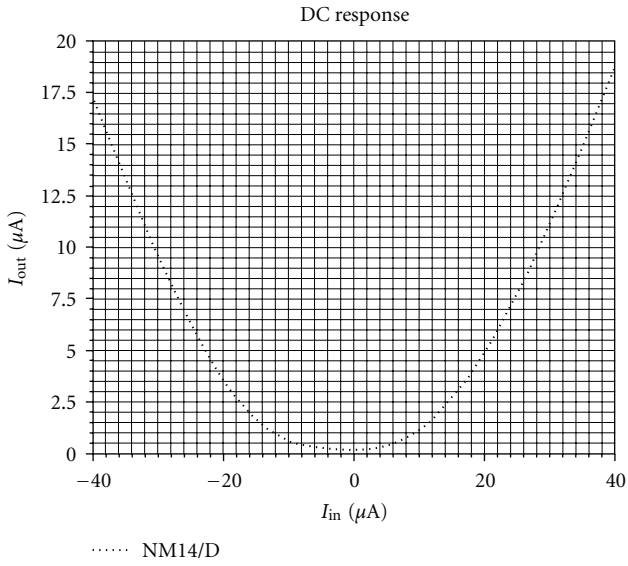

Figure 7: Output current of squarer/divider.

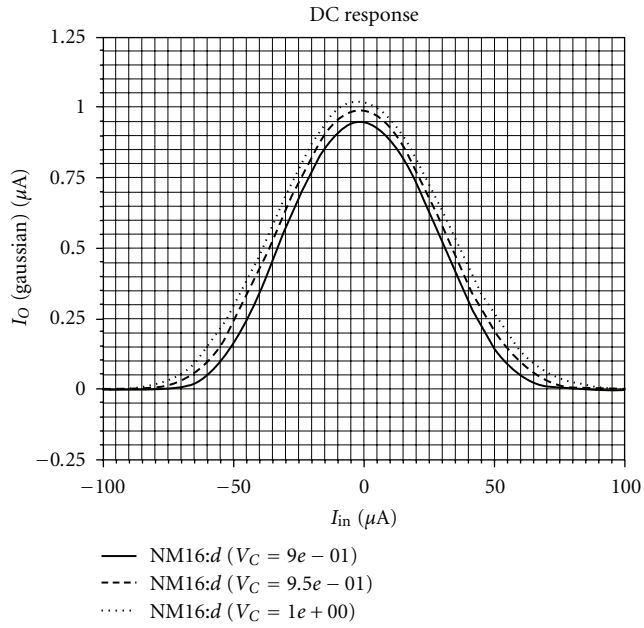

Figure 8: Variation of output current with respect to I_{in} at different value of control voltage V_C.

4. Simulation Results

The designed circuits are simulated using Cadence Spectre simulator in TSMC 0.18 um CMOS technology using 1.8 V power supply.

Simulation result for squarer/divider is shown in Figure 7. The bias current (I_B) for squarer/divider is 10 μA and the input current (I_{in}) varies from $-40\,\mu$A to 40 μA.

Figure 8 shows the variation of output current (I_O) with respect to input (I_{in}) and control voltage V_C varying from 0.9 V to 1 V. It can be noticed from output waveforms (Figure 8) that width of the Gaussian function can be controlled by varying the control voltage V_C. Figure 9 shows the power dissipated by the circuit at different values of input current I_{in}. It can be seen that the circuit has power dissipation of 0.1 mW at the input current of 10 μA. Table 1 summarizes the aspect ratio of the MOS used in the proposed circuit. Table 2 shows the output current relative error defined as

$$E_r = \frac{(I_O - I_R)}{I_R} \times 100\% \quad (15)$$

Table 1: Aspect ratio of transistors of Figure 6.

Transistor	$W(\mu m)$	$L(\mu m)$
M1–M3, M4, M6	0.54	0.18
M5	3.6	0.18
M7–M10	1.44	0.18
Ma–Md	0.4	0.18

for different values of control voltage V_C. It can be seen that percentage error is zero for $V_C = 0.95$ V.

Table 3 gives the performance parameters of the proposed circuit. It can be seen that circuit has the total noise of 1.6441e−14 V^2/Hz at the frequency of 100 kHz. The complexity of the circuit is also low as compared to other circuits implementing full Gaussian function.

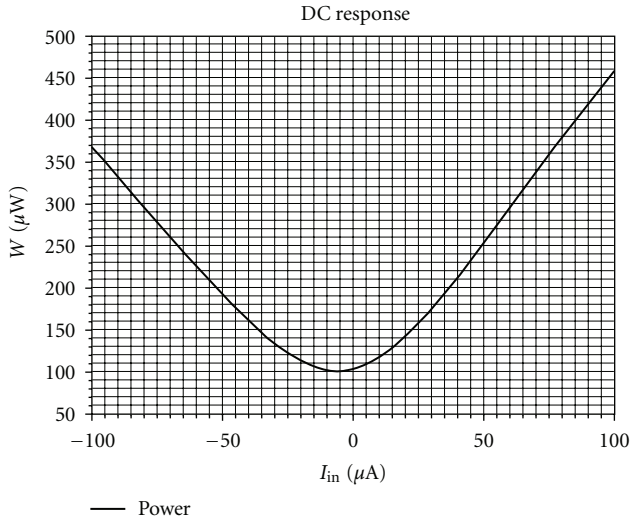

Figure 9: Variation of output power with respect to input current.

Table 2: Output current relative error for different values of V_C at $I_R = 1\,\mu$A.

I_R (μA)			1	
V_C (V)	0.85	0.9	0.95	1
E_r (%)	−3	−1	0	2

Table 3: Performance parameters of the proposed circuit.

Parameters	Simulated results
Supply voltage (V)	1.8
Input current (I_{in}) range (μA)	−100 to 100
Power dissipated (mW) (at $I_{in} = 10\,\mu$A)	0.1
Total noise (V^2/Hz)	$1.6441e-14$
No. of transistor	14

5. Conclusion

In this paper FGMOS based fully programmable Gaussian circuit has been proposed which utilizes the advantages of FGMOS transistor for better tuning ability and low mismatching error between the MOS pair. The proposed circuit uses two-quadrant square/divider to implement full Gaussian function. Complexity and power dissipation of the circuit are very low. Thus the newly developed Gaussian circuit is the best choice for highly accurate and low power applications of Gaussian function.

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