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Research Article

Controller Design Considerations for ACM APFC Systems

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This paper is concerned with performance of the current shaping network in Average Current Mode (ACM) Active Power Factor Correction (APFC) systems. Theoretical expressions for the ripple components are derived. Then, ripple interaction and impact on the current loop reference signal are investigated. A modification of the controller network is suggested that results in an improved Total Harmonic Distortion (THD). Design guidelines are suggested. The theoretical predictions were validated by simulation.

1. Introduction

Over the past few years, a variety of current shaping methodologies were developed for Active Power Factor Correction (APFC) [1–3]. Each approach undertaken is a compromise in between the performance indexes and the circuit complexity and cost. The Critical Conduction Mode (CrCM) APFC operating on the CCM-DCM boundary [4–7] shapes the average input current by comparator/zero detector and is unconditionally stable. However, the natural simplicity, robustness, and stability of CrCM APFC are offset by high ripple current which cause increased conduction and core losses. Difficulties in filtering the variable frequency current ripple and poor efficiency restrict this technique to low-power and low-cost applications. Other Discontinuous Conduction Mode (DCM) based designs, which upside is simplicity suffer from similar problems exhibiting also higher harmonic distortion of the line current [8, 9].

APFC without line voltage sensing, [10–13] stands out as a robust, technologically simple, and cost-effective solution. A simple and clear physical insight into the principle of operation of the current loop of this class of APFCs was suggested in [14]. All of the mentioned above APFCs with no input voltage sensing make use of a hidden current loop inside a DC-DC converter. The designs mainly differ in their method of realization of the transresistive feedback, PWM, and supplementary current loop control circuitry. Regardless of the implementation, however, the duty cycle programming is implemented according to the converters input port ideal average relationships and ideal modulator ramp signal. As a result, accurate current loop operation can only be attained in the Continuous Conduction Mode (CCM) under negligible current ripple conditions. In practice, however, the CCM-DCM mode changes, current ripple, and ramp carrier imperfections cause the duty cycle to deviate from the ideal relationship resulting in distortion in the average input current.

The very proper average current mode three-loop APFC [15–18] achieves its control objectives by a control scheme shown at Figure 1. The three-loop APFC uses a slow outer voltage loop to control the output voltage and a fast current loop for active shaping of the average input current. The reference signal for the inner current loop is derived from the rectified power line voltage by the multiplier-squarer-divider circuit. Additional outer feed-forward loop compensates for the line voltage variations. Such an APFC could be designed to operate in CCM most of the cycle but could tolerate also DCM intervals sustaining good current tracking.

The two feedback loops of the APFC of Figure 1 have conflicting objectives. In particular, a strong outer loop that manages to stabilize the output voltage will deteriorate the power factor by dictating an input current that ensures a fixed output voltage rather than the desired sinusoidal-shaped current. The outer loop is usually designed with

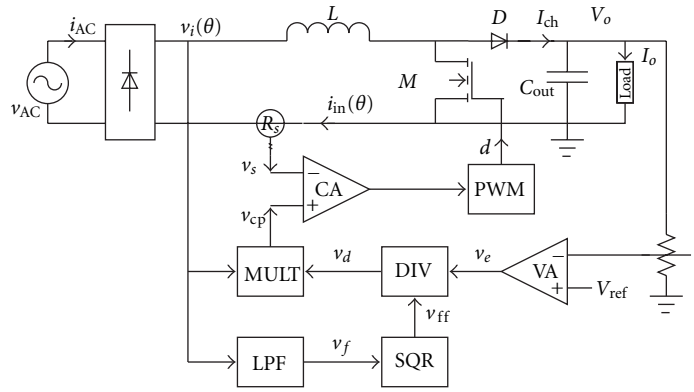

Figure 1: Three-loop ACM APFC system block diagram.

a limited bandwidth as well as with a low gain so to heavily attenuate the output ripple. Otherwise, the ripple will distort the input current by penetrating into the reference of the current loop. As a result the response of the outer loop to load variations is rather slow. The outer loop error amplifier output voltage contains a second harmonic ripple component which modulates the current amplitude and thus distorts the current reference signal. Obviously, this also results in distorted line current.

This paper suggests that one of the causes of the major current distortion in most, if not all, APFC systems is the second harmonic ripple components that are brought into the current reference by the outer loops. The proposed solution to the problem can be found by compensating the output ripple rather than filtering. This alternative was investigated in this study analytically and by simulation. It was found that such a strategy is possible and furthermore it can easily be implemented by simple additional circuitry to commercially available APFC controllers. This paper presents the theory of the proposed approach and demonstrates the improvement in Total Harmonic Distortion (THD) that can be gained and provides design guidelines.

2. Basic Assumptions and Strategy

The analyses to follow are carried under the following assumptions:

(a) the line voltage is a pure sinusoidal wave;

(b) the rectifiers are ideal;

(c) the power stage is linear and 100% efficient;

(d) the current loop is ideal, that is, it forces the input current to follow the reference signal;

(e) the holdup capacitor is large and hence the output ripple is small as compared to the dc output voltage.

The following approach is adopted: initially it is assumed that the input current is a pure sine wave. Next, the outer loop ripple components propagation mechanism into the current reference circuit is investigated. The assumption of the ideal current loop helps identify the current reference distortion components, which originate in the outer loops. Based on the results, the requirements for maintaining a distortion-free current reference are formulated. Finally, under the assumption of the ideal current loop, the residual distortion caused by the proposed ripple cancellation scheme is examined.

3. General Considerations: Review of APFC Output Current and Voltage

Under the assumptions above, the line voltage and current of the APFC of Figure 1 are in phase and of a sinusoidal shape. To simplify the notation the analyses are confined to one-half of the line period for which the rectified inputs can be expressed as

$$\begin{aligned} v_{in}(\theta) &= V_m \sin\theta, \\ i_{in}(\theta) &= I_m \sin\theta, \end{aligned} \tag{1}$$

where $\theta = \omega t$ is the power line angle ($0 \le \theta \le \pi$). The instantaneous input power of the APFC is given by

$$p_{in}(\theta) = v_{in}(\theta) i_{in}(\theta) = V_m I_m \sin^2\theta = P_{av}(1 - \cos 2\theta), \tag{2}$$

where $P_{av} = (1/2)V_m I_m$ is the average power over the power line cycle. The instantaneous charging power at the output of the APFC is a function of the output voltage, $v_{out}(\theta)$, and the output charging current, $i_{ch}(\theta)$:

$$p_{out}(\theta) = v_{out}(\theta) i_{ch}(\theta) \approx V_{DC} i_{ch}(\theta). \tag{3}$$

Here, the output ripple is neglected, that is, the output voltage, $v_{out}(\theta)$, of the APFC is assumed to be equal to its average value, V_{DC}. For an ideal power stage with 100% efficiency, instantaneous input and output power are equal:

$$p_{in}(\theta) = p_{out}(\theta). \tag{4}$$

Applying (2)–(4), the charging current, $i_{ch}(\theta)$, is approximated to

$$i_{ch}(\theta) = \frac{P_{av}}{V_{DC}}(1 - \cos 2\theta). \tag{5}$$

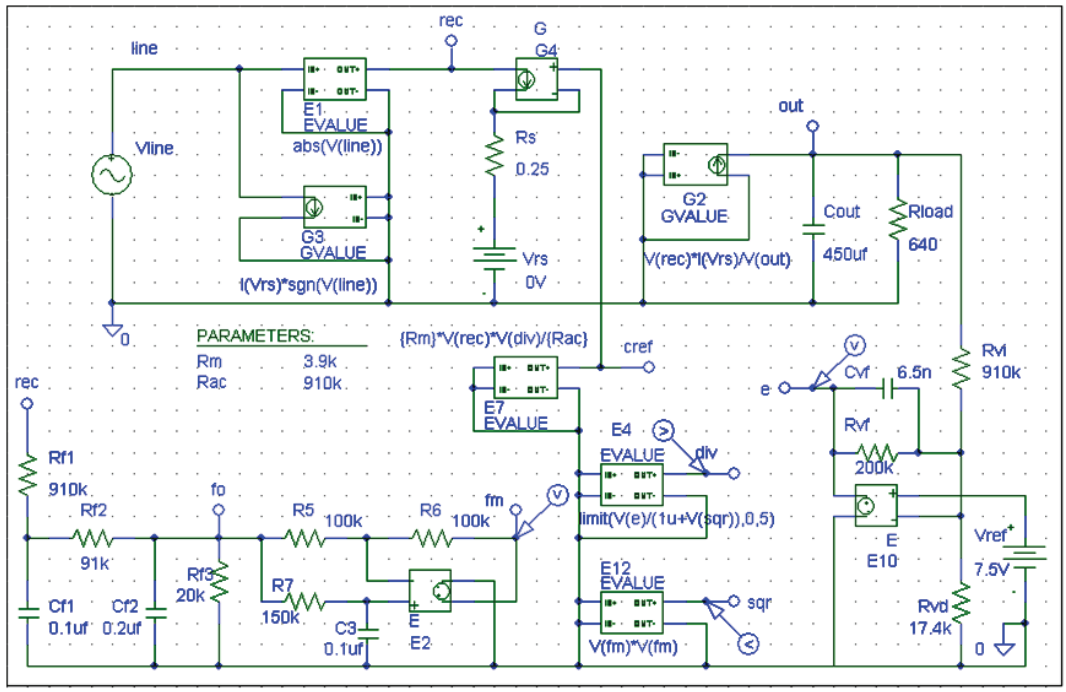

Figure 2: Simulation diagram of the modified three-loop APFC based on the behavioral model.

The holding capacitor current, $i_c(\theta)$, is the difference between the charging current and the DC load currents:

$$i_c(\theta) = i_{\text{ch}}(\theta) - I_{\text{DC}} = -\frac{P_{\text{av}}}{V_{\text{DC}}}\cos 2\theta. \tag{6}$$

The AC current of the holdup capacitor, $i_c(\theta)$, generates a second harmonics ripple component, $v_{o2}(\theta)$, which appears at the output:

$$v_{o2}(\theta) = \frac{1}{\omega C}\int i_c(\theta)d\theta = \frac{-P_{\text{av}}}{2\omega C V_{\text{DC}}}\sin 2\theta. \tag{7}$$

Clearly, the output ripple is a linear function of power. The instantaneous output voltage including the second harmonic ripple can now be written as

$$v_{\text{out}}(\theta) = V_{\text{DC}} + v_{o2}(\theta). \tag{8}$$

Using (7) yields

$$v_{\text{out}}(\theta) = V_{\text{DC}}\left(1 - \frac{P_{\text{av}}}{2\omega C V_{\text{DC}}^2}\sin 2\theta\right). \tag{9}$$

The second harmonic frequency peak-to-peak ripple, γ, is derived from the above to be

$$\gamma = \frac{\Delta V_{\text{out}_{\text{pp}}}}{V_{\text{DC}}}100\% = \frac{P_{\text{av}}}{\omega C V_{\text{DC}}^2}100\%. \tag{10}$$

4. The Feed-Forward Path Signal

The rectified input voltage fed to the feed-forward path filter (LPF) of the PFC topology under study, see Figure 1, can be represented by the Fourier series:

$$v_{\text{in}}(\theta) = V_{i0} + V_{i2}\cos 2\theta + V_{i4}\cos 4\theta + \cdots, \tag{11}$$

where $V_{i0} = (2/\pi)V_m$, $V_{i2} = -(4/3\pi)V_m$, $V_{i4} = -(4/15\pi)V_m$, and so forth are the Fourier coefficients. The relative phases of the harmonics are zero. When this signal is fed to the LPF feed-forward network of Figure 2, the LPF output voltage, $v_f(\theta)$, appears as

$$\begin{aligned} v_f(\theta) = {} & V_{i0}H_{f0} + V_{i2}H_{f2}\cos\left(2\theta + \phi_{f2}\right) \\ & + V_{i4}H_{f4}\cos\left(4\theta + \phi_{f4}\right) + \cdots, \end{aligned} \tag{12}$$

where H_{fn} and ϕ_{fn} are the gain and phase of the LPF transfer function at the nth harmonic of the line frequency. Since the amplitude of the harmonics of the rectified voltage decreases with their frequency and since the LPF provides sufficient attenuation at high frequencies, harmonic components higher than the second one may be neglected at the output of the LPF. Therefore, the response of the LPF is approximated to

$$v_f(\theta) = V_{i0}H_{f0}\left(1 + \frac{V_{i2}}{V_{i0}}\frac{H_{f2}}{H_{f0}}\cos\left(2\theta + \phi_{f2}\right)\right). \tag{13}$$

The $v_f(\theta)$ signal is squared with the gain of k_s by the squarer circuit, see Figure 1. Applying the same reasoning as above the resulting quadratic term could be neglected. Therefore, the approximated feed-forward signal is

$$\begin{aligned} & v_{ff}(\theta) \\ & = k_s v_f^2(\theta) \approx k_s V_{i0}^2 H_{f0}^2\left(1 + 2\frac{V_{i2}}{V_{i0}}\frac{H_{f2}}{H_{f0}}\cos\left(2\theta + \phi_{f2}\right)\right). \end{aligned} \tag{14}$$

Substituting the values of the Fourier coefficients, the expression for the feed-forward signal fed to the divider is obtained as

$$v_{ff}(\theta) = V_{ff0} v_{ffn}(\theta), \tag{15}$$

where the term, $V_{ff0} = k_s(4/\pi^2)V_m^2 H_{f0}^2$ and $v_{ffn}(\theta)$ is the normalized feed-forward voltage:

$$v_{ffn}(\theta) = \frac{v_{ff}(\theta)}{V_{ff0}} = 1 - \frac{4}{3}\frac{H_{f2}}{H_{f0}}\cos\left(2\theta + \phi_{f2}\right). \tag{16}$$

Equation (15) describes a waveform having a DC value proportional to the square of the amplitude of the input voltage, V_m^2, scaled by the DC gain of the feed-forward path: $k_s(4/\pi^2)H_{f0}^2$. The normalized feed-forward signal (16) contains an undesirable second harmonic component propagating into the current reference. Interesting to note is that the normalized ripple (16) at the output of the LPF is constant and depends on the attenuation at the second harmonic frequency, $(4/3)(H_{f2}/H_{f0})$. The amount of attenuation is determined by LPF configuration and its comer frequency. Lowering the corner frequency increases the attenuation, lowering also the harmonic contents of the feed-forward signal. This results in better line current quality. However, lowering the corner frequency slows the APFC response to line variations.

5. The Voltage Feedback Path Signal

To establish the operating point of the voltage error amplifier the issue of the input current generation should be addressed first. The input current of the PFC circuit of Figure 1 is generated by the following algorithm:

$$i_{\text{in}}(\theta) = I_m \sin\theta = K(v_e(\theta))\left(\frac{1}{V_m^2}\right)(V_m \sin\theta). \tag{17}$$

where, $v_e(\theta)$ is the voltage feedback error amplifier signal and K is the system's gain constant. Thus the amplitude of the input current and the average input power are

$$I_m = K\left(\frac{v_e(\theta)}{V_m}\right), \tag{18}$$

$$P_{\text{av}} = \frac{I_m V_m}{2} = \frac{K}{2} v_e(\theta). \tag{19}$$

The advantage of the feed-forward path is apparent; the APFC power level (19) is independent of the line voltage.

The steady-state output voltage of the error amplifier, $v_e(\theta)$, contains the DC term, V_{e0}, as well as the second harmonics ripple component, $v_{e2}(\theta)$:

$$v_e(\theta) = V_{e0} + v_{e2}(\theta). \tag{20}$$

The steady state DC error amplifier voltage, V_{e0}, required to maintain the average power level, P_{av}, could be derived from (19) neglecting the ripple component as

$$V_{e0} = \frac{2}{K} P_{\text{av}}. \tag{21}$$

The second harmonic component, $v_{e2}(\theta)$, appears as the response of the error amplifier to the output voltage ripple, $v_{o2}(\theta)$, given by (7)

$$v_{e2}(\theta) = -\frac{H_{v2}}{2\omega C}\frac{P_{\text{av}}}{V_{\text{DC}}}\sin(2\theta + \phi_{v2}). \tag{22}$$

Here, the error amplifier's gain and phase, at the frequency of the second harmonic, are denoted H_{v2} and ϕ_{v2} respectively. Combining (20), (21), and (22), yields the expression for the error amplifier output voltage delivered to the input of the divider as

$$v_e(\theta) = V_{e0} v_{en}(\theta), \tag{23}$$

where $v_{en}(\theta)$ is the normalized feedback voltage:

$$v_{en}(\theta) = \frac{v_{e(\theta)}}{V_{e0}} = 1 - \frac{K}{4V_{\text{DC}}}\frac{H_{v2}}{\omega C}\sin(2\theta + \phi_{v2}). \tag{24}$$

Note that the normalized second harmonic ripple component at the output of the error amplifier is constant and independent of the power level output voltage of the APFC. This observation forms the basis for the following development of the proposed ripple cancellation method.

6. The Current Programming Signal

To produce the correct current programming signal, the APFC circuit of Figure 1 uses the divider output, $v_d(\theta)$, to modulate the line voltage waveform. The divider output signal is calculated using (15) and (23) yielding

$$v_d(\theta) = k_d\left(\frac{v_e(\theta)}{v_{ff}(\theta)}\right) = \left(\frac{\pi^2}{2}\frac{k_d}{k_s K H_{f0}^2}\frac{P_{\text{av}}}{V_m^2}\right)v_{dn}(\theta). \tag{25}$$

Here, k_d is the divider gain constant and $v_{dn}(\theta)$ is the normalized divider output:

$$v_{dn}(\theta) = \frac{v_{en}(\theta)}{v_{ffn}(\theta)} = \frac{1 - (K/4V_{\text{DC}})(H_{v2}/\omega C)\sin(2\theta + \phi_{v2})}{1 - (4/3)\left(H_{f2}/H_{f0}\right)\cos\left(2\theta + \phi_{f2}\right)}. \tag{26}$$

The current programming signal, $v_{\text{cp}}(\theta)$, produced by modulation of the line voltage (1) with the divider output (25) is given by

$$\begin{aligned} v_{\text{cp}}(\theta) &= k_m v_d(\theta) v_{\text{in}}(\theta) \\ &= \left(\frac{\pi^2}{2}\frac{k_m k_d}{k_s}\frac{1}{K H_{f0}^2}\frac{P_{\text{av}}}{V_m}\right)v_{dn}(\theta)\sin(\theta), \end{aligned} \tag{27}$$

where k_m is the multiplier gain constant. The current programming signal amplitude is therefore

$$v_{\text{cp}m} = \left(\frac{\pi^2}{2}\frac{k_m k_d}{k_s}\frac{1}{K H_{f0}^2}\frac{P_{\text{av}}}{V_m}\right)v_{dn}(\theta). \tag{28}$$

Equations (27) and (28) reveal the mechanism by which distortion components of the outer loops are introduced into the current reference. The term $v_{dn}(\theta)$ contains harmonic components which modulates the current programming signal amplitude (28). Consequently, the input current of the APFC could not possibly be any less distorted than (27).

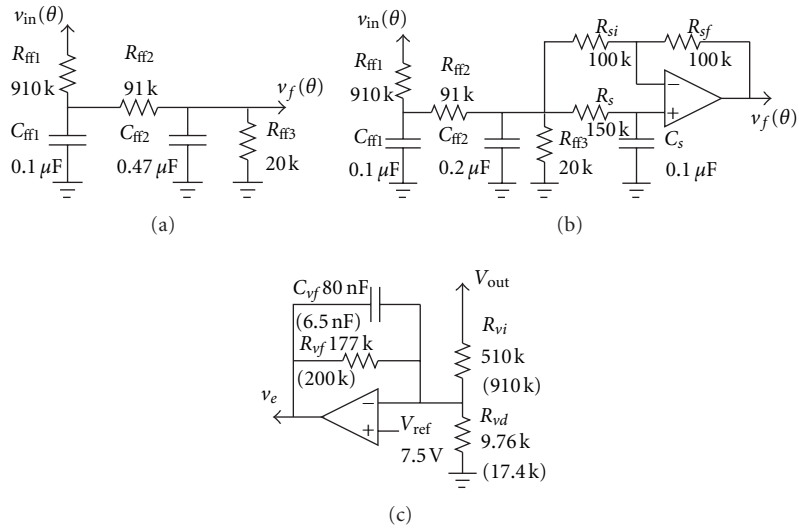

Figure 3: APFC feed-forward filters: original design (a); modified (b); voltage error amplifier configuration with original and modified (in brackets) values (c).

7. The Power Gain Constant

When the current loop tightly regulates the input current, the output voltage of the current sensing network, $v_{\text{sense}}(\theta)$, see Figure 1, is forced to follow the current programming signal, $v_{\text{cp}}(\theta)$:

$$v_{\text{sense}}(\theta) = v_{\text{cp}}(\theta). \tag{29}$$

In the most common case, the current sensing network is just a series resistance, R_s, so the amplitude of the sensed voltage is

$$V_{\text{sense}_m} = I_m R_s = 2\frac{P_{\text{av}}}{V_m} R_s. \tag{30}$$

The power gain constant K may be found substituting (28), (30) into (29) and assuming an ideal $v_{dn}(\theta)$, that is, (26) equals unity. This gives

$$K = \frac{\pi^2}{4}\frac{k_m k_d}{k_s}\frac{1}{R_s H_{f0}^2}. \tag{31}$$

This relationship remains valid also for the general case, when the current sensing network transfer function low frequency gain is denoted by R_s.

8. Filter Design for Minimum Line Current Distortion

Examination of (27) and (28) reveals that any harmonic disturbances at the divider output will produce cross products with the sine term. This will appear as harmonics in the current programming signal and cause distortion in the input current. Traditionally, the designers [15–18] minimize the distortion by providing large attenuation of the second harmonic, that is, minimizing the H_{v2} and H_{f2} terms in (16), (24), and (26). However, this has only a limited success for the following reasons. To ensure stability and adequate phase margin, the error amplifier usually has a single-pole transfer function of −20 db/decade gain roll off beyond its corner frequency and its filtering action is poor. Since the ripple frequency is quite low the bandwidth of the error amplifier is severely restricted resulting in poor transient response. A high-order low-pass filter may be used to achieve efficient filtering of the average component of the rectified input voltage. However, once again due to the low second harmonic frequency the filter has a narrow bandwidth and its transient response is rather poor. Here an alternative approach is proposed. Equations (27) and (28) suggest that it is possible to achieve distortion-free current programming signal by making the normalized divider output (26) equal unity:

$$v_{dn}(\theta) = \frac{1 - (K/4V_{\text{DC}})(H_{v2}/\omega C)\sin(2\theta + \phi_{v2})}{1 - (4/3)\left(H_{f2}/H_{f0}\right)\cos\left(2\theta + \phi_{f2}\right)} = 1. \tag{32}$$

To satisfy (32) requires that the normalized ripple components of the error and the feed-forward signals be equal both in amplitude and phase:

$$\frac{K}{4V_{\text{DC}}}\frac{H_{v2}}{\omega C}\sin(2\theta + \phi_{v2}) = \frac{4}{3}\frac{H_{f2}}{H_{f0}}\cos\left(2\theta + \phi_{f2}\right). \tag{33}$$

Since the normalized ripple components are of the same frequency and of a constant amplitude, it is possible to fulfill (34) by proper controller circuit design. For this purpose both amplitude and phase conditions must be satisfied. The amplitude condition defines the LPF attenuation needed to equate the amplitudes of the ripple components:

$$\frac{H_{f2}}{H_{f0}} = \frac{3K}{8V_{\text{DC}}}\frac{H_{v2}}{(2\omega)C}. \tag{34}$$

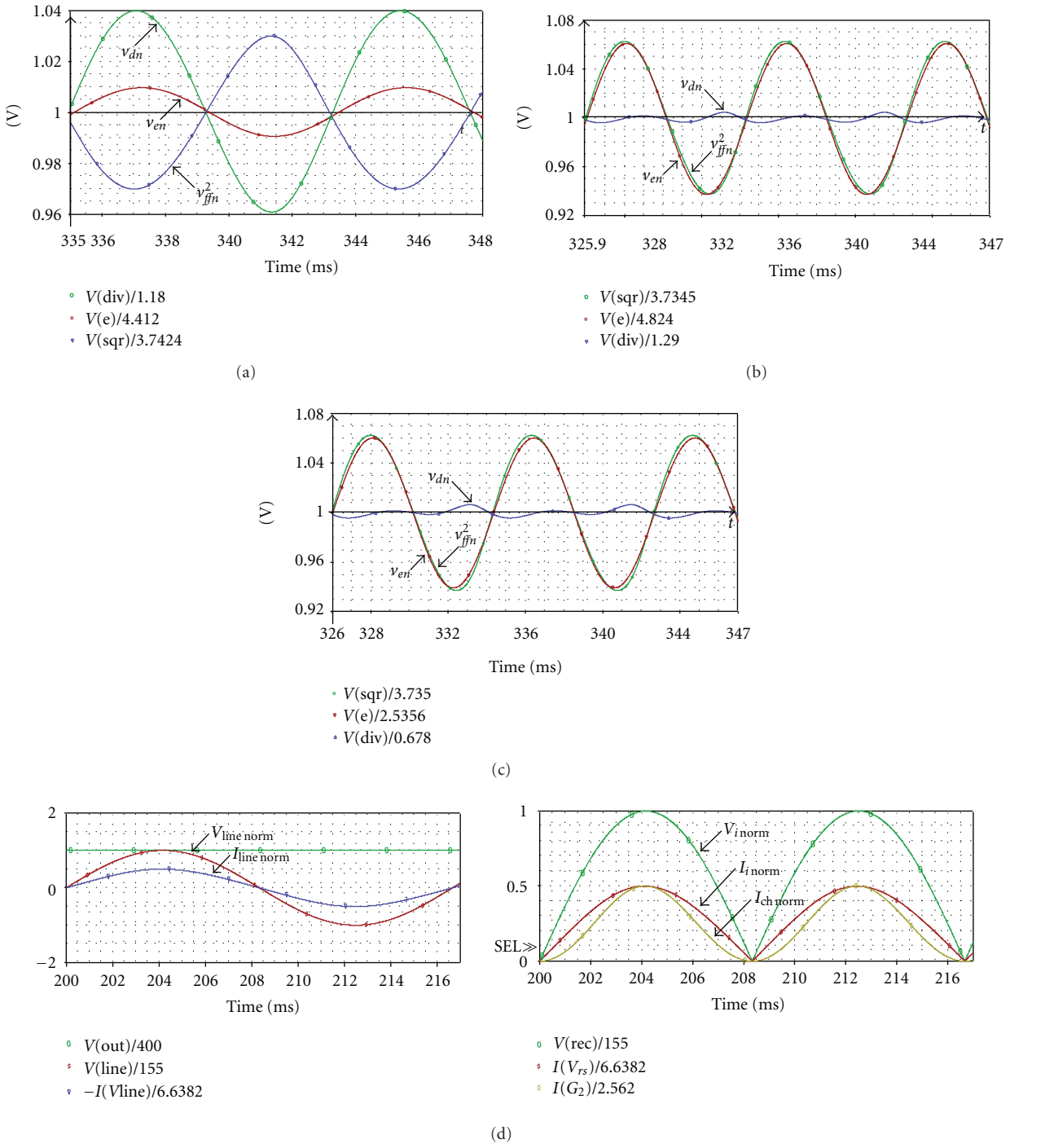

FIGURE 4: Normalized voltages of the error amplifier v_{en}, the feed-forward network v_{ffn}, and the divider output v_{dn}, in the original design (250 W) (a); modified design (250 W) (b), Modified design (125 W) (c), Modified design waveforms of the normalized rectified voltage V_{in}, converter's input current I_{in}, and the APFC's charging current I_{ch} (d).

This could be rearranged using (31) into the following form:

$$H_{f2} = \frac{3\pi}{128 f C R_s H_{f0} V_{\text{DC}}} \left(\frac{k_m k_d}{k_s}\right) H_{v2}, \tag{35}$$

where, f is the line frequency.

The phase condition could be derived by equating the sine and cosine terms in (33) and using elementary trigonometry relationship:

$$\cos\left(2\theta + \phi_{f2}\right) = \sin\left(2\theta + \phi_{v2}\right) = \cos\left(2\theta + \phi_{v2} - \frac{\pi}{2}\right). \tag{36}$$

Table 1: Analysis printout of the original circuit, full power (250 W).

Fourier components of transient response DC component = $2.758333E-04$					
Harm no.	Freq (Hz)	Fourier comp	Normalized comp	Phase (Deg)	Norm. phase (Deg)
1	$6.000E+01$	$3.198E+00$	$1.000E+00$	$-1.797E+02$	$0.000E+00$
2	$1.200E+02$	$4.295E-04$	$1.343E-04$	$1.456E+02$	$5.050E+02$
3	$1.800E+02$	$5.949E-02$	$1.860E-02$	$1.742E+01$	$5.565E+02$
4	$2.400E+02$	$1.831E-04$	$5.724E-05$	$-1.779E+02$	$5.408E+02$
5	$3.000E+02$	$1.372E-03$	$4.290E-04$	$2.705E-01$	$8.987E+02$
6	$3.600E+02$	$1.248E-04$	$3.903E-05$	$1.740E+02$	$1.252E+03$
7	$4.200E+02$	$1.649E-04$	$5.157E-05$	$6.782E+00$	$1.265E+03$
8	$4.800E+02$	$8.522E-05$	$2.665E-05$	$1.764E+02$	$1.614E+03$
9	$5.400E+02$	$1.090E-05$	$3.409E-06$	$1.197E+02$	$1.737E+03$
10	$6.000E+02$	$7.085E-05$	$2.215E-05$	$-1.798E+02$	$1.617E+03$
Total harmonic distortion = $1.860710E+00$ percent					

Table 2: Analysis printout of the modified circuit, full power (250 W).

Fourier components of transient response DC component = $3.755277E-04$					
Harm no.	Freq (Hz)	Fourier comp	Normalized comp	Phase (Deg)	Norm. phase (Deg)
1	$6.000E+01$	$3.424E+00$	$1.000E+00$	$1.800E+02$	$0.000E+00$
2	$1.200E+02$	$1.028E-03$	$3.002E-04$	$1.585E+02$	$-2.015E+02$
3	$1.800E+02$	$4.195E-03$	$1.225E-03$	$1.890E+01$	$-5.210E+02$
4	$2.400E+02$	$3.668E-04$	$1.071E-04$	$1.752E+02$	$-5.447E+02$
5	$3.000E+02$	$4.809E-03$	$1.405E-03$	$-1.639E+02$	$-1.064E+03$
6	$3.600E+02$	$2.352E-04$	$6.870E-05$	$1.797E+02$	$-9.001E+02$
7	$4.200E+02$	$1.009E-03$	$2.947E-04$	$-1.640E+02$	$-1.424E+03$
8	$4.800E+02$	$1.685E-04$	$4.922E-05$	$-1.782E+02$	$-1.618E+03$
9	$5.400E+02$	$3.725E-04$	$1.088E-04$	$-1.705E+02$	$-1.790E+03$
10	$6.000E+02$	$1.309E-04$	$3.824E-05$	$-1.777E+02$	$-1.977E+03$
Total harmonic distortion = $1.919198E-01$ percent					

Thus, the required phase shift of the LPF at the second harmonic frequency is

$$\phi_{f2} = \phi_{v2} - \frac{\pi}{2}. \tag{37}$$

The error amplifier transfer function is determined primarily by the stability and performance considerations of the outer loop. Consequently, to make the solutions of (34), (37) unique, the design of the feed-forward filter should be carried out after the complete knowledge of the error amplifier characteristics is gained. Note that ϕ_{v2}, as defined by (22), is the overall error amplifier phase shift. Since the phase shift of a single-pole error amplifier lags from the initial +180 degrees, due to the inverting configuration, to about +90, applying (37) requires about 0/360 degrees of LPF phase shift. Designing the feed-forward path filter according to the amplitude and phase conditions stated above will ensure minimum distortion of the PFC input current. It should be emphasized that, under the assumptions made, this approach will render a perfect current programming signal independent of the APFC power level.

9. Simulation Results

To study the performance of the APFC circuit of Figure 1, the system's model was simulated by PSPICE circuit simulator. The simulation was focused on the performance of the feedback and feed-forward loops under the assumption that the inner loop is ideal. The inner loop and power stage models were characterized by (4), (5), and (16) and implemented in PSPICE according to these behavioral relationships, see Figure 2. The design of the feed-forward LPF and voltage feedback amplifier followed the procedure discussed in [15, 16]. The program simulated a closed-loop PFC system fed by a rectified 110 V/60 Hz line and delivers $P_{\text{av}} = 250\,\text{W}$ at $V_{\text{DC}} = 400\,\text{V}$ to a resistive load of $640\,\Omega$. The holdup capacitor of 450 uF was chosen. The overall squarer-multiplier-divider constant, defined by external resistors, was set to $k_m k_d / k_s = R_m / R_{\text{AC}} = 3.9k/910k = 4.286 \cdot 10^{-3}$. Current sense resistor used was $R_s = 0.25\,\Omega$. According to Figure 3(b), the feed-forward filter transfer function was: $H_{f0} = (R_{ff3}/(R_{ff1} + R_{ff2} + R_{ff3})) = 19.59 \cdot 10^{-3}$. For these conditions, the numerical value of expression (31) equals $K = 110.2\,[\text{W/V}]$.

Table 3: Analysis printout of the modified circuit, half power (125 W).

Fourier components of transient response DC component = $3.755277E-04$					
Harm no.	Freq (Hz)	Fourier comp	Normalized comp	Phase (Deg)	Norm. phase (Deg)
1	$6.000E+01$	$1.801E+00$	$1.000E+00$	$1.799E+02$	$0.000E+00$
2	$1.200E+02$	$5.410E-0$	$3.004E-04$	$1.584E+02$	$-2.015E+02$
3	$1.800E+02$	$1.431E-03$	$7.949E-04$	$-2.125E+01$	$-5.611E+02$
4	$2.400E+02$	$1.938E-04$	$1.076E-04$	$1.753E+02$	$-5.444E+02$
5	$3.000E+02$	$2.529E-03$	$1.405E-03$	$-1.637E+02$	$-1.063E+03$
6	$3.600E+02$	$1.239E-04$	$6.883E-05$	$1.798E+02$	$-8.998E+02$
7	$4.200E+02$	$5.320E-04$	$2.955E-04$	$-1.638E+02$	$-1.423E+03$
8	$4.800E+02$	$8.877E-05$	$4.930E-05$	$-1.781E+02$	$-1.618E+03$
9	$5.400E+02$	$1.962E-04$	$1.090E-04$	$-1.704E+02$	$-1.790E+03$
10	$6.000E+02$	$6.895E-05$	$3.829E-05$	$-1.776E+02$	$-1.977E+03$
Total harmonic distortion = $1.677760E-01$ percent					

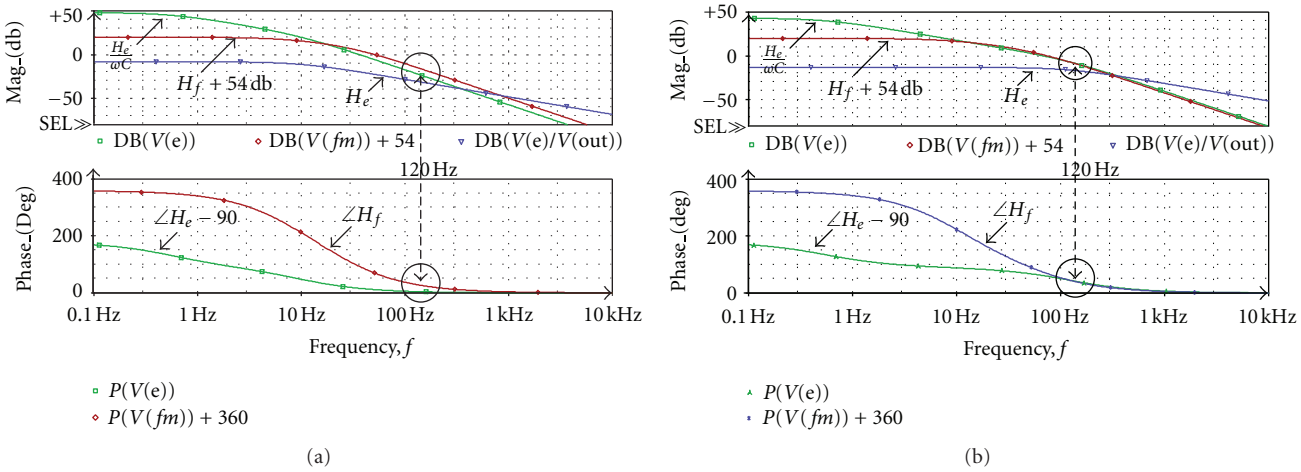

Figure 5: Frequency response of the error amplifier, H_e, and the feed-forward network, H_f, in the original design (a) and the modified design (b). Notice that the magnitude and phase conditions are satisfied at the vicinity of the second-line harmonic frequency.

To demonstrate the validity of the proposed ripple cancellation method, the LPF of the feed-forward network was modified to follow (34) and (37) as shown at Figure 3(b). New values were given to the error amplifier parameters as depicted in Figure 3(c). The simulation results of the original and proposed circuits are presented in Figures 4(a) and 4(b). Here, the normalized outputs of the voltage error amplifier, feed-forward, and divider circuits are shown. Comparison of the results reveals that the amplitude of the ripple voltage at the divider output is greatly reduced by the proposed method, reducing also the THD of the simulated APFC system. The normalized rectified line voltage and current as well as the APFC's charging currents are shown in Figure 4(c). Fourier analysis was carried out by SPICE on the simulated line current. Fourier analysis results are given in Tables 1, 2 and 3. The analysis reveals that the distorted current programming signal of the original design, see Table 1, contributes 1.86% to the total harmonic distortion of the APFC system, which is rather good performance index, whereas, using the proposed method the distortion is reduced to a negligible level of only 0.19%, see Table 2. That is about one order of magnitude improvement of THD.

10. Conclusions

One of the main sources of input current distortion in high-frequency APFC systems is the output voltage ripple which propagates into the feedback loop as well as the second harmonic of the line voltage injected through the feed-forward loop. These signals adversely affect the current reference signal quality.

This paper examined the propagation of the ripple components in the feedback and feed-forward loops of the APFC controller circuits and their interaction within the current shaping network. Based on this analysis, a ripple cancellation method is proposed. Analytical results are confirmed by simulation and show good agreement with predicted theoretical results. The simulation results suggest that the proposed method can reduce the THD of the input current

of PFC system by more than an order of magnitude. The present analysis and simulation were carried out under some simplifying assumptions, yet, second-order effects proved to be negligible.

Another important advantage of the proposed method is a dramatic increase of the error amplifier bandwidth, see Figure 5. This is possible in view of the fact that effective ripple cancellation requires a lesser amount of error amplifier attenuation of the second-line harmonic. Therefore, the outer feedback loop bandwidth becomes dominated by the relatively large holding capacitor, which value is determined primarily by the energy storage requirements.

The discussion of this paper is confined to the topology of one family of APFC controllers (Figure 1); however, the proposed approach could be expanded to other APFC schemes by following the idea of ripple compensation developed here.

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